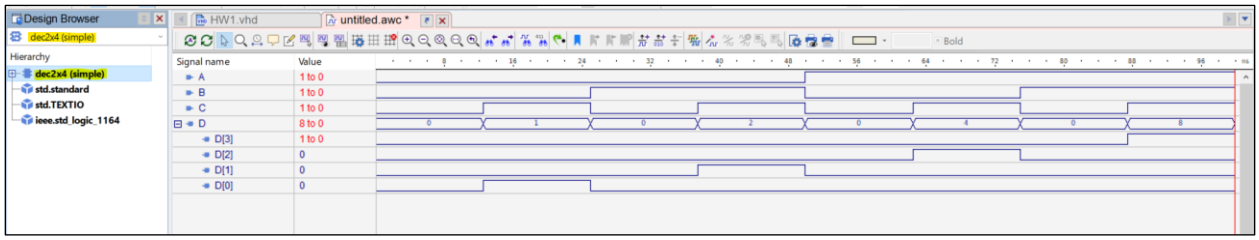
ENCS533

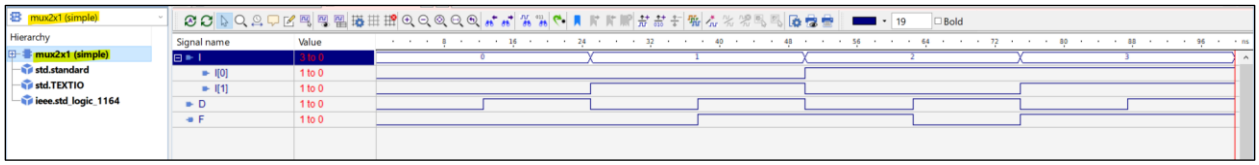
HW1 Simulations

TAREQ SHANNAK- 1181404

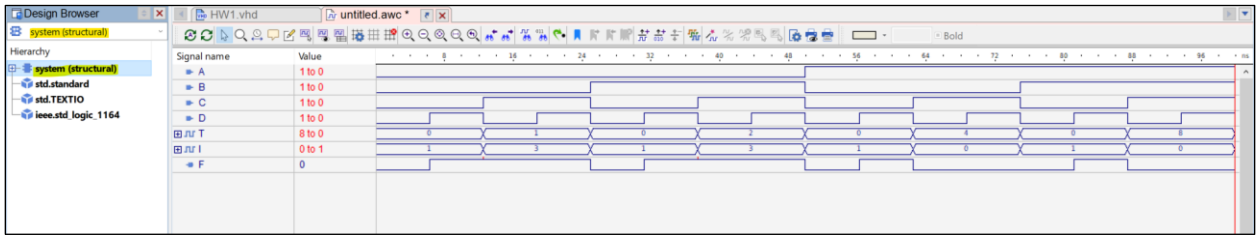
DECODER 2X4 WITH ENABLE



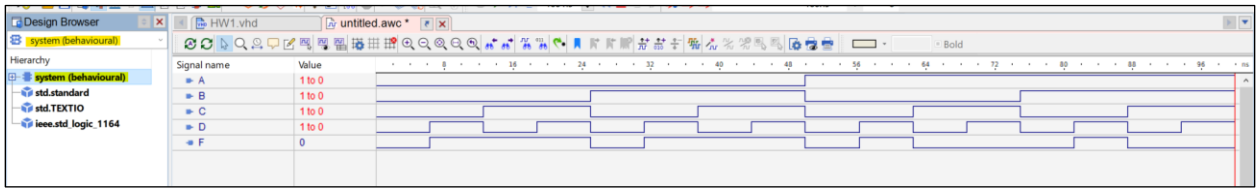
MULTIPLEXER 2X1



Simulation Of Structural Description for the Circuit



Simulation Of Behavioural Description for the Circuit



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HW 1 ENCS533

Truth Table:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

AB \ CD	00	01	11	10
00	0	1	1	1
01	0	1	1	1
11	0	1	0	0
10	0	1	0	0

$F = \bar{C}D + \bar{A}D + \bar{A}C$

$= \bar{C}D + C\bar{A}$