ADVANCED DIGITAL SYSTEMS DESIGN

HW_1_

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Section: 1

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❖ Procedure:

1- Decoder 2x4 :

- Code:

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity dec2x4 is
5       port(I:in std_logic_vector(1 downto 0);
6       En: in std_logic;
7       D:out std_logic_vector(3 downto 0));
8   end;
9
10  architecture Dec of dec2x4 is
11  begin
12      D(0)<= (not I(1) and not I(0)) and  En ;
13      D(1)<= (not I(1) and I(0) ) and  En ;
14      D(2)<= (I(1) and not I(0)) and En ;
15      D(3)<= (I(1) and I(0)) and En ;
16
17
18  end;
19
20
```

Fig_1_(code of decoder)

- Simulation:

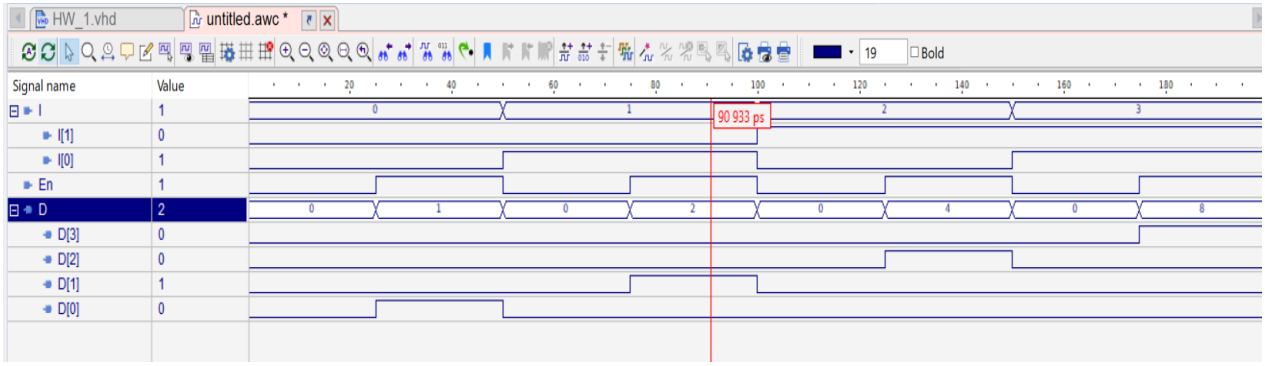

Fig_2_(simulation of decoder)

2- Multiplexer 2x1:

- Code:

```
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  entity mux2x1 is
24      port(I: in std_logic_vector(0 to 1);
25      S: in std_logic;
26      Y: out std_logic);
27  end;
28
29  architecture mux of mux2x1 is
30  begin
31
32      Y<= (I(0) and not S)
33      or (I(1) and S)  ;
34
35  end ;
36
```

Fig_3_(code of Multiplexer)

- Simulation:

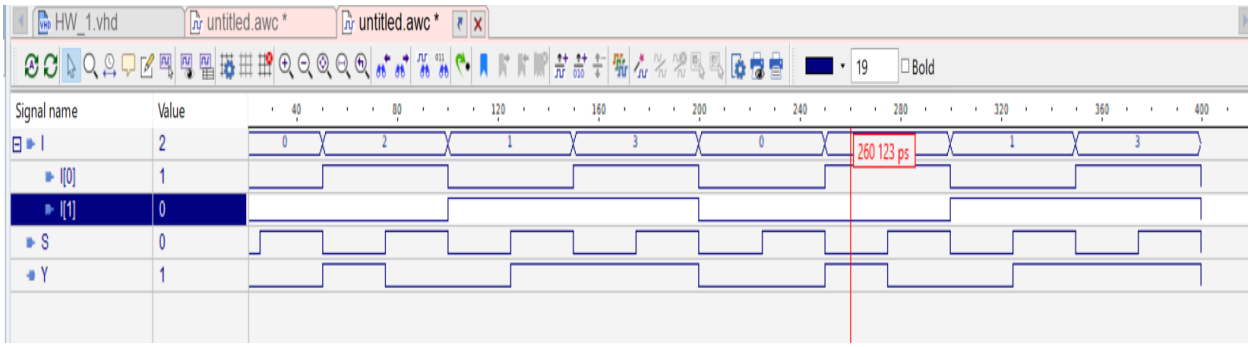

Fig_4_(simulation of Multiplexer)

3- All Circuit architecture:

- Code:

```
36
37  library ieee;
38  use ieee.std_logic_1164.all;
39  entity allcircuit is
40      port(A,B,C,D: in std_logic;
41      F: out std_logic);
42  end;
43
44  architecture structural of allcircuit is
45  signal inputs: std_logic_vector(1 downto 0);
46  signal j: std_logic_vector (3 downto 0);
47  signal l: std_logic_vector( 0 to 1);
48
49  begin
50      inputs<= A & B ;
51      l(0)<= j(0) xor j(1);
52      l(1)<= j(2) xnor j(3);
53
54      dec: entity work.dec2x4(Dec) port map(inputs,C,j);
55      max: entity work.mux2x1(mux) port map(l,D,F);
56  end;
57
58
```

Fig_5_(code of all circuit architecture)

- Simulation:

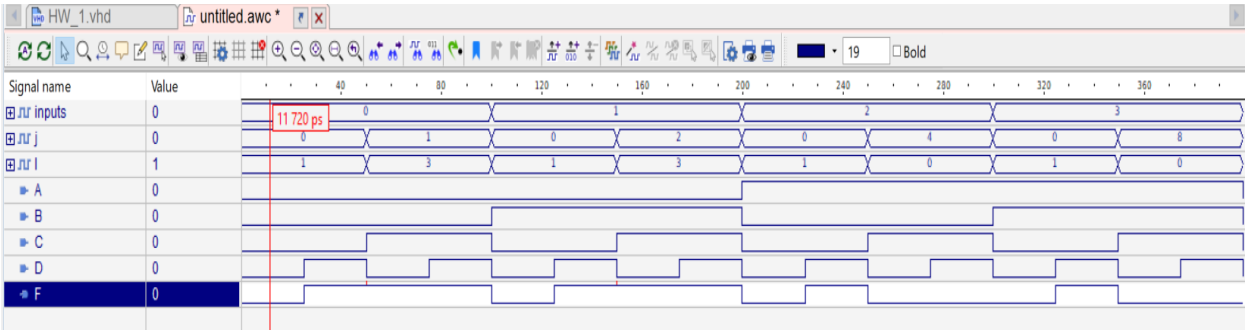

Fig_5_(simulation of all circuit architecture)

4- All circuit behavioral:

- Code:

```
57
58  architecture behavioral of allcircuit is
59  begin
60      F<= (not C and D) or (not A and C);
61  end;
62
63
64
```

Fig_6_(code of all circuit behavioral)

- Simulation:

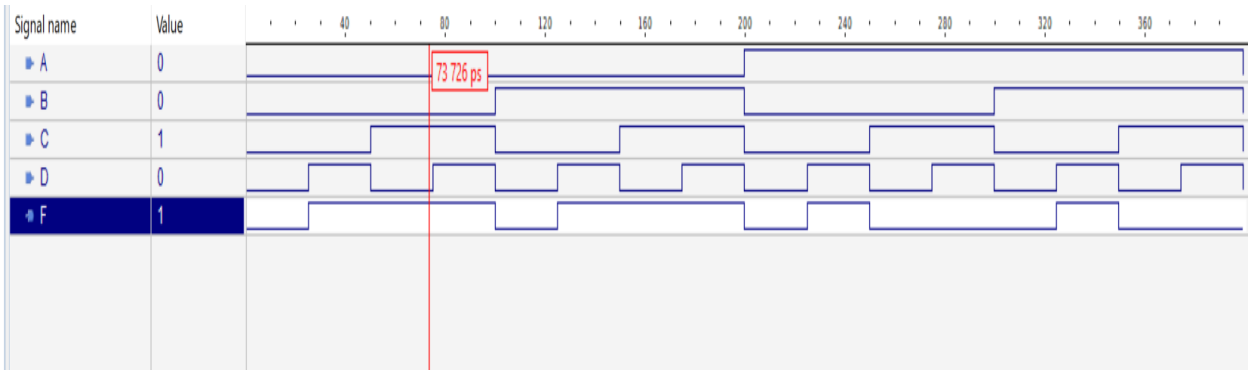

Fig_6_(simulation of all circuit behavioral)

❖ Truth table , key_map and the equation :

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

By the truth table i make key_map:

Map

	$\overline{C}.\overline{D}$	$\overline{C}.D$	$C.D$	$C.\overline{D}$
$\overline{A}.\overline{B}$	0	1	1	1
$\overline{A}.B$	0	1	1	1
$A.B$	0	1	0	0
$A.\overline{B}$	0	1	0	0

And hence the equation that we want is : F = C' . D + A' . C