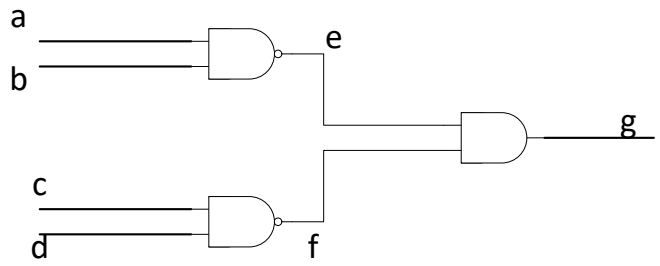
BIRZEIT UNIVERSITY

Faculty of Engineering and Technology
Electrical and Computer Engineering Departmen
Advanced Digital Design ENCS533
Homework#4

Q1) Use the following figure to answer the following questions:



a. Use Boolean Difference to find when the output g is sensitive to node a.
b. Use Boolean Difference to find when the output g is sensitive to node f.
c. Find the test vectors for a s-a-0 and s-a-1.
d. Find the test vectors for b s-a-0 and s-a-1.
e. Find the test vectors for c s-a-0 and s-a-1.
f. Find the test vectors for d s-a-0 and s-a-1.
g. Find the test vectors for e s-a-0 and s-a-1.
h. Find the test vectors for f s-a-0 and s-a-1.
i. Find the test vectors for g s-a-0 and s-a-1.
j. Find a minimum set of test vectors that can test all faults.
k. What is the Fault Coverage for these 4 test vectors together: “1100”, “0011”, “1011”, “1101”.

Answer:

Q1

a+c) $g = F(a,b,c,d)$

$= (a.b)' . (c.d)'$

$\frac{dg}{da} = F(a=0) \oplus F(a=1)$

$= (c.d)' \oplus \acute{b}.(cd)'$

$= (c.d).\acute{b}.(\acute{c}\acute{d}) + (c.d)'(b+(c.d))$

$= 0 + (c.d)'b + (c.d)'(c.d)$

$= (c.d)'.b$

g sensitive to a when $\frac{dg}{da} = 1$

$\frac{dg}{da} = 1$

$(c.d)'.b = 1$

b	c	d
1	0	0
1	0	1
1	1	0

→ a s-a-0 : $a.\frac{dg}{da} = 1$

$a.[(b.\acute{c}) + (\acute{d}.b)]$

a	b	c	d
1	1	0	0
1	1	0	1
1	1	1	0

→ a s-a-1 : $\acute{a}.\frac{dg}{da} = 1$

$\acute{a}.[(b.\acute{c}) + (\acute{d}.b)]$

a	b	c	d
0	1	0	0
0	1	0	1
0	1	1	0

-1-

b+h) $g = F(a,b,f)$
$= f \cdot (a \cdot b)'$

$\frac{dg}{df} = f(f=0) \oplus f(f=1)$
$= 0 \oplus (a \cdot b)'$
$= (a \cdot b)'$
$= \acute{a} + \acute{b}$

g sensitive to f when $\frac{dg}{df} = 1$

$\frac{dg}{df} = 1$

$\acute{a} + \acute{b} = 1$

a	b
0	1
1	0
0	0

→ f sa-0

$f \cdot \frac{dg}{df} = 1$

$(c \cdot d)' \cdot (\acute{a} + \acute{b}) = 1$

$(\acute{c} + \acute{d}) \cdot (\acute{a} + \acute{b}) = 1$

a	b	c	d
0	0	0	0
0	0	1	0
0	0	0	1
1	0	0	0
1	0	1	0
1	0	0	1
0	1	0	0
0	1	1	0
0	1	0	1

-2-

⟹ f s-a-1

$f \cdot \frac{dg}{df} = 1$

$(c \cdot d) \cdot (\acute{a} + \acute{b}) = 1$

a	b	c	d
0	0	1	1
1	0	1	1
0	1	1	1

⟹ Using fault equivilance:

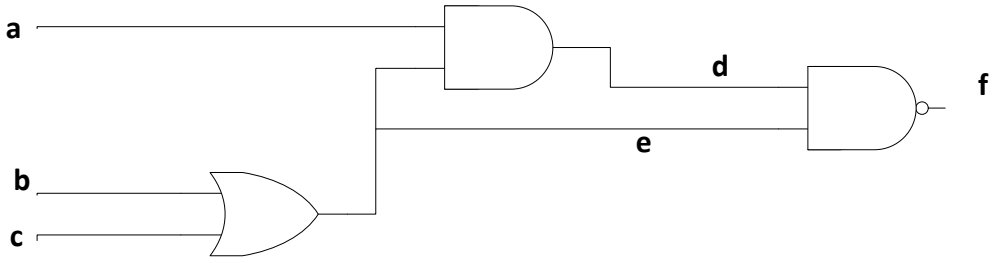
fault	Test vectors	Note
A s-a-0 B s-a-0 e s-a-1	1100, 1101, 1110	from Nand equal
c s-a-0 d s-a-0 f s-a-1	0011, 0111, 1011	from Nand
e s-a-0 f s-a-0 g s-a-0	0000, 0001, 0100, 1000 0101, 1001, 0010, 0110, 1010	from AND
A s-a-1	0110, 0101, 0100	from A s-a-0
b s-a-1	1000, 1010, 1001	from b s-a-0
c s-a-1	1001, 0101, 0001	from c s-a-0
d s-a-1	1010, 0110, 0010	from b s-a-0
g s-a-1	0011, 0111, 1011, 1100, 1101, 1110, 1111	from all-g s-a-0

j) the minimum of vector that can test all faults

1100 , 1001 , 0110 , 0011

k) the fault coverage = $\frac{4+3}{14} = \frac{7}{14} * 100\% = 50\%$

Q2) For the following figure

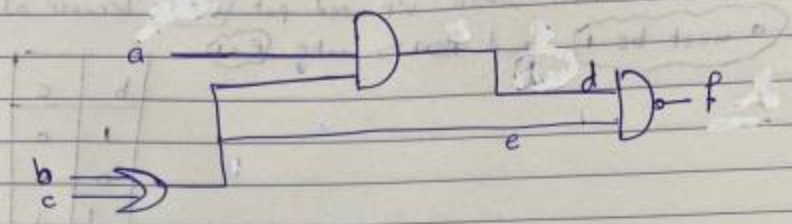


a) Use the D-algorithm method to find the test vectors for d s-a-0 and s-a-1 faults.
b) Use the D-algorithm method to find the test vectors for e s-a-0 and s-a-1 faults.

Answer:

Q2:

a) 1) d s-a-0



d s-a-0 this mean we need put (d=1), because of that (a must be 1) and (e=1) and to make (e=1)

b	c
0	1
1	0
1	1

∴

a	b	c
1	0	1
1	1	0
1	1	1

and $f = \acute{D}$

1 if no fault, 0 if faulty

2) d sa-1:

d s-a-0 this mean we need put (d=0), because of that (a must be 0) and (e=1) and to make (e=1)

b	c
0	1
1	0
1	1

∴

a	b	c
0	0	1
0	1	0
0	1	1

and $f = D$

1 if no fault, 0 if faulty

b) 1) e_s_a_0

e s_a_0 this mean we need put (e=1), because of that (a must be 1) and to make (e=1)

b	c
1	0
0	1
1	1

∴

a	b	c
1	1	0
1	0	1
1	1	1

and $f = \acute{D}$

0 if no fault 1 if faulty

2) e_s_a_1

e s_a_1 this mean we need put (e=0), because of that (a must be 1) and to make (e=0)

b	c
0	0

∴

a	b	c
1	0	0

and $f = D$

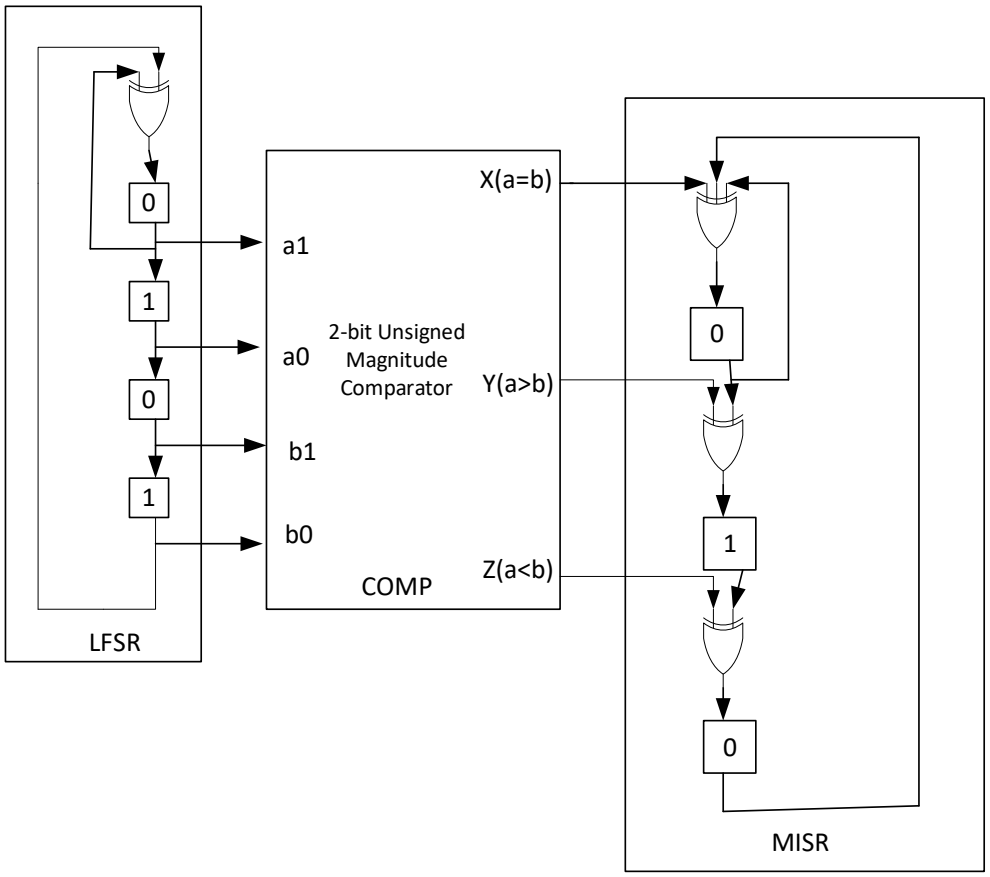
0 if faulty 1 if no fault

Q3) The following figure shows a Built-In Self-Test Circuit for a 2-bit comparator (unsigned magnitude comparator). The comparator will compare between 2 numbers a = a_1a_0 and b =b_1b_0. It will produce 3 outputs X(a=b), Y(a>b), and Z(a<b). The test vectors are generated using a 4-bit LFSR and the results are analysed using a 3-bit MISR as shown in the figure.

. **a)** Show the first 6 test vectors generated by the LFSR (Initial value of the LFSR are shown in the figure "0101", show the next 5 test vectors).

b) What is the fault free signature of this system after we generate these 6 test vectors using the LFSR? (Initial value of the MISR are shown in the figure "010").

c) Assume that the output X(a=b) is Sa0. What is the signature after we generate the same 6 test vectors using the LFSR? Comment on your result? (Initial value of MISR are shown in the figure "010")



Answer:

a) the first 6 test vectors generated by the LFSR

A1	A0	B1	B0
0	1	0	1
1	0	1	0
1	1	0	1
0	1	1	0
0	0	1	1
1	0	0	1

b) the fault free signature of this system after we generate these 6 test vectors using the LFSR

A1	A0	B1	B0	X(a=b)	Y(a>b)	Z(a<b)	C2	C1	C0
							0	1	0
0	1	0	1	1	0	0	1	0	1
1	0	1	0	1	0	0	1	1	0
1	1	0	1	0	1	0	1	0	1
0	1	1	0	0	0	1	0	1	1
0	0	1	1	0	0	1	1	0	0
1	0	0	1	0	1	0	1	0	0

NOTE : **signature = 100 , this is a good signature and the circuit fault free signature**

c) Assume that the output X(a=b) is Sa0. the signature after we generate the same 6 test vectors using the LFSR

A1	A0	B1	B0	X(a=b)	Y(a>b)	Z(a<b)	C2	C1	C0
							0	1	0
0	1	0	1	0	0	0	0	0	1
1	0	1	0	0	0	0	1	0	0
1	1	0	1	0	1	0	1	0	0
0	1	1	0	0	0	1	1	1	1
0	0	1	1	0	0	1	0	1	0
1	0	0	1	0	1	0	0	1	1

NOTE: **signature != good signature**

100 != 011

So the circuit faulty