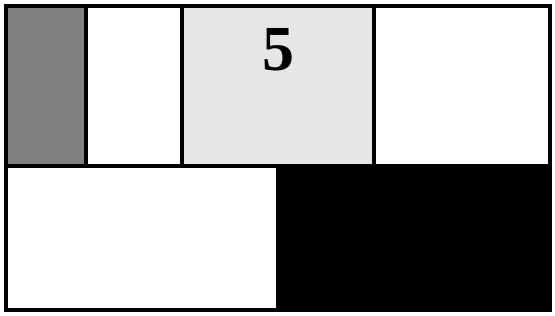
CHAPTER



THE CMOS INVERTER

Quantification of integrity, performance, and energy metrics of an inverter
Optimization of an inverter design

5.1 Exercises and Design Problems

1. [M, SPICE, 3.3.2] The layout of a static CMOS inverter is given in Figure 5.1. (λ = 0.125 µm).

a. Determine the sizes of the NMOS and PMOS transistors.

Solution

The sizes are w_n=1.0µm, l_n=0.25µm, w_p=0.5µm, and l_p=0.25 µm.

b. Plot the VTC (using HSPICE) and derive its parameters (V_{OH}, V_{OL}, V_M, V_{IH}, and V_{IL}).

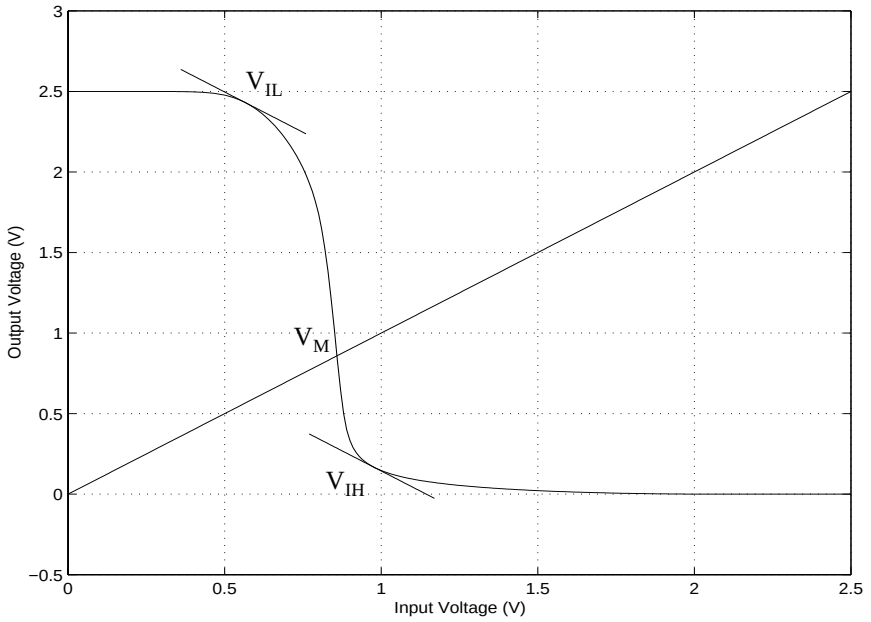
Solution

The inverter VTC is shown below. For a static CMOS inverter with a supply voltage of 2.5 V, V_{OH} =2.5 V and V_{OL}=0 V. In order to calculate V_m, note from the VTC that the value is between 0.8 V and 0.9 V. Therefore, the NMOS is saturated and the PMOS is velocity saturated. Let $V_{in}=V_{out}=V_m$ and set the currents equal to obtain the following equation:

$$(k_n/2)(V_{GS}-V_{TN})^2(1+\lambda V_{DS})=k_p V_{DSAT}[(V_{GS}-V_{TP})-(V_{DSAT}/2)](1+\lambda V_{DS})$$

Substitute the appropriate values and solve numerically to find V_m=0.883 V.

Use the VTC data to solve for V_{IL} and V_{IH} numerically. The result is that V_{IH}=0.97 V and V_{IL}=0.56 V.



c. Is the VTC affected when the output of the gates is connected to the inputs of 4 similar gates?

Solution

No. CMOS gates are a purely capacitive load so the DC circuit characteristics are not affected.

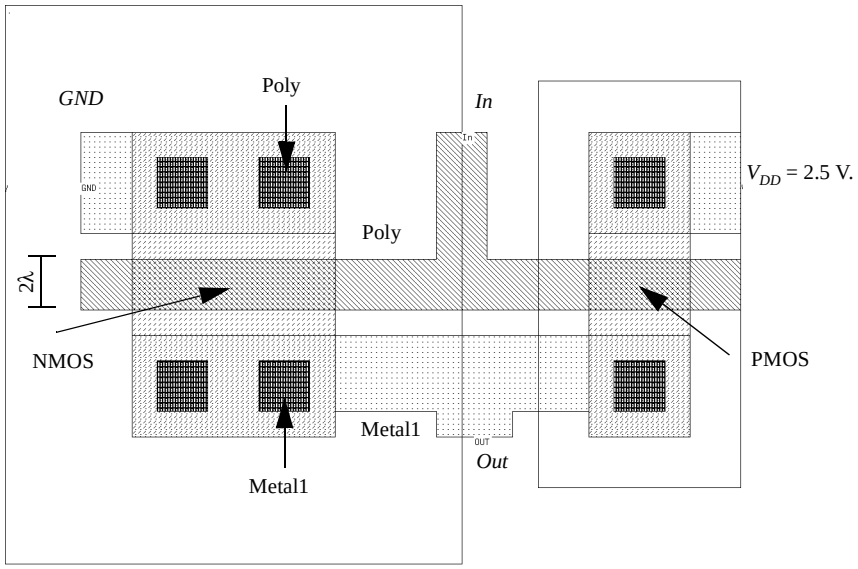


Figure 5.1 CMOS inverter layout.

d. Resize the inverter to achieve a switching threshold of approximately 0.75 V. Do not lay-out the new inverter, use HSPICE for your simulations. How are the noise margins affected by this modification?

Solution

Changing the NMOS sizing to w_n=2.0µm moves the switching threshold to 0.75 V. This increases N_{MH} and decreases N_{ML}.

2. Figure 5.2 shows a piecewise linear approximation for the VTC. The transition region is approximated by a straight line with a slope equal to the inverter gain at V_M. The intersection of this line with the V_{OH} and the V_{OL} lines defines V_{IH} and V_{IL}.

a. The noise margins of a CMOS inverter are highly dependent on the sizing ratio, $r = k_p/k_n$, of the NMOS and PMOS transistors. Use HSPICE with $V_{Tn} = |V_{Tp}|$ to determine the value of r that results in equal noise margins? Give a qualitative explanation.

Solution

The TSMC 0.25µm models were used for simulation and the threshold voltages of NMOS and PMOS devices are nearly equal in this process. A value near r=1 should result in equal noise margins, since the transistors will be closely matched. HSPICE showed that the resulting noise margins for this sizing were N_{MH}=0.97 V and N_{ML}=1.1 V. The mismatch is due to the fact that the PMOS threshold voltage is actually slightly lower, so the PMOS is stronger and the upper noise margin is reduced. The actual value that results in equal noise margins is r=0.83.

b. Section 5.3.2 of the text uses this piecewise linear approximation to derive simplified expressions for NM_H and NM_L in terms of the inverter gain. The derivation of the gain is based on the assumption that both the NMOS and the PMOS devices are velocity saturated at V_M. For what range of r is this assumption valid? What is the resulting range of V_M?

Solution

Using the equations for finding the region of operation, it can be shown that the PMOS and NMOS are both velocity saturated only while the switching threshold is between 1.06 V and 1.10 V. Since this range may be considered inclusive, we can assume that both devices are velocity saturated and set the currents equal with $V_{IN}=V_{OUT}=V_M$ to find k_p/k_n . The result is that k_p/k_n must be between 0.34 and 0.41. This result can be checked by sizing the devices accordingly and testing the resulting V_M in HSPICE. The result gives a range of 1.04 V to 1.09 V. This makes sense, because the NMOS must be much stronger than the PMOS to achieve a switching threshold near 1 V.

c. Derive expressions for the inverter gain at V_M for the cases when the sizing ratio is just above and just below the limits of the range where both devices are velocity saturated. What are the operating regions of the NMOS and the PMOS for each case? Consider the effect of channel-length modulation by using the following expression for the small-signal resistance in the saturation region: $r_{o,sat} = 1/(\lambda I_D)$.

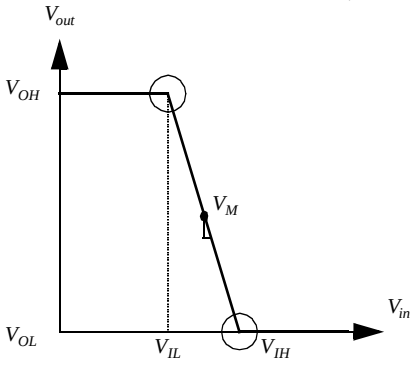


Figure 5.2 A different approach to derive V_{IL} and V_{IH}.

Solution:

When V_M is slightly larger than 1.1 V, the NMOS is velocity saturated and the PMOS is saturated. When V_M is slightly smaller than 1.06 V, the PMOS is velocity saturated and the NMOS is saturated. Section 5.3.2 of the text shows this derivation for the case when both devices are velocity saturated. These derivations can be completed by substituting the correct current equations and using the same method. The results are as follows:

For the case when the NMOS is saturated and the PMOS is velocity saturated:

$$\frac{dV_{out}}{dV_{in}} = -\frac{k_n(V_{in}-V_{tn})(1+\lambda_n V_{out})+k_p V_{DSATP}(1+\lambda_p(V_{out}-V_{DD}))}{\frac{k_n\lambda_n}{2}(V_{in}-V_{tn})^2+k_p V_{DSATP}\lambda_p\left(V_{in}-V_{DD}-V_{tp}-\frac{V_{DSATP}}{2}\right)}$$

Dropping the second order terms in the numerator, substituting V_m for V_{in}, and simplifying the denominator leads to the following expression for the gain:

$$\frac{dV_{out}}{dV_{in}} = -\frac{k_n(V_m-V_{tn})+k_p V_{DSATP}}{I_D(V_m)(\lambda_n-\lambda_p)}$$

For the case when the NMOS is velocity saturated and the PMOS is saturated:

$$\frac{dV_{out}}{dV_{in}} = -\frac{k_n V_{DSATN}(1+\lambda_n V_{out})+k_p(V_{in}-V_{DD}-V_{tp})(1+\lambda_p(V_{out}-V_{DD}))}{k_n V_{DSATN}\lambda_n\left(V_{in}-V_{tn}-\frac{V_{DSATN}}{2}\right)+\frac{k_p\lambda_p}{2}(V_{in}-V_{DD}-V_{tp})^2}$$

Again, dropping the second order terms in the numerator, substituting V_m for V_{in}, and simplifying the denominator leads to the following expression for the gain:

$$\frac{dV_{out}}{dV_{in}} = -\frac{k_n V_{DSATN} + k_p(V_m - V_{DD} - V_{tp})}{I_D(V_m)(\lambda_n - \lambda_p)}$$

3. [M, SPICE, 3.3.2] Figure 5.3 shows an NMOS inverter with a resistive load.

a. Qualitatively discuss why this circuit behaves as an inverter.

Solution

For $V_{IN} < V_T$, M1 is in cutoff regime, thus I=0 and V_{out}=2.5V. For $V_{IN} > V_T$, M1 is conducting and V_{out}=2.5V - (I*R). This in turn gives a low V_{out} and the input signal is inverted.

b. Find V_{OH} and V_{OL} calculate V_{IH} and V_{IL}.

Solution

Assuming negligable leakage, when $V_{in} < V_T$, transistor M1 is off and V_{OH}=2.5V. For V_{in}=2.5V, assume M1 is in the linear region, and because V_{DS} is negligable in the linear region, channel-length modulation can be ignored. For the linear region, $V_{min}=V_{DS}=V_{out}=V_{OL}$ =46.25m. Checking the assumption: V_{GT}=2.07V, V_{DSat}=0.63V, and V_{DS}=46.25m, thus, M1 was correctly assumed to be in the linear region.

To find V_M, set the resistor current equal to the NMOS current, with an input and out put voltage of V_M.

$$\frac{2.5 - V_M}{75k} = k_n \frac{(V - 0.43)^2}{2}(1 + 0.06V_M)$$

Thus, V_M = 0.79V.

To find V_{IL} and V_{IH}, the slope of the VTC, at V_M, is derived and the line is extrapolated out to V_{OH} and V_{OL} respectively. Ignoring the effects of channel length modulation, the slope is given by the following:

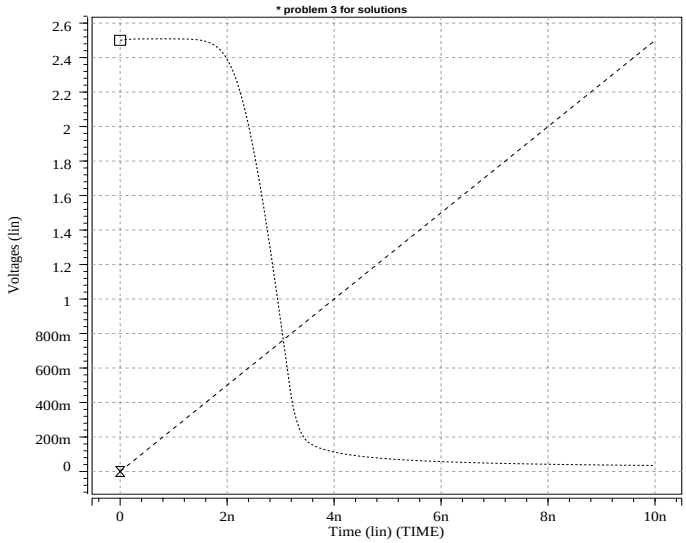
$$\frac{dV_o}{dV_{in}} = -\frac{R_L k_n W}{2L}(2V_{in} - 0.86)$$

Plugging V_M =0.79V, into the slope equation above, gives a slope of 9.32. Extrapolating the line back to V_{OH} gives V_{IL}=0.607V and the extrapolation of the line to V_{OL} gives V_{IH}=0.87V.

c. Find NM_L and NM_H, and plot the VTC using HSPICE.

Solution

$NM_L = V_{IL}$ = 0.607V and NM_H = 2.5V - V_{IH} = 1.63V



d. Compute the average power dissipation for: (i) V_{in} = 0 V and (ii) V_{in} = 2.5 V

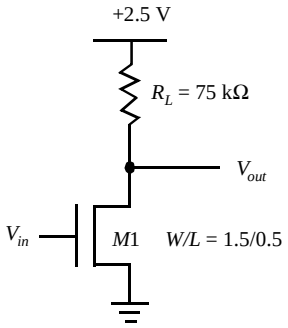


Figure 5.3 Resistive-load inverter

Solution

(i) V_{in}=0 means M1 is cutoff, therefore, I_{VDD}=0 and consequently P_{VDD}=0

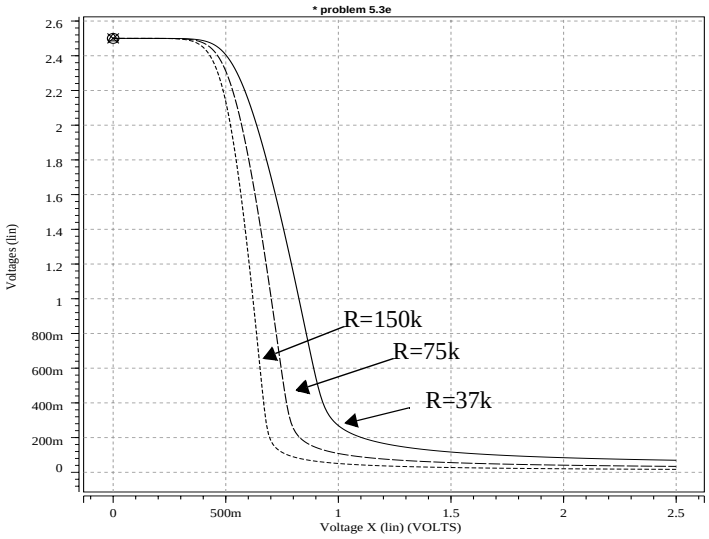
(ii) V_{in}=2.5V, V_{out}=V_{OL}=46.25mV,

$$I_{VDD} = \frac{\Delta V}{R} = \frac{2.5 - 46.25m}{75k} = 32.7uA$$

P=V_{DD}*I_{VDD}=2.5V*32.7mA=81.75mW

e. Use HSPICE to sketch the VTCs for R_L = 37k, 75k, and 150k on a single graph.

Solution



f. Comment on the relationship between the critical VTC voltages (i.e., V_{OL}, V_{OH}, V_{IL}, V_{IH}) and the load resistance, R_L.

Solution

As R_L increases, the VTC curve becomes more ideal for the following reasons: V_{OL} decreases, NM_L increases, V_{IH} decreases, and NM_H increases. However, these come as tradeoffs because, as R_L increases, V_{IL} decreases, which is less ideal, and V_{OH} remains unchanged.

g. Do high or low impedance loads seem to produce more ideal inverter characteristics?

Solution

As the impedance load increases, there is a tradeoff, the inverter VTC becomes more ideal with a higher gain and thus better noise margins. However, the VTC curve is shifted in favor of M1 and the threshold voltage is lowered as the VTC moves to the left.

4. [E, None, 3.3.3] For the inverter of Figure 5.3 and an output load of 3 pF:

a. Calculate t_{plh}, t_{phl}, and t_p.

Solution

$t_{pLH}=0.69R_LC_L=$ 155 nsec.

For t_{pHL}: First calculate R_{on} for V_{out} at 2.5V and 1.25V. At V_{out}=2.5V, I_{DVsat}=0.439mA giving R_{on}= 5695Ω and when V_{out}=1.25V, I_{Dvsat}=0.41m giving R_{on}= 3049W.

Thus, the average resistance between V_{out}=2.5Vand V_{out}=1.25V is $R_{average}$=4.372kΩ. $t_{pLH}=0.69R_{average}C_L$=9.05nsec.

t_p=av{t_{pLH}, t_{pHL}}=82.0nsec

b. Are the rising and falling delays equal? Why or why not?

Solution

t_{pLH} >> t_{pHL} because R_L=75kΩ is much larger than the effective linearized on-resistance of M1.

c. Compute the static and dynamic power dissipation assuming the gate is clocked as fast as possible.

Solution

Static Power:

$V_{IN}=V_{OL}$ gives $V_{out}=V_{OH}$=2.5V, thus I_{VDD}=0A so P_{VDD}=0W.
$V_{IN}=V_{OH}$ gives $V_{out}=V_{OL}$=46.3mV, which is in the linear region.

Calculating the current through M1 gives I_{VDD}=32.8mA --> P_{VDD}=82mW

Dynamic Power:

$P_{dyn}=C_L\Delta V*V_{dd}*f_{max}$=3pF*(2.5V-46.3mV)*2.5V*12.2MHz=0.225mW.

5. The next figure shows two implementations of MOS inverters. The first inverter uses only NMOS transistors.

a. Calculate V_{OH}, V_{OL}, V_M for each case.

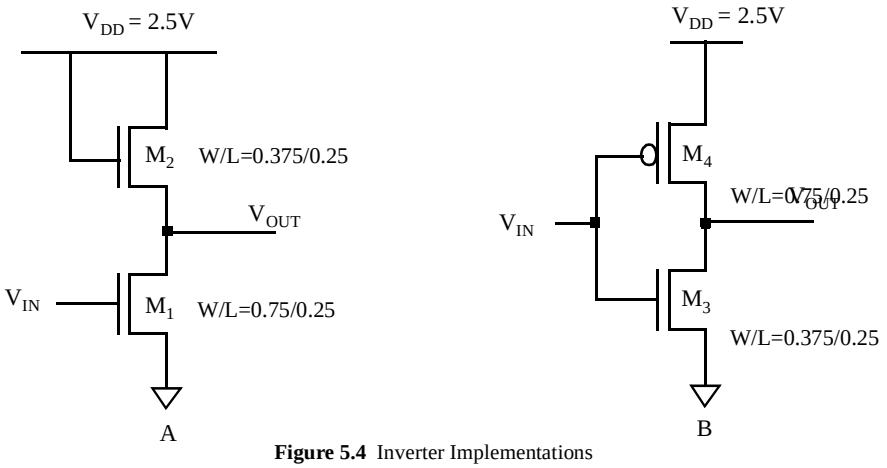


Figure 5.4 Inverter Implementations

Solution

Circuit A.

V_{OH}: We calculate V_{OH}, when M1 is off. The threshold for M2 is:

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|-2\phi_F\right|}\right),\ V_{SB} = V_{OUT},\ \left|-2\phi_F\right| = 0.6V$$

and M2 will be off when: $V_{GS} - V_T = V_{DD} - V_{OUT} - V_T = 0$,
Substitute V_T in the last equation and solve for V_{OUT}.

$$V_{DD} - V_{OUT} - V_T = 2.5 - V_{OUT} - (0.43 + 0.4 \cdot (\sqrt{|0.6 + V_{OUT}|} - \sqrt{|0.6|})) = 0$$

We get **$V_{OUT}=V_{OH}$=1.765V**

V_{OL}: To calculate V_{OL}, we set $V_{IN}=V_{DD}$=2.5V.

We expect V_{OUT} to be low, so we can make the assumption that M2 will be velocity saturated and M1 will be in the linear region.

For M2: $I_{D2} = k'_n \cdot \frac{W_2}{L_2} \cdot \left((V_{GS} - V_T) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) \cdot (1 + \lambda V_{DS})$ and

for M1: $I_{D1} = k'_n \cdot \frac{W_1}{L_1} \cdot \left((V_{GS} - V_{T0}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right)$

Setting $I_{D1} = I_{D2}$, we get an equation and we solve for V_{OUT}.
We get: $\mathbf{V_{OUT}=V_{OL}=0.263V}$, so our assumption holds.

V_M: To calculate V_M we set $V_M=V_{IN}=V_{OUT}$.

Assuming that both transistors are velocity saturated, then we have the next pair of equations:

$$I_{D1} = k'_n \cdot \frac{W_1}{L_1} \cdot \left((V_M - V_{T0}) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) \cdot (1 + \lambda V_M)$$

$$I_{D2} = k'_n \cdot \frac{W_2}{L_2} \cdot \left((V_{DD} - V_M - V_T) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) \cdot (1 + \lambda (V_{DD} - V_M))$$

Setting $I_{D1} = I_{D2}$, we get for $\mathbf{V_M = 1.269V}$

Circuit B.

When V_{IN}=0V, the NMOS transistor is off and the PMOS transistor in on and pulls V_{OUT} up to V_{DD}, so $\mathbf{V_{OH}=2.5}$. Similarly, when V_{IN}=2.5V, the PMOS transistor is off and the NMOS transistor pulls V_{OUT} all the way down to ground, so V_{OL}=0V.

To calculate V_M we set $V_M=V_{IN}=V_{OUT}$.

We assume that both transistors are velocity saturated. We get the following pair of equations.

$$I_{D4} = k'_p \cdot \frac{W_4}{L_4} \cdot \left((V_M - V_{DD} - V_{T0p}) \cdot V_{DSATp} - \frac{V_{DSATp}^2}{2} \right) \cdot (1 + \lambda_p V_M)$$

$$I_{D3} = k'_n \cdot \frac{W_3}{L_3} \cdot \left((V_M - V_{T0n}) \cdot V_{DSATn} - \frac{V_{DSATn}^2}{2} \right) \cdot (1 + \lambda_n V_M)$$

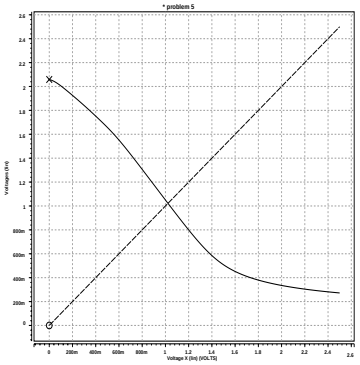
Setting $I_{D3} + I_{D2} = 0$, we get for $\mathbf{V_M = 1.095V.}$

So the assumption that both transistors were velocity saturated holds.

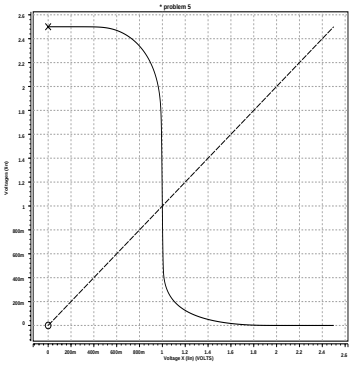
b. Use HSPICE to obtain the two VTCs. You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, λ = 0.125 μm, and the source/drain extensions are 5λ for the PMOS; for the NMOS the source/drain contact regions are 5λx5λ.

Solution

The two VTCs are shown below.



Depletion Load Inverter



CMOS Inverter

c. Find V_{IH}, V_{IL}, NM_L and NM_H for each inverter and comment on the results. How can you increase the noise margins and reduce the undefined region?

Solution

Circuit A

V_{IL} = 0.503V => V_{OUT1} = 1.65V, V_{IH} = 1.35V => V_{OUT2} = 0.588V

$NM_H = V_{OH} - V_{OUT2}$ = 1.765 - 1.65 = 0.115V, $NM_L = V_{OUT1} - V_{OL}$ = 0.588- 0.23 = 0.358V

Circuit B

V_{IL} = 0.861V => V_{OUT1} = 2.33V, V_{IH} = 1.22V => V_{OUT2} = 0.219V

$NM_H = V_{OH} - V_{OUT2}$ = 2.5V - 1.22V = 1.28V, $NM_L = V_{OUT1} - V_{OL}$ = 0.861V- 0V = 0.861V

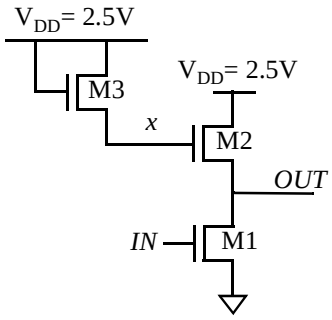
We can increase the noise margins by moving V_M closer to the middle of the output voltage swing.

d. Comment on the differences in the VTCs, robustness and regeneration of each inverter.

Solution

It is clear from the two VTCs, that the CMOS inverter is more robust, since the low and high noise margins are higher than the first inverter. Also the regeneration in the second inverter is greater since it provides rail to rail output and the gain of the inverter is much greater.

6. Consider the following NMOS inverter. Assume that the bulk terminals of all NMOS devices are connected to GND. Assume that the input IN has a 0V to 2.5V swing.



a. Set up the equation(s) to compute the voltage on node *x*. Assume γ=0.5.

Solution

The voltage on node x is set to one threshold value V_T below V_{DD}. So:

$$V_X = V_{DD} - V_T$$

$$V_X = V_{DD} - [V_{T0} + \gamma(\sqrt{V_{SB} + |-2\phi_F|} - \sqrt{|-2\phi_F|})]$$

$$V_X = 2.5 - [0.43 + 0.5(\sqrt{V_X + 0.6} - \sqrt{0.6})]$$

$$V_X = 2.07 + 0.39 - 0.5\sqrt{V_X + 0.6}$$

$$V_X = 2.46 - 0.5\sqrt{V_X + 0.6}$$

which gives V_X=1.7014V.

b. What are the modes of operation of device M2? Assume γ=0.

Solution

$$V_X = V_{DD} - V_T$$

$$V_{DS2} = V_{DD} - V_{OUT}$$

$$V_{GS2} - V_T = V_{DD} - V_T - V_{OUT} - V_T = V_{DD} - V_{OUT} - 2V_T$$

This means that $V_{DS2} > V_{GS2} - V_T$, so M2 is either saturated (or vel. saturated) or cut off.

c. What is the value on the output node *OUT* for the case when *IN* =0V?Assume γ=0.

Solution

When IN=0 then M1 is off and OUT will charge up to:

$$V_{out(max)} = V_X - V_T$$

$$V_{out(max)} = V_{DD} - V_T - V_T$$

$$V_{out(max)} = V_{DD} - 2V_T$$

d. Assuming γ=0, derive an expression for the switching threshold (V_M) of the inverter. Recall that the switching threshold is the point where $V_{IN} = V_{OUT}$. Assume that the device sizes for M1, M2 and M3 are $(W/L)_1$, $(W/L)_2$, and $(W/L)_3$ respectively. What are the limits on the switching threshold?

For this, consider two cases:

i) $(W/L)_1 >> (W/L)_2$

ii) $(W/L)_2 >> (W/L)_1$

Solution

Assuming that both devises are velocity saturated we can equate the currents when $V_{IN} = V_{OUT} = V_M$. This gives

$$k'_n\left(\frac{W}{L}\right)_1\left(V_{GS1}-V_T-\frac{V_{DSAT}}{2}\right)=k'_n\left(\frac{W}{L}\right)_2\left(V_{GS2}-V_T-\frac{V_{DSAT}}{2}\right)$$

$$\left(\frac{W}{L}\right)_1\left(V_M-V_T-\frac{V_{DSAT}}{2}\right)=\left(\frac{W}{L}\right)_2\left(V_{DD}-V_T-V_M-V_T-\frac{V_{DSAT}}{2}\right)$$

Solving for V_M and substituting $r = \frac{(W/L)_2}{(W/L)_1}$ we get:

$$\left(V_M-V_T-\frac{V_{DSAT}}{2}\right)=r\left(V_{DD}-2V_T-V_M-\frac{V_{DSAT}}{2}\right)$$

$$V_M=\frac{r\left(V_{DD}-2V_T-\frac{V_{DSAT}}{2}\right)+V_T+\frac{V_{DSAT}}{2}}{1+r}$$

To find the limits for V_M we check the two cases:

i) When $(W/L)_1 >> (W/L)_2$, $V_M = V_T + V_{DSAT}/2 = 0.43 + 0.63/2 = 0.745$

ii) When $(W/L)_2 >> (W/L)_1$, $V_M = V_{DD} - 2V_T - V_{DSAT}/2 = 1.325$

For both cases the assumptions for M1 and M2 are valid.

7. Consider the circuit in Figure 5.5. Device M1 is a standard NMOS device. Device M2 has all the same properties as M1, except that its device threshold voltage is *negative* and has a value of -0.4V. Assume that all the current equations and inequality equations (to determine the mode of operation) for the depletion device M2 are the same as a regular NMOS. Assume that the input *IN* has a 0V to 2.5V swing.

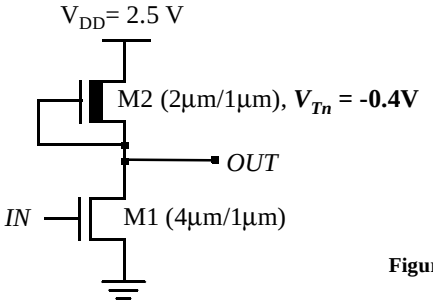


Figure 5.5 A depletion load NMOS inverter

a. Device M2 has its gate terminal connected to its source terminal. If V_{IN} = 0V, what is the output voltage? In steady state, what is the mode of operation of device M2 for this input?

Solution

When V_{IN} = 0V then M1 is off. M2 is on since $V_{GS}=0 > V_{Tn2}$. Since there is no current through M2, the drain to source voltage of M2 is 0 (linear mode). This means that V_{OUT}=2.5V.

b. Compute the output voltage for V_{IN} = 2.5V. You may assume that V_{OUT} is small to simplify your calculation. In steady state, what is the mode of operation of device M2 for this input?

Solution

We assume that M1 is in the linear mode and M2 is velocity saturated. This means:

$$k_{n1}\left[(2.5-0.4)V_{out}-\frac{V_{out}^2}{2}\right] = k_{n2}\left[(0-(-0.4))V_{Dsat}-\frac{V_{Dsat}^2}{2}\right]$$

Since V_{out} is small we can neglect the $V^2_{out}/2$ term and the previous equation becomes

$$V_{out} = \frac{k_{n2}}{k_{n1}}\frac{0.05355}{2.1}, \text{ which gives } V_{out} \cong 12mV$$

So our assumptions are valid.

c. Assuming $Pr_{(IN=0)}$= 0.3, what is the static power dissipation of this circuit?

Solution

There is static power dissipation when both transistors are on. This happens when V_{IN}=1. Then the static power dissipation is given by:

$$P_{static} = P_{in=1}V_{DD}I_D$$

$$P_{static} = (1-0.3)2.5\left(\frac{115uA}{V^2}\frac{2}{1}\left(0.4\cdot 0.63-\frac{0.63^2}{2}\right)\right)$$

$$P_{static} = 21.55uW$$

8. [M, None, 3.3.3] An NMOS transistor is used to charge a large capacitor, as shown in Figure 5.6.

a. Determine the t_{pLH} of this circuit, assuming an ideal step from 0 to 2.5V at the input node.

Solutions

To determine the rise time, an average current has to be calculated between the start of the transistion with V_O=0V and midpoint of the transition.

At the start of the transistion: V_O=V_{OL}=0V, M1 is velocity saturated and I_{Dsat}=1.46mA. To find the votlage swing, V_{OH} must be calculated using the body effect:

$$V_{gs} = 2.5V - V_{OH} = V_{tn} + \gamma(\sqrt{|0.6+V_{OH}|}-\sqrt{0.6})$$

V_{OH}=1.76V. The midpoint is thus,

$$\frac{V_{OH}-V_{OL}}{2} = 0.88V$$

and the threshold voltage at the midpoint is: $V_T(V_{sb}=0.88V)$=0.607V.

Using this threshold voltage, V_{GT}=1.013V, V_{DS}=1.62V, and V_{DSat}=0.63V, thus, the transistor M1 is still velocity saturated, giving I_{DSat}=49.17mA.

Finding the average current between V_0= 0V and V_0= 0.88V gives: $I_{average}$=0.756mA.

$$t_p = \frac{C_L\Delta V}{I_{average}} = \frac{5pF\times 0.88V}{0.756mA} = 5.82n\sec$$

b. Assume that a resistor R_S of 5 kΩ is used to discharge the capacitance to ground. Determine t_{pHL}.

Solution

t_{pLH}=0.69*$R_L C_L$=0.69*5kΩ*5pF=17.25ns

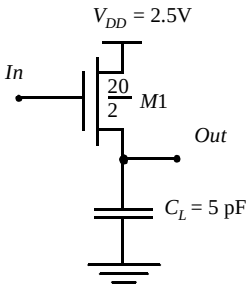


Figure 5.6 Circuit diagram with annotated *W/L* ratios

c. Determine how much energy is taken from the supply during the charging of the capacitor. How much of this is dissipated in M1. How much is dissipated in the pull-down resistance during discharge? How does this change when R_S is reduced to 1 kΩ.

Solution

$\Delta Q_{VDD}=C_L\Delta V=5pF*1.76V=8.8pC$

$\Delta E_{VDD}=\Delta Q_{VDD}*V_{dd}=8.8pC*2.5V=22pC$

Half the energy is dissipated in the transistor M1, while the other half is dissipated in the restistor R_s. The energy dissipated is independent of R_s.

d. The NMOS transistor is replaced by a PMOS device, sized so that k_p is equal to the k_n of the original NMOS. Will the resulting structure be faster? Explain why or why not.

Solution

If a PMOS device replaces the NMOS device, body effect will not exist and the PMOS device will be faster.

9. The circuit in Figure 5.7 is known as the *source follower* configuration. It achieves a DC level shift between the input and the output. The value of this shift is determined by the current I_0. Assume x_d=0, γ=0.4, $2|\phi_f|$=0.6V, V_{T0}=0.43V, k_n'=115μA/V^2 and λ=0.

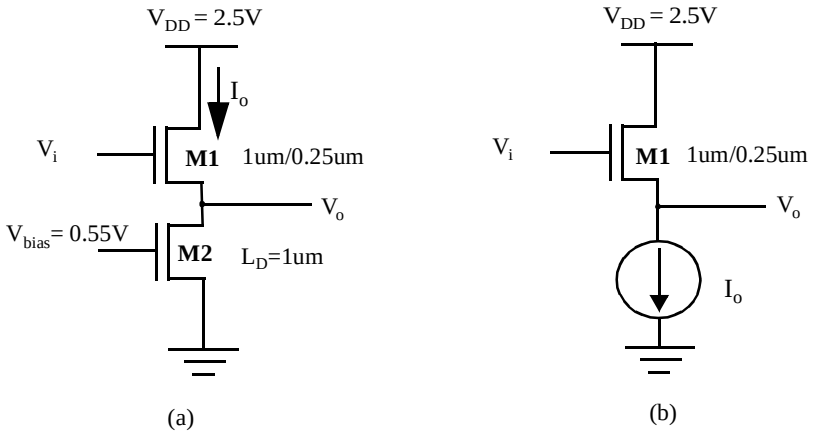


Figure 5.7 NMOS source follower configuration

a. Suppose we want the nominal level shift between V_i and V_o to be 0.6V in the circuit in Figure 5.7 (a). Neglecting the backgate effect, calculate the width of M2 to provide this level shift (Hint: first relate V_i to V_o in terms of I_o).

Solution

The level shift of 0.6V tells us that V_{GS1}=0.6V so V_{GT1}=0.17V. This means that **M1** must be in the saturation region (not velocity saturated). Thus,

$$\frac{k'_n \cdot \frac{W}{L}}{2} \cdot (V_{GS} - V_T)^2 = I_D \text{, and } I_D = 6.647\,\mu\text{A}.$$

For **M2**, V_{GT}=0.12, so **M2** is also in the saturation region (not velocity saturated). Using the same equation as above and solving for W/L gives **W/L = 8.**

b. Now assume that an ideal current source replaces M2 (Figure 5.7 (b)). The NMOS transistor M1 experiences a shift in V_T due to the backgate effect. Find V_T as a function of V_o for V_o ranging from 0 to 2.5V with 0.5V intervals. Plot V_T vs. V_o

Solution

The threshold voltage equation provides the relation that we need:

$$V_T = V_{T0} + \gamma \cdot (\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}) = V_{T0} + \gamma \cdot (\sqrt{|2\phi_F| + V_o} - \sqrt{|2\phi_F|}) .$$

See the graph at the end of this problem.

c. Plot V_o vs. V_i as V_o varies from 0 to 2.5V with 0.5 V intervals. Plot two curves: one neglecting the body effect and one accounting for it. How does the body effect influence the operation of the level converter?

Solution

To plot V_o versus V_i, we need to relate V_o to V_i. We can do this by solving the current equation (**M1** should remain in the same region to first order because V_{GT} will remain roughly constant to maintain the correct drain current) for V_i:

$$V_i = V_o + V_T + \sqrt{\frac{2I_D}{k'_n \cdot \frac{W}{L}}} .$$

d. At V_o(with body effect) = 2.5V, find V_o(ideal) and thus determine the maximum error introduced by the body effect.

Solution

The maximum error occurs at the highest V_{SB}. At Vo = 2.5, the error is 3.4944-3.1=**0.3944** V.

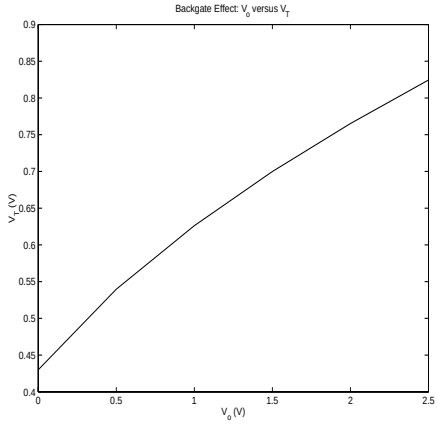


Figure for part (b)

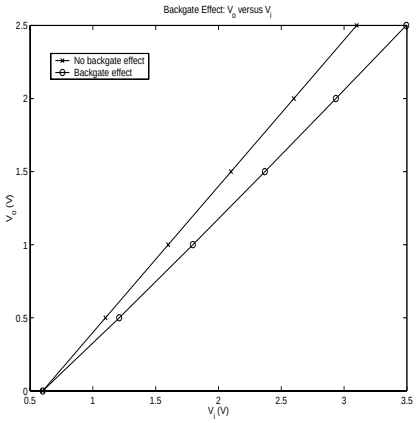


Figure for part (c)

10. For this problem assume:

V_{DD} = 2.5V, W_P/L = 1.25/0.25, W_N/L = 0.375/0.25, L=L_{eff} =0.25μm (i.e. x_d= 0μm), C_L=$C_{inv\text{-}gate}$, k_n' = 115μA/V^2, k_p'= -30μA/V^2, V_{tn0} = | V_{tp0} | = 0.4V, λ = 0V^{-1}, γ = 0.4, 2|ϕ_f|=0.6V, and t_{ox} = 58A. Use the HSPICE model parameters for parasitic capacitance given below (i.e. C_{gd0}, C_j, C_{jsw}), and assume that V_{SB}=0V for all problems except part **(e)**.

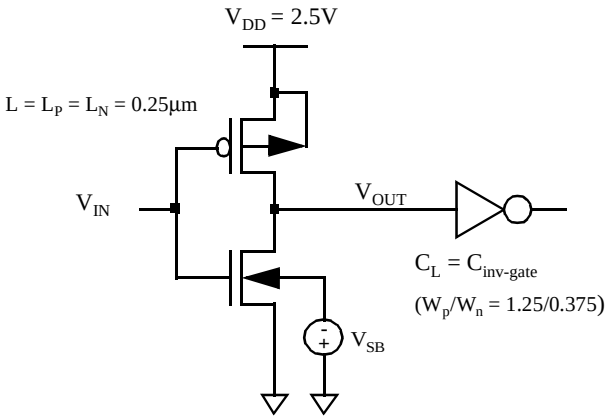


Figure 5.8 CMOS inverter with capacitive

Parasitic Capacitance Parameters (F/m)##
NMOS: CGDO=3.11x10^{-10}, CGSO=3.11x10^{-10}, CJ=2.02x10^{-3}, CJSW=2.75x10^{-10}
PMOS: CGDO=2.68x10^{-10}, CGSO=2.68x10^{-10}, CJ=1.93x10^{-3}, CJSW=2.23x10^{-10}

a. What is the V_m for this inverter?

Solution

Assume that Vm is around midrail (1.25V). That means that the NMOS is velocity saturated and the PMOS is saturated. To find Vm, we set the sum of the currents at Vout equal to 0 using the correct equation for each device:

$$k_n \cdot V_{DSATn} \cdot \left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + k_p \cdot 0.5 \cdot (V_M - V_{DD} - V_{Tp})^2 = 0 .$$

Plug in numbers:

$$172.5 \cdot 0.6 \cdot (V_M - 0.4 - 0.315) + (-150) \cdot 0.5 \cdot (V_M - 2.5 - (-0.4))^2 = 0$$

$$103.5 V_M - 74 - \left(-75 \cdot \left(V_M{}^2 - 4.2 V_M + 4.41\right)\right) = 0 .$$

Solving this quadratic gives $\boldsymbol{V_M = 1.245\ V}$.

b. What is the effective load capacitance C_{Leff} of this inverter? (Include parasitic capacitance, refer to the text for K_{eq} and m.) **Hint:** You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, λ = 0.125 μm, and the source/drain extensions are 5λ for the PMOS; for the NMOS the source/drain contact regions are 5λx5λ.

Solution

The calculation of the lumped load capacitance follows the format presented in the lecture notes. The only difference is the dimensions of the devices.
$C_{Leff} = C_L + C_{parasitic} = C_{g3} + C_{g4} + C_{db1} + C_{db2} + C_{gd1} + C_{gd2}$.
$\mathbf{C_{g3}} = (C_{GD0n} + C_{GSOn})W_n + C_{ox}W_nL = 2(3.11e\text{-}10)(0.375e\text{-}6) + 6e\text{-}15(0.375)(0.25) = \mathbf{0.796fF}$
$\mathbf{C_{g4}} = (C_{GD0p} + C_{GSOp})W_p + C_{ox}W_pL = 2(2.68e\text{-}10)(1.25e\text{-}6) + 6e\text{-}15(1.25)(0.25) = \mathbf{2.545fF}$
$\mathbf{C_{db1}} = K_{eqn}(AD_n)C_j + K_{eqswn}(PD_n)C_{jsw}$. Need to do this calculation for both transitions and average the results. The K_{eq} values are already calculated in the text.
$AD_p=AS_p=1.25um*0.625um=0.78125um^2$ and
$AD_n=AS_n=0.125*0.375+0.625^2=0.4375um^2$.
$PD_p=PS_p=2*0.625um+1.25um=2.5um$ and
$PD_n=PS_n=5*0.125um*3+(2+1+1)*0.125um=2.375um$.
(0.57*0.4375*2 + 0.61*2.375*0.28) = 0.904fF for HL transition
(0.79*0.4375*2 + 0.81*2.375*0.28) = 1.23fF for LH. Average $\mathbf{C_{db1}=1.067fF}$.
$\mathbf{C_{db2}} = K_{eqp}(AD_p)C_j + K_{eqswp}(PD_p)C_{jsw}$.
(0.79*0.78125*1.9 + 0.86*2.5*0.22) = 1.65fF for HL transition
(0.59*0.78125*1.9 + 0.7*2.5*0.22) = 1.26fF for LH. Average $\mathbf{C_{db2}=1.455fF}$.
$\mathbf{C_{gd1}} = 2C_{GD0n}W_n = 2*3.11e\text{-}10*0.375e\text{-}6 = \mathbf{0.233fF}$.
$\mathbf{C_{gd2}} = 2C_{GD0p}W_p = 2*2.68e\text{-}10*1.25e\text{-}6 = \mathbf{0.67fF}$.
$\mathbf{C_L}$ = sum = **6.767fF**. Note - since the problem states that x_d=0, it is ok if you neglected the last two parasitic capacitances. We intended for them to be included, though.

c. Calculate t_{PHL}, t_{PLH} assuming the result of (b) is 'C_{Leff} = 6.5fF'. (Assume an ideal step input, i.e. t_{rise}=t_{fall}=0. Do this part by computing the average current used to charge/discharge C_{Leff}.)

Solution

We can estimate the propagation delay using the approximation $\Delta t = \Delta Q/I$, where $\Delta Q = C_{Leff}V_{DD}$ and I is the average current used to charge/discharge C_{Leff}. During the high-to-low transition C_{Leff} is discharged through the NMOS transistor so $I = I_{avgN}$. During the low-to-high transition C_{Leff} is charged through the PMOS transistor so $I = I_{avgP}$. In summary:

$$t_{delay} \cong \frac{V_{DD} \cdot C_{Leff}}{2 \cdot I_{avg}}, \text{ where}$$

$$I_{avgN} = \frac{I_{ds}(V_o = 0) + I_{ds}\left(V_o = \frac{V_{DD}}{2}\right)}{2}, I_{avgP} = \frac{I_{ds}(V_o = V_{DD}) + I_{ds}\left(V_o = \frac{V_{DD}}{2}\right)}{2}$$

Table 1 shows corresponding values for I_{avgN}, I_{avgP}, t_{PLH}, and t_{PHL}. NOTE- This solution

	V_o (V)	Operation Mode	I_{ds} (mA)	I_{avg} (mA)	Prop Delay (ps)
for t_{PLH}	0	PMOS vel sat.	0.300	0.285	28.5
	1.25	PMOS vel sat	0.270		
for t_{PHL}	2.5	NMOS vel sat.	0.209	0.202	40.0
	1.25	NMOS vel sat	0.195		

Table 1: Average currents and propagation delays for Problem 4(c).

included channel length modulation, but it is ok if your solution did not (see problem assumptions).

d. Find (W_p/W_n) such that $t_{PHL} = t_{PLH}$.

Solution

One way to do this is to solve the current average equations for W_p/W_n after setting the propagation delays equal to one another. A much easier method is to sweep the widths in HSPICE. The HSPICE sim shows that **W_p/W_n =2.6** gives equal rise and fall times.

e. Suppose we increase the width of the transistors to reduce the t_{PHL}, t_{PLH}. Do we get a proportional decrease in the delay times? Justify your answer.

Solution

The propagation delays DO NOT decrease in proportion to the widths because of self-loading effects. As the device size increases, its parasitic capacitances increase as well. In this problem, increasing device size increases both average current and $C_{Leff.}$

f. Suppose V_{SB} = 1V, what is the value of V_{tn}, V_{tp}, V_m? How does this qualitatively affect C_{Leff}?

Solution

V_{tp} = V_{tp0} = **-0.4V.**

V_{tn} = $0.4 + \gamma \cdot (\sqrt{2\phi_F + 1} - \sqrt{|2\phi_F|})$ = **0.596 V**.

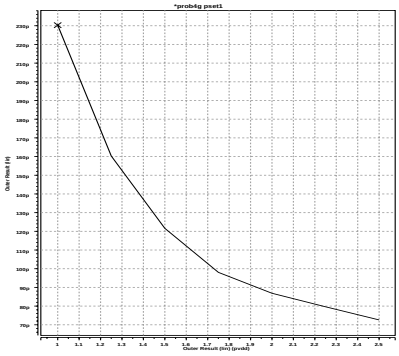
Using the equation for part a) and plugging in the new value of V_{tn} gives: **V_M = 1.35V** The increased V_{sb} will increase the depletion region and lower the junction capacitance, lowering C_{Leff}.

11. Using Hspice answer the following questions.

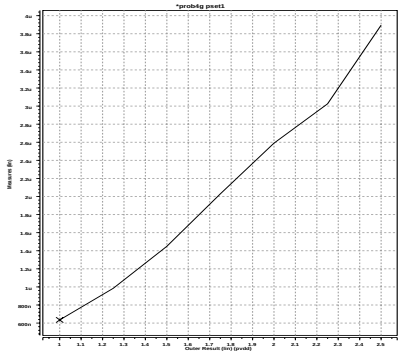
a. Simulate the circuit in Problem 10 and measure t_P and the average power for input V_{in}: pulse(0 V_{DD} 5n 0.1n 0.1n 9n 20n), as V_{DD} varies from 1V - 2.5V with a 0.25V interval. [t_P = (t_{PHL} + t_{PLH}) / 2]. Using this data, plot 't_P vs. V_{DD}', and 'Power vs. V_{DD}'.

Specify AS, AD, PS, PD in your spice deck, and manually add C_L = 6.5fF. Set V_{SB} = 0V for this problem.

Solution



Delay vs VDD (part a)



Power vs VDD (part a)

b. For Vdd equal to 2.5V determine the maximum fan-out of identical inverters this gate can drive before its delay becomes larger than 2 ns.

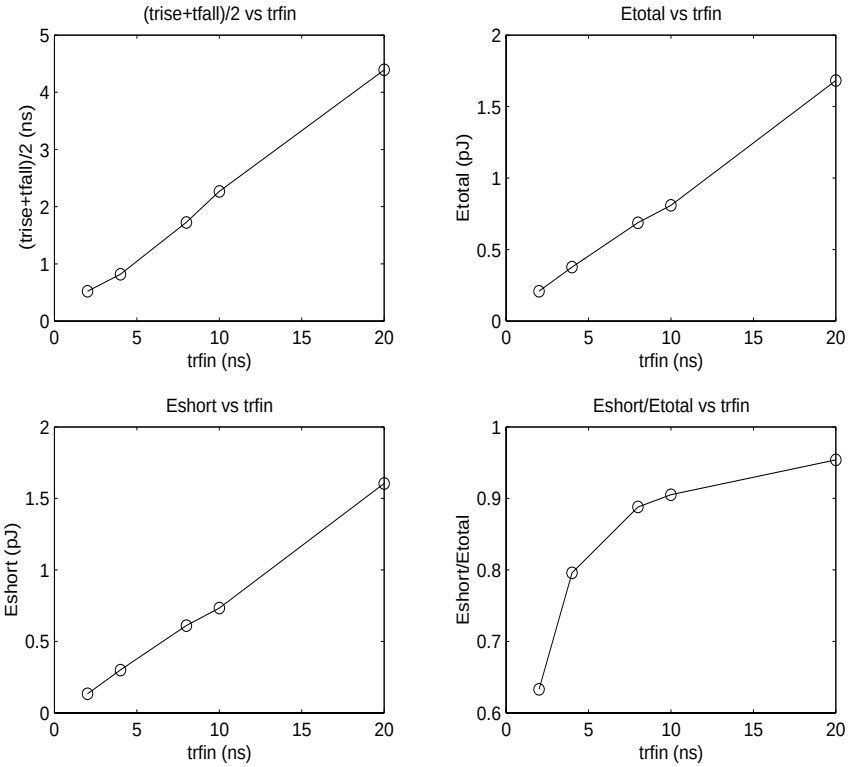
Solution

The maximum number of identical inverters that this gate can drive before the propagation delay exceeds 2ns is 115 inverters.

c. Simulate the same circuit for a set of 'pulse' inputs with rise and fall times of $t_{in\_rise,fall}$ =1ns, 2ns, 5ns, 10ns, 20ns. For each input, measure (1) the rise and fall times t_{out_rise} and t_{out_fall} of the inverter output, (2) the total energy lost E_{total}, and (3) the energy lost due to short circuit current E_{short}.

Using this data, prepare a plot of (1) $(t_{out\_rise}+t_{out\_fall})/2$ vs. $t_{in\_rise,fall}$, (2) E_{total} vs. $t_{in\_rise,fall}$, (3) E_{short} vs. $t_{in\_rise,fall}$ and (4) E_{short}/E_{total} vs. $t_{in\_rise,fall.}$

Solution



d. Provide simple explanations for:

(i) Why the slope for (1) is less than 1?

(ii) Why E_{short} increases with $t_{in\_rise,fall}$?

(iii) Why E_{total} increases with $t_{in\_rise,fall}$?

Solution

i) The slope is less than 1 because of the regenerative property of the inverter. The high gain around the switching point causes the output to change faster than the inputs.

ii) The amount of time for which both devices are on simultaneously increases.

iii) Total energy increases because the short circuit energy begins to dominate, and the short circuit increases as the rise/fall time increases.

12. Consider the low swing driver of Figure 5.9:

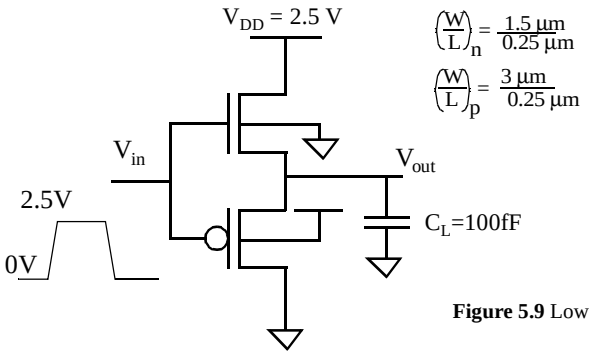


Figure 5.9 Low Swing Driver

a. What is the voltage swing on the output node (V_{out})? Assume γ=0.

Solution

The range will be from 0.4 V to 2.07 V, since the PMOS is a weak pull down device and the NMOS is a weak pull up device.

b. Estimate (i) the energy drawn from the supply and (ii) energy dissipated for a 0V to 2.5V transition at the input. Assume that the rise and fall times at the input are 0. Repeat the analysis for a 2.5V to 0V transition at the input.

Solution

For a 0 V to 2.5 V transition on the input, the energy drawn from the power supply is:

$$E_{SUPPLY} = \int i_{DD} V_{DD} dt = V_{DD}\Delta Q = CV_{DD}((V_{DD} - V_{tn}) - |V_{tp}|)$$

The PMOS will be in cutoff and the energy dissipated in the NMOS will be:

$$E_{DISSIPATED} = E_{SUPPLY} - \Delta E_{CAP}$$

$$E_{DISSIPATED} = CV_{DD}((V_{DD} - V_{tn}) - |V_{tp}|) - C\left[\left(\frac{V_{DD} - V_{tn}}{2}\right)^2 - \left(\frac{|V_{tp}|}{2}\right)^2\right]$$

For a 2.5 V to 0 V transition on the input, the NMOS will be in cutoff and no energy will be drawn from the power supply. The energy dissipated in the PMOS device will be equal to:

$$E = C\left[\left(\frac{V_{DD} - V_{tn}}{2}\right)^2 - \left(\frac{|V_{tp}|}{2}\right)^2\right]$$

c. Compute t_{pLH} (i.e. the time to transition from V_{OL} to $(V_{OH} + V_{OL})/2$). Assume the input rise time to be 0. V_{OL} is the output voltage with the input at 0V and V_{OH} is the output voltage with the input at 2.5V.

Solution

When the input is high and the capacitor charges, the PMOS device is in cutoff and the NMOS is velocity saturated for the duration of the charging. The total voltage range is 0.4 V to 2.07 V, so the midpoint is 1.24 V. We can use the average current method to approximate t_{plh}. For the velocity saturated NMOS:

$$I = \left(\frac{\mu_n C_{ox} W}{L}\right) V_{DSATN}\left(V_{GS} - V_{tn} - \frac{V_{DSATN}}{2}\right)(1 + \lambda V_{DS})$$

Solving for the current at V=0.4 V and V=1.24 V and averaging yields an average current of 404 uA. Then:

$$t_{plh} = \frac{C\Delta V}{I_{avg}} = \frac{(100fF)(1.24V - 0.4V)}{404uA} = 208ps$$

d. Compute V_{OH} taking into account body effect. Assume $\gamma = 0.5V^{1/2}$ for both the NMOS and the PMOS.

Solution

The PMOS will be deep in cutoff when V_{out} approaches V_{OH}. Therefore, we consider only the NMOS. We can express the equation for threshold voltage numerically as follows:

$$V_{tn} = 0.43 + 0.5(\sqrt{(0.6 + 2.5 - V_{tn})} - \sqrt{0.6})$$

This is an equation in one variable, so it may be solved numerically to find that V_{tn}=0.8 V.

13. Consider the following low swing driver consisting of NMOS devices M1 and M2. Assume an NWELL implementation. Assume that the inputs IN and $\overline{IN}$ have a 0V to 2.5V swing and that $V_{\overline{IN}}$ = 0V when $V_{\overline{IN}}$ = 2.5V and vice-versa. Also assume that there is no skew between IN and $\overline{IN}$ (i.e., the inverter delay to derive $\overline{IN}$ from IN is zero).

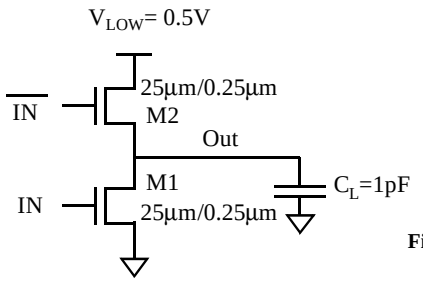


Figure 5.10 Low Swing Driver

a. To what voltage is the bulk terminal of M2 connected?

Solution

In an NWELL process, the bulk terminal of an NMOS must be connected to ground.

b. What is the voltage swing on the output node as the inputs swing from 0V to 2.5V. Show the low value and the high value.

Solution

Because the supply voltage is more than a threshold voltage lower than the gate drive voltage, the output range will not be limited. Therefore the low value is 0 V and the high value is 0.5 V.

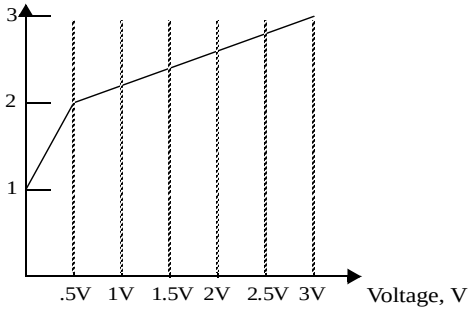
c. Assume that the inputs IN and $\overline{IN}$ have zero rise and fall times. Assume a zero skew between IN and $\overline{IN}$. Determine the low to high propagation delay for charging the output node measured from the the 50% point of the input to the 50% point of the output. Assume that the total load capacitance is 1pF, including the transistor parasitics.

Solution

The lower NMOS will be off during the low to high transition and the upper NMOS will be in the linear region throughout the transition from 0.0V to 0.25V. We will assume that the body effect is negligible, since the maximum value of V_{SB} is 0.25V. Use the average current method to find t_{plh}. Using the current equation for the linear region, the current when the capacitor is at 0V, is 10.8mA. When the capacitor reaches 0.25V, the current is 4.58mA. Threfore, the average current is 7.7mA.

$$t_{plh} = \frac{C\Delta V}{I_{avg}} = \frac{(1pF)(0.25V)}{7.7mA} = 32.5ps$$

d. Assume that, instead of the 1pF load, the low swing driver drives a non-linear capacitor, whose capacitance vs. voltage is plotted below. Compute the energy drawn from the low supply for charging up the load capacitor. Ignore the parasitic capacitance of the driver circuit itself.



Solution

The capacitor charges only from 0 V to 0.5 V, so only the first segment of the graph should be considered. The total energy drawn from the supply is:

$$E = V_{DD}\int I(t)dt = Q_{total}V_{DD}$$

The total charge required to charge the capacitor is:

$$Q = \int_0^{0.5} C(V)dV = 1pF\int_0^{0.5}(1+2V)dV = 0.75pC$$

Therefore, since the the E=QV, the total energy drawn from the supply is 0.375 pJ.

14. The inverter below operates with V_{DD}=0.4V and is composed of |Vt| = 0.5V devices. The devices have identical I_0 and n.

a. Calculate the switching threshold (V_M) of this inverter.

Solution

The subthreshold I-V relation is given by $I_D = I_o e^{(V_{GS}-V_t)/(nV_T)}(1+\lambda V_{DS})$, assuming V_{DS} > 50mV. To calculate the switching voltage, we need to find where V_{in}=V_{out} occurs. So equating the absolute values of the currents for the two transistors we get:

$$I_o e^{V_{in}/(nV_T)}(1+\lambda_n V_{out}) = I_o e^{(V_{DD}-V_{in})/(nV_T)}(1+\lambda_p(V_{DD}-V_{out}))$$

Considering V_{in}=V_{out} and doing some cancellations we get:

$$\ln[(1+\lambda_n V_{in})/(1+\lambda_p(V_{in}-V_{DD}))] = 1/((n\cdot V_T)(V_{DD}-V_{in}-V_{in}))$$

after massaging the last equation we have:

$$V_{DD}/2 - nV_T/2 \cdot \ln[(1+\lambda_n V_{in})/(1+\lambda_p(V_{DD}-V_{in}))] = V_{in}$$

Iterating this expression with V_{DD}=0.4V, V_T=26mV, λ_n=0.06, λ_p=0.1 and n=1.5 we get V_{in}=0.2V. So we have a switching threshold of V_{DD}/2=0.2V.

b. Calculate V_{IL} and V_{IH} of the inverter.

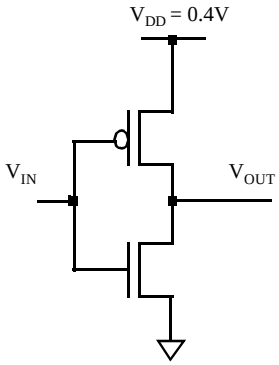


Figure 5.11 Inverter in Weak Inversion Regime

Solution

To calculate the noise margins we need to calculate the slope of the VTC at V_M=V_{DD}/2. Equating the currents we get:

$$I_{o'}e^{V_{in}/(nV_T)}(1+\lambda_n V_{out}) = I_{o'}e^{(V_{DD}-V_{out})/(nV_T)}(1+\lambda_p(V_{DD}-V_{out}))$$

and cancelling out $I_{o'}$ and differentiating both sides with respect to V_{in} we get:

$$\frac{\partial}{\partial V_{in}}(e^{V_{in}/(nV_T)}(1+\lambda_n V_{out})) = \frac{\partial}{\partial V_{in}}e^{(V_{in}-V_{DD})/(nV_T)}(1+\lambda_p(V_{out}-V_{DD}))$$

$$e^{V_{in}/(nV_T)}(1+\lambda_n V_{out})/nV_T + e^{V_{in}/(nV_T)}\lambda_n\frac{\partial V_{out}}{\partial V_{in}} =$$

$$= -e^{(V_{DD}-V_{in})/(nV_T)}(1+\lambda_p(V_{DD}-V_{out}))/nV_T - e^{(V_{DD}-V_{in})/(nV_T)}\lambda_p\frac{\partial V_{out}}{\partial V_{in}}$$

manipulating this expression we get:

$$(e^{(V_{DD}-V_{in})/(nV_T)}\lambda_p + e^{V_{in}/(nV_T)}\lambda_n)\frac{\partial V_{out}}{\partial V_{in}} =$$

$$= e^{V_{in}/(nV_T)}(1+\lambda_n V_{out})/nV_T + e^{(V_{DD}-V_{in})/(nV_T)}(1+\lambda_p(V_{DD}-V_{out}))/nV_T$$

plugging in V_{out}=V_{in}=V_{DD}/2 we reach:

$$-e^{(V_{DD}/2)/(nV_T)}(\lambda_p+\lambda_n)\frac{\partial V_{out}}{\partial V_{in}} = e^{(V_{DD}/2)/(nV_T)}(2+(\lambda_p+\lambda_n)V_{DD}/2)/(nV_T)$$

Finally:

$$\left.\frac{\partial V_{out}}{\partial V_{in}}\right|_{Vin\,=\,Vout\,=\,V_{DD}/2} = -(2+(\lambda_p+\lambda_n)V_{DD}/2)/(nV_T)/(\lambda_p+\lambda_n)$$

Using the values V_{DD}=0.4V, V_T=26mV, λ_n=0.06, λ_p=0.1 and n=1.5 we obtain:

$$g = \frac{\partial V_{out}}{\partial V_{in}} = -325.6$$

This value is much more that we would expect from an MOS inverter (which has g~-30). However we should keep in mind that in the subthreshold regime MOS devices behave essentially as bipolar devices and can yield such values of gain.

We know that $V_{IL}=V_M+(V_{DD}-V_M)/g$ and $V_{IH}=V_M-V_M/g$ from the text (eq 5.7). Using these equations and the results that we got we have: V_{IL}=0.1994V and V_{IH}=0.2006V.

Also $NM_H=NM_L$=0.1994V

15. Sizing a chain of inverters.

a. In order to drive a large capacitance (C_L = 20 pF) from a minimum size gate (with input capacitance C_i = 10fF), you decide to introduce a two-staged buffer as shown in Figure 5.12. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay.

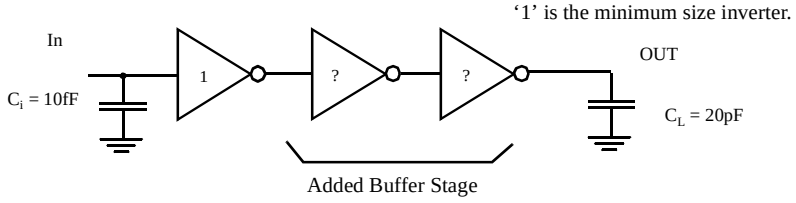


Figure 5.12 Buffer insertion for driving large loads.

Solution

Minimum delay occurs when the delay through each buffer is the same. This can be achieved by sizing the buffer as f, f^2, respectively
where $f = \sqrt[N]{F} = \sqrt[3]{2000} = 12.6$, so ($\gamma$=0)

$$t_p = Nt_{p0}(1+f/\gamma) = 3\cdot 70ps\cdot(1+12.6) = 2.8ns$$

b. If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?

Solution

From the text, we know that the minimum delay occurs when f = e. Therefore,

$$N = \frac{\ln(2000)}{\ln(f)} = 7.6$$

$$f = e^{\frac{\ln(2000)}{7}} = 2.96$$

$$t_{delay} = 7 \times 3.96 \times 70\text{ps} = 1.9ns$$

c. Describe the advantages and disadvantages of the methods shown in (a) and (b).

Solution

Solution (b) is faster but it consumes much more area than (a).

d. Determine a closed form expression for the power consumption in the circuit. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V and an activity factor of 1?

Solution

The power consumption is determined as follows

$$P = C_{tot}V_{dd}^2 \frac{1}{T}\alpha$$

$$P = C_iV_{dd}^2\frac{1}{T}\alpha\sum_{k=0}^{3} f^k = C_iV_{dd}^2\frac{1}{T}\alpha\left(\frac{f^4-1}{f-1}\right) = 136\left(\frac{1}{T}\right)\text{ pWatts}$$

16. [M, None, 3.3.5] Consider scaling a CMOS technology by S > 1. In order to maintain compatibility with existing system components, you decide to use constant voltage scaling.

a. In traditional constant voltage scaling, transistor widths scale inversely with S, W$\propto$1/S. To avoid the power increases associated with constant voltage scaling, however, you decide to change the scaling factor for *W*. What should this new scaling factor be to maintain approximately constant power. Assume long-channel devices (i.e., neglect velocity saturation).

Solution

We know that: $P \propto CV_{DD}^2 f$ and $f \propto \frac{1}{t_P} \propto \frac{I_{Dsat}}{CV_{DD}}$, so

$$P \propto I_{Dsat}V \propto k'\frac{W}{L}(V-V_t)^2V \propto (s)\frac{(W)}{\left(\frac{1}{s}\right)}$$

To keep power constant we need to scale $W \propto \frac{1}{s^2}$. which means redesigning gates with W a factor of 1/s smaller.

b. How does delay scale under this new methodology?

Solution

$$t_p \propto \frac{CV}{k'\frac{W}{L}V^2} \propto \frac{WL\frac{\varepsilon}{t}}{k'\frac{W}{L}V} \propto \frac{\left(\frac{1}{s^2}\right)\left(\frac{1}{s}\right)\frac{1}{1/s}}{s\frac{1/s^2}{1/s}}$$

so $t_P \propto 1/s^2$.

c. Assuming short-channel devices (i.e., velocity saturation), how would transistor widths have to scale to maintain the constant power requirement?

Solution

$P \propto I_{SAT} V_{DD} \propto V_{DD} W C_{ox} (V_{gs} - V_t) \upsilon_{max} \propto W(s)$, so $W \propto \frac{1}{s}$.
This means that no changes need to be made.

DESIGN PROBLEM

Using the 0.25 μm CMOS introduced in Chapter 2, design a static CMOS inverter that meets the following requirements:

1. Matched pull-up and pull-down times (i.e., $t_{pHL} = t_{pLH}$).
2. $t_p = 5$ nsec (± 0.1 nsec).

The load capacitance connected to the output is equal to 4 pF. Notice that this capacitance is substantially larger than the internal capacitances of the gate.

Determine the W and L of the transistors. To reduce the parasitics, use minimal lengths ($L = 0.25$ μm) for all transistors. Verify and optimize the design using SPICE after proposing a first design using manual computations. Compute also the energy consumed per transition. If you have a layout editor (such as MAGIC) available, perform the physical design, extract the real circuit parameters, and compare the simulated results with the ones obtained earlier.