BIRZEIT UNIVERSITY

Faculty of Engineering and Technology
Department of Electrical and Computer Engineering

Course Information	
Course Title	**Digital Integrated Circuits**
Course Number	ENCS 333
Prerequisites	ENEE 233
Semester	Second Semester 2018/2019
Instructors	Dr. Khader Mohammad khamadawwad@birzeit.edu
Office Hours	See Ritaj for the office hours.
Required Reading	1. Handouts /lectures notes 2. Rabaey, Jan, Anantha Chandrakasan, and Bora Nikolic. *Digital Integrated Circuits: A Design Perspective*. 2nd ed. Upper Saddle River, NJ: Prentice Hall, 2002. ISBN: 0130909963. 3. Analysis and design of Digital Integrated Circuits: David Hodges et. al. 4. Principles of CMOS VLSI Design by: N. Weste and K. Eshraghian

Course Summary and Objectives

- In this course, we will study the fundamental structures of digital integrated circuit systems. We start by looking at the MOS transistors (n-channel and p-channel) and the ways in which we can use them to create the most basic structure—the digital switch. We can proceed to build a range of VLSI structures from this switch, including NAND/NOR gates, Multiplexers, Latches and Registers. Continuing in a bottom-up fashion, we can examine the structure of more complex VLSI design components (those at Digital Logic and Register Transfer levels of abstraction) using these primitives.
- We will also learn about the processes associated with fabricating CMOS devices. Using CMOS as our technology, we examine the circuit level design rules associated with circuit geometries and their layout according to a set of process technology-specific design rules. We also look at factors affecting design: capacitance, resistance, clocking, delay and power. Part of the course will tackle the issue of reliability and how an integrated circuit is qualified to meet user requirements and environmental issues.
- Students at the end of the course should be able to:
  - Use mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits, including logic components, and it's interconnect.
  - Create models of moderately sized CMOS circuits that realize specified digital functions.
  - Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
  - Have an understanding of the characteristics of CMOS circuit construction

ABET OUTCOMES

B: Ability to design and conduct experiments, analyze and interpret data,

C: Ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, sustainability political, ethical, health and safety, manufacturability, and

K: Ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

	Course topics and Schedule
Lectures	**Subject**
1	Introduction to Digital Integrated Circuits Design
2	Semiconductor material: pn-junction, NMOS, PMOS
3	IC Manufacturing and Design Metrics CMOS
4	Transistor Devices and Logic Design The CMOS inverter
5	Combinational logic structures
6	Sequential logic gates; Latches and Flip-Flops
7	Layout of an Inverter and basic gates
8	Parasitic Capacitance Estimation
9	Device modeling parameterization from I-V curves.
	Short Test
10	Arithmetic building blocks
11	Interconnect: R, L and C - Wire modeling
12	Timing
	Power dissipation;
13	SPICE Simulation Techniques (Project)
14	Memories and array structures
	Midterm
15	Clock Distribution
16	Supply and Threshold Voltage Scaling
17	Reliability and IC qualification process
18	Advanced Voltage Scaling Techniques
19	Power Reduction Through Switching Activity Reduction
20	CAD tools and algorithms

***The above order is not chronological. Other topics might be discussed as seen fit**

Assessment Policy		
Assessment Type	**Expected Due Date**	**Weight**
Short Exams//Quizzes	TBD	15%
Midterm Exam	TBD	30%
Projects/Assignments	TBD	20%
Final Exam	TBD	35%

ميثاق شرف الأمانة الأكاديمية

بموجب التسجيل في هذا المساق يلتزم الطالب باحترام أنظمة وقوانين الجامعة وخاصة تلك المتعلقة بالأمانة العلمية وعدم الغش. ويتحمل الطالب مسئولية ذاتية، أدبية وقانونية، عن المحافظة على الأمانة العلمية وذلك بالامتناع عن الغش في الامتحانات والوظائف والتقارير، وعدم السماح لغيره من الطلاب بأن ينقلوا عنه في الامتحانات والوظائف والتقارير.

يستوجب الغش أو محاولة الغش التوبيخ والإجراءات القانونية المنصوص عليها في تعليمات الأمانة الأكاديمية التي أقرها مجلس الجامعة، وتشمل ما يلي:

1. **العقوبة الأكاديمية: يقررها مدرس المساق وقد تصل إلى علامة رسوب في المساق.**
2. **العقوبة التأديبية: تقررها لجنة النظام في الكلية وقد تصل إلى الفصل المؤقت أو النهائي من الجامعة.**

بموجب تسجيلي في هذا المساق واستلامي لهذا الميثاق أتعهد أمام الله أن أحافظ على الأمانة الأكاديمية بأن أمتنع عن الغش، وأن لا أتسامح مع أي محاولة للغش من قِبل الآخرين.