جامعة بيرزيت

Computer Systems Engineering Department

Adlam Snwan
1091496

Integrated Circuits ENCS333

First Exam

Instructor: Dr. Wasel Ghanem

Question #1

Consider the following function $F = ((A.B + C).(D + E))'$ with static CMOS gates.
Assuming $R_{sqn} = 4R_{sqp}$:

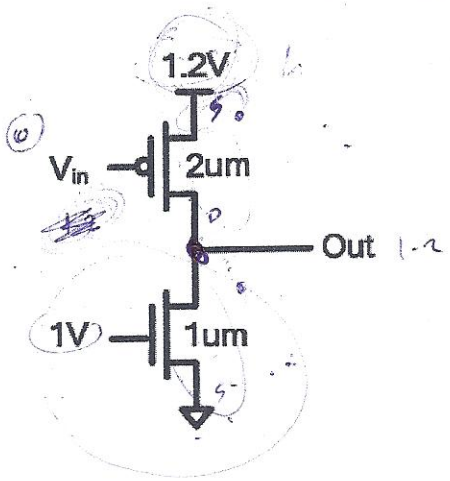
- Implement the function F.

- Sketch the Stick diagram for the above function and estimate the area.

-Size the gates so that the worst-case pull up resistance is equal to the worst-case pull down resistance.

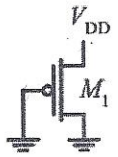
Question #2

(a) What value of *Vin* makes the drain current of the two transistors equal to each other, consider L=90nm.

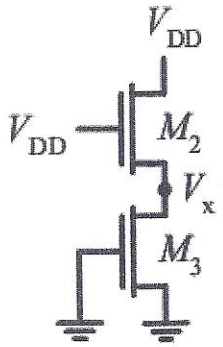


(b) Determine the region of operation (Off, Linear, Saturation, Velocity saturation) in the

following configurations. You may assume that all transistors are short-channel devices and have identical sizes, VDD= 2.5V



(a)

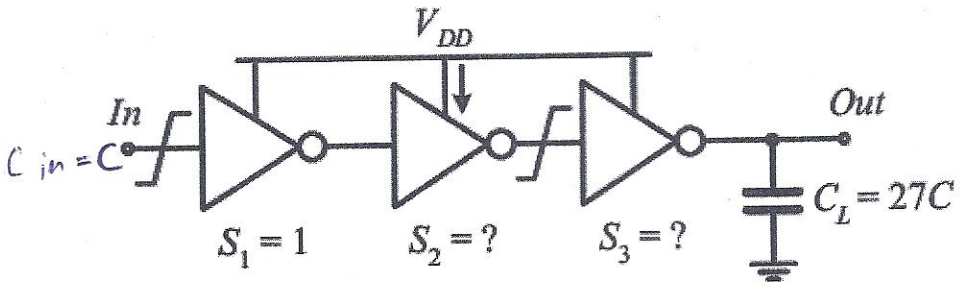


(b)

NMOS: V_{Tn} = 0.2V $k_n = 115\mu A/V^2$, $V_{DSATn} = 0.6V$, $\lambda = 0$, $\gamma = 0.4V^{1/2}$, $2\Phi_F = -0.6V$
PMOS: V_{Tp} = -0.2V $kp = -30\mu A/V^2$, $V_{DSATp} = -1V$, $\lambda = 0$, $\gamma = -0.4V^{1/2}$, $2\Phi_F = 0.6V$

Question #3

(a) Consider the following:



-For inverters in the figure above, pick the best sizing factor S2 and S3 to minimize propagation delay. What is the minimum delay in terms of tinv?

-What is the total energy drawn from the supply when the input switches from 0 to VDD?

-If the load is changed to $C_L = 3000C$, what is the optimum number of stages and best sizes for the inverters. What is the delay in this case?

(b) Explain briefly the main steps/processes used in fabrication of CMOS devices with schematics.