Digital Integrated Circuits ENCS 333

Instructor:

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What will you learn here?

- Introduction to digital integrated circuit design engineering
 - Key concepts needed to be a good digital IC designer
 - Design creativity
- Models that allow reasoning about circuit behavior
 - Allow analysis and optimization of the circuit's performance, power, cost, etc.
 - Understanding circuit behavior is key to making sure it will actually work
- □ Teach you how to make sure your circuit works
 - Do you want your transistor to be the one that screws up a 1 billion transistor chip?

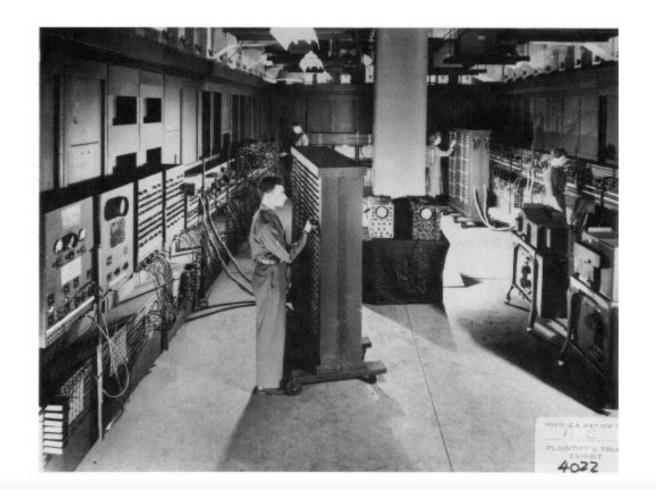
What will you learn?

- Understanding, designing, and optimizing digital circuits for various quality metrics:
 - Performance (speed)
 - Power dissipation
 - Cost
 - Reliability

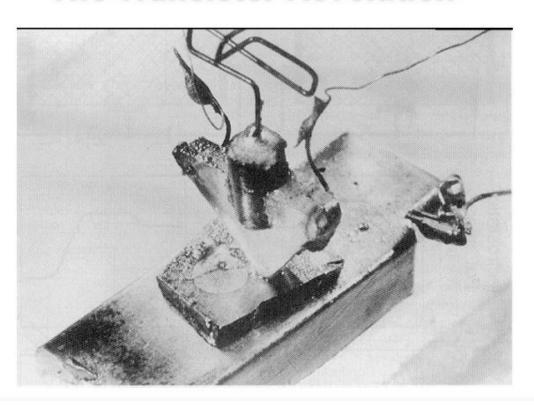
Introduction

- Digital Integrated Circuit Design: The Past, The Present and The Future
 - What made Digital IC design what it is today
 - Why is designing digital ICs different today than it was before?
 - Will it change in the future?

ENIAC - The First Electronic Computer (1946)



The Transistor Revolution

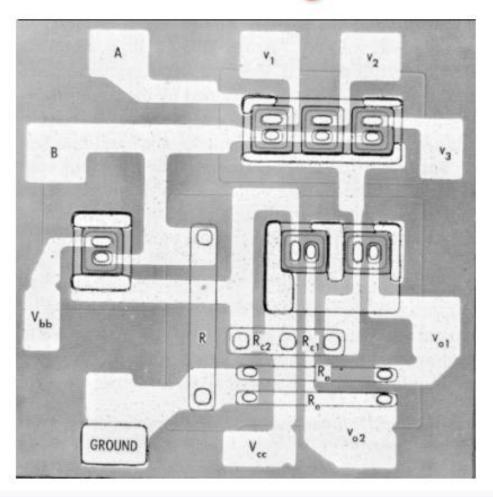


First transistor Bell Labs, 1948



John Bardeen, William Shockley and Walter Brattain at Bell Labs, 1948.

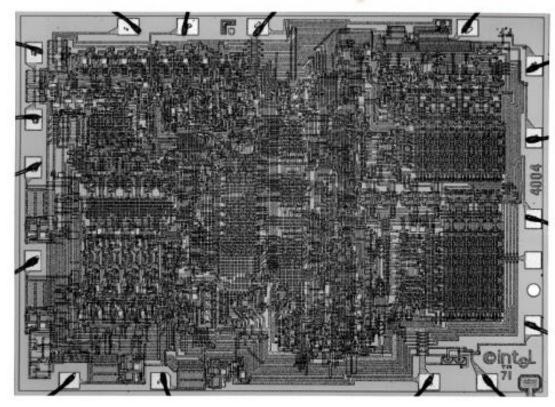
The First Integrated Circuits



Bipolar logic 1960's

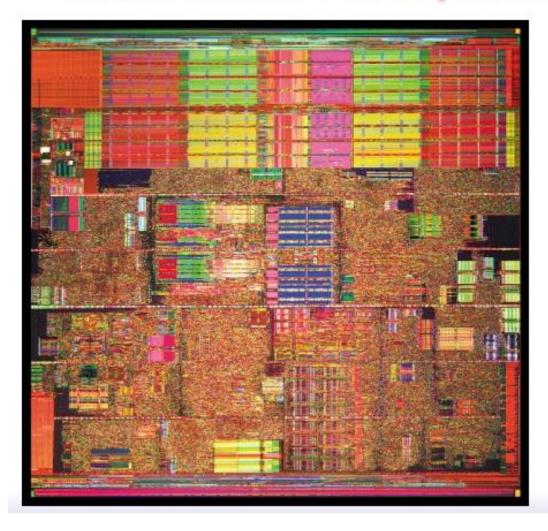
ECL 3-input Gate Motorola 1966

Intel 4004 Microprocessor



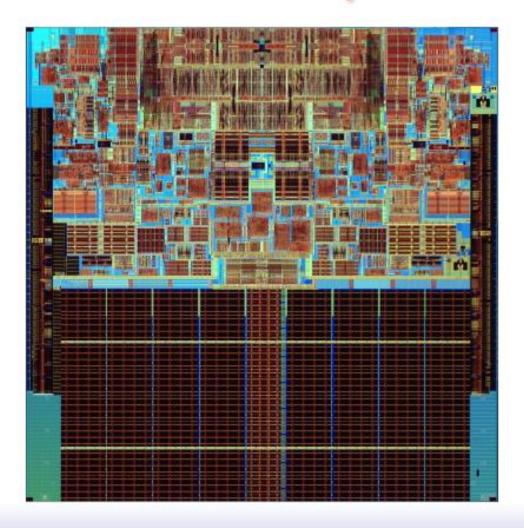
Intel, 1971. 2,300 transistors (12mm²) 740 KHz operation (10µm PMOS technology)

Intel Pentium 4 Microprocessor



Intel, 2005. 125,000,000 transistors (112mm²) 3.8 GHz operation (90nm CMOS technology)

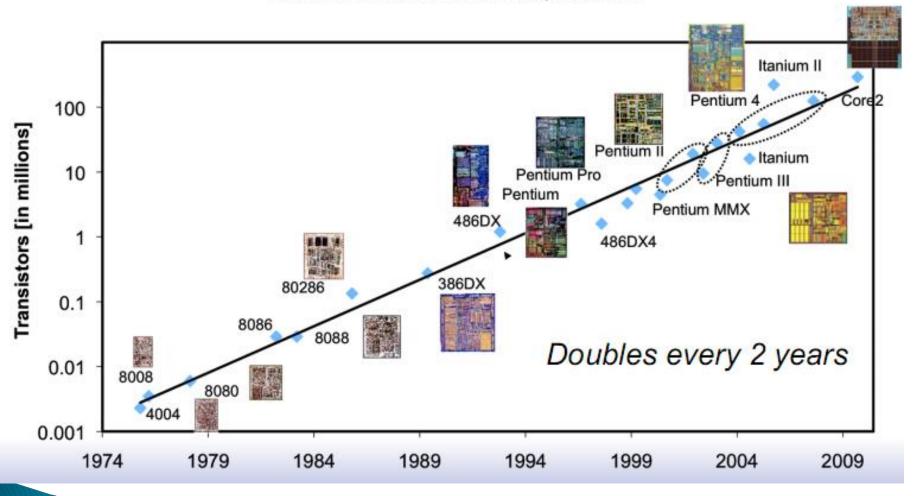
Intel Core 2 Microprocessor



Intel, 2006. 291,000,000 transistors (143mm²) 3 GHz operation (65nm CMOS technology)

Transistor Counts

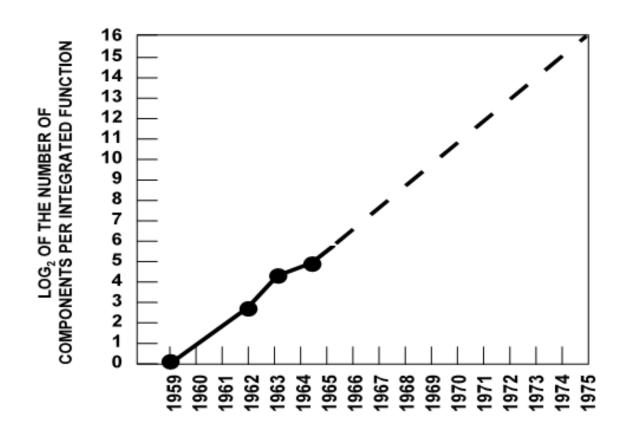
Transistor Counts in Intel's Microprocessors



Moore's Law

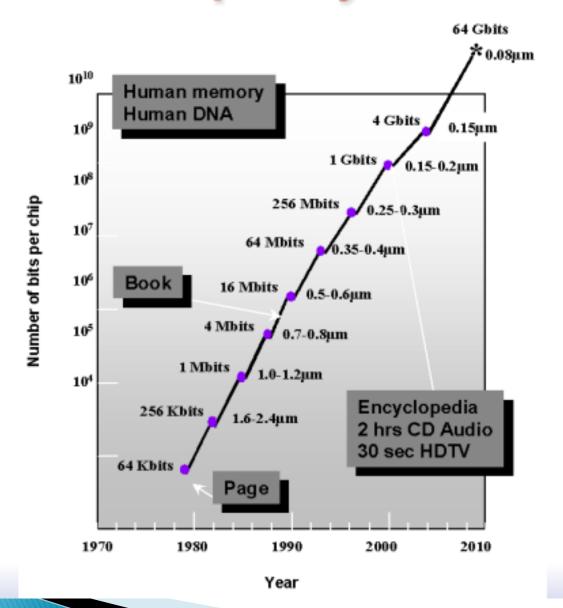
- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

Moore's Law



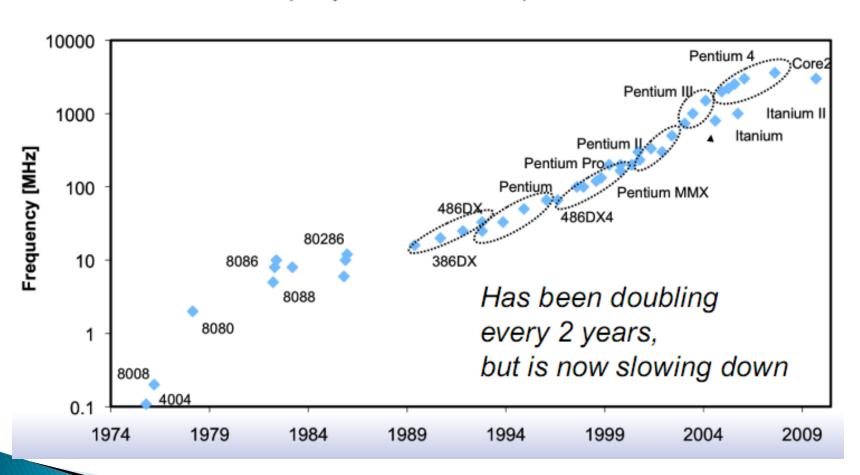
Electronics, April 19, 1965.

Evolution in Complexity

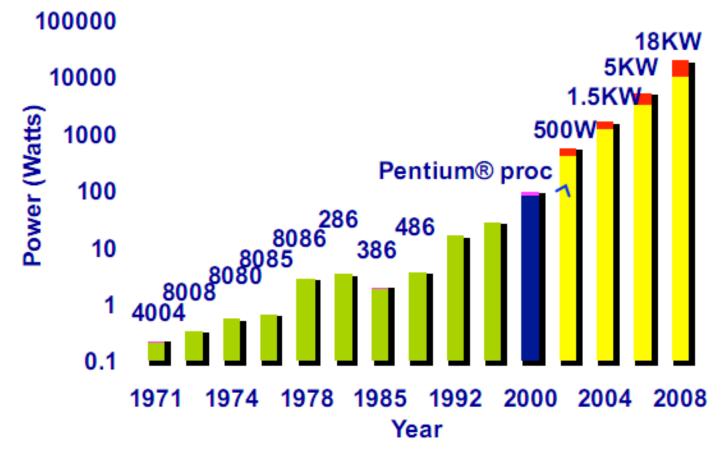


Frequency

Frequency Trends in Intel's Microprocessors



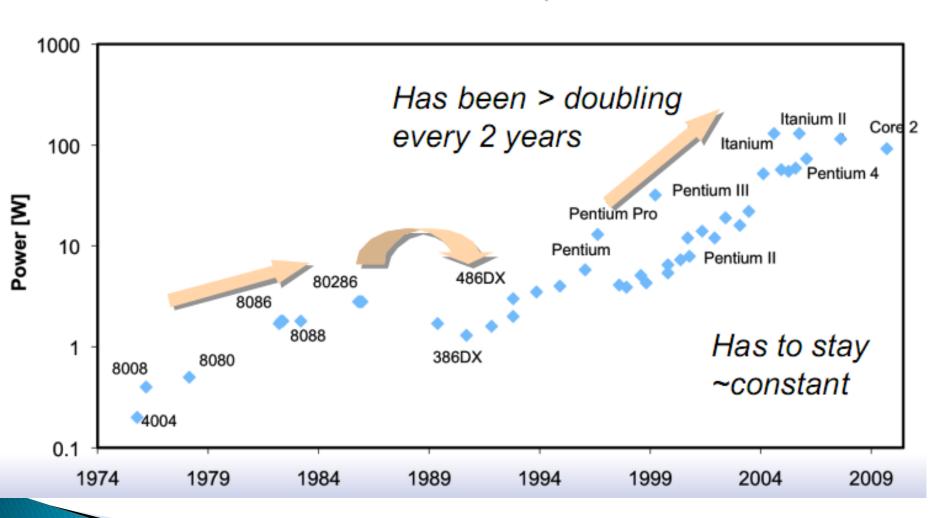
Power Dissipation Prediction (2000)



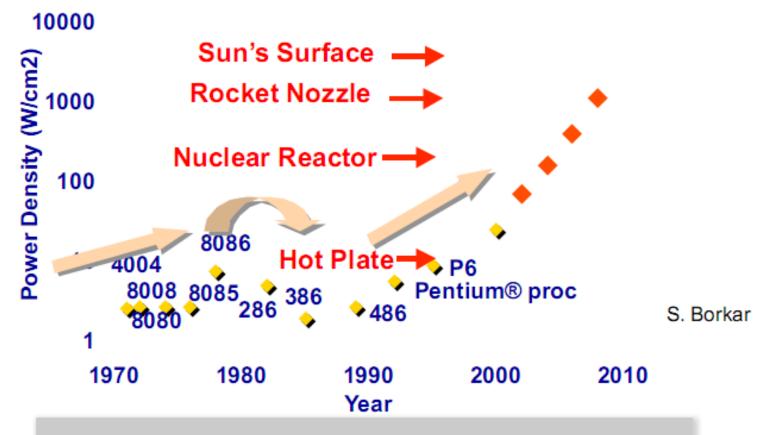
Did this really happen?

Power Dissipation Data

Power Trends in Intel's Microprocessors



Cause: Power Density



Power density too high for cost-effective cooling

Not enough cooling...





*Pictures from http://www.tomshardware.com/2001/09/17/hot_spot/

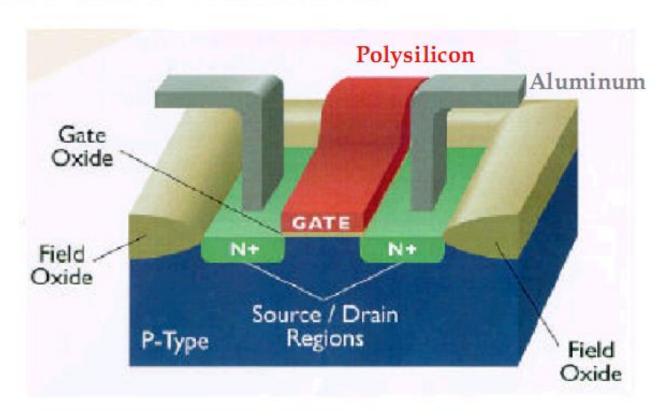
Why Scaling?

- □ Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- □ But ...
 - How to design chips with more and more functions?
 - Design engineering population does not double every two years...
- Hence, a need for more efficient design methods
 - Exploit different levels of abstraction

Intel Technology Roadmap

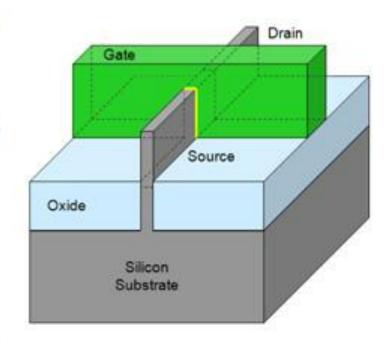
Process Name	P1266	P1268	P1270	P1272	P1274
Lithography	45 nm	32 nm	22 nm	14 nm	10 nm
1st Production	2007	2009	2011	2013	2015

The MOS Transistor



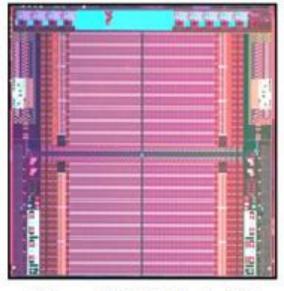
Tri-Gate Transistor Benefits

- Dramatic performance gain at low operating voltage, better than Bulk, PDSOI or FDSOI
 - 37% performance increase at low voltage >50% power reduction at constant performance
- Improved switching characteristics (On current vs. Off current)
- Higher drive current for a given transistor footprint
- Only 2-3% cost adder (vs. ~10% for FDSOI)



22 nm Tri-Gate Circuits

- 364 Mbit array size
- >2.9 billion transistors
- 3rd generation high-k + metal gate transistors
- Same transistor and interconnect features as on 22 nm CPUs

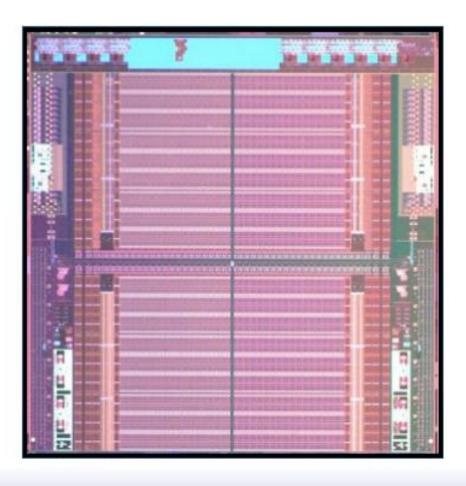


22 nm SRAM, Sept. '09

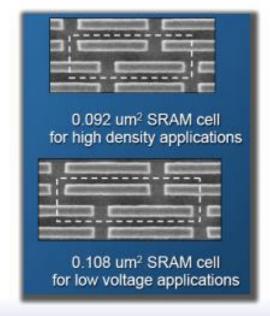
22 nm SRAMs using Tri-Gate transistors were first demonstrated in Sept. '09

Intel is now demonstrating the world's first 22 nm microprocessor (Ivy Bridge) and it uses revolutionary Tri-Gate transistors

Intel SRAM Prototype Chip (2009)



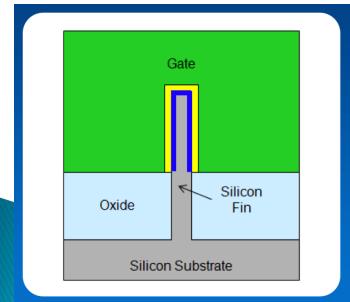
- □ 22 nm
- 364 Mbyte SRAM
- □ > 2.9 Billion Transistors
- □ 3rd generation high-k + metal gate



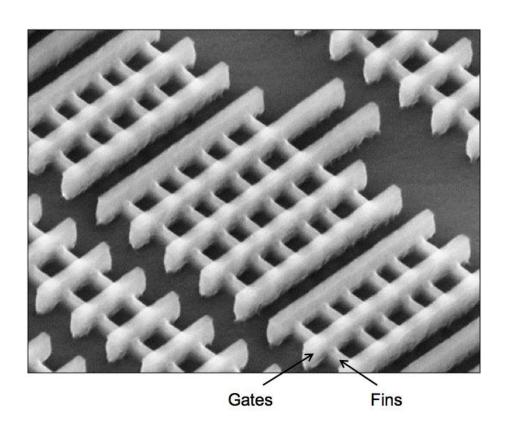
22 nm Tri-Gate Transistor

Oxide Silicon Substrate

Tri-Gate transistors can have multiple fins connected tog to increase total drive strength for higher performance



22 nm Tri-Gate Transistor



Challenges in Digital Design

"Microscopic Problems"

- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.



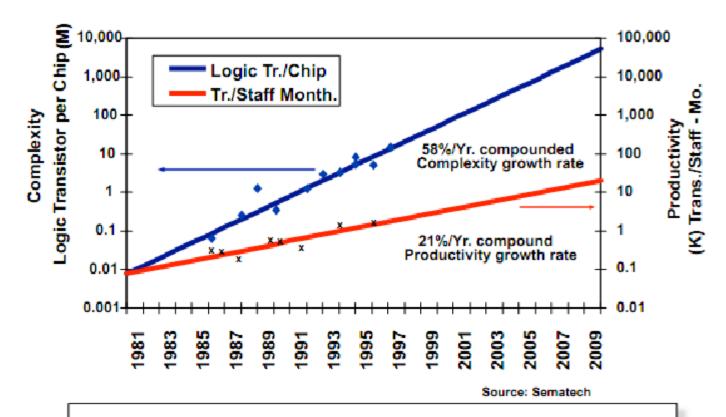
"Macroscopic Issues"

- Complexity
- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- · etc.

Everything Looks a Little Different

?

...and There's a Lot of Them!



Complexity outpaces design productivity

Courtesy, ITRS Roadmap

