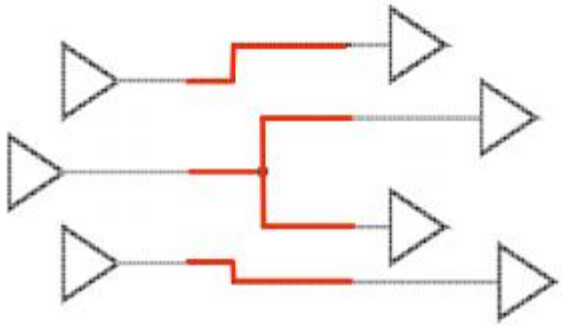
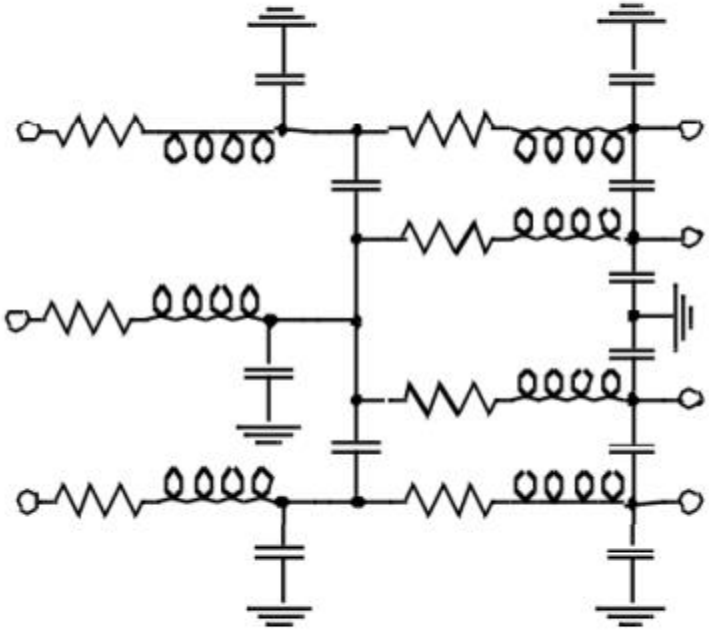
The Wire



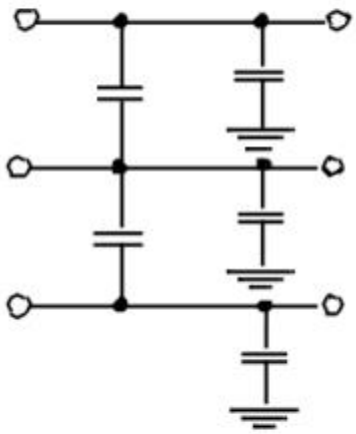
Schematic

Physical

Wire Models



All-inclusive model

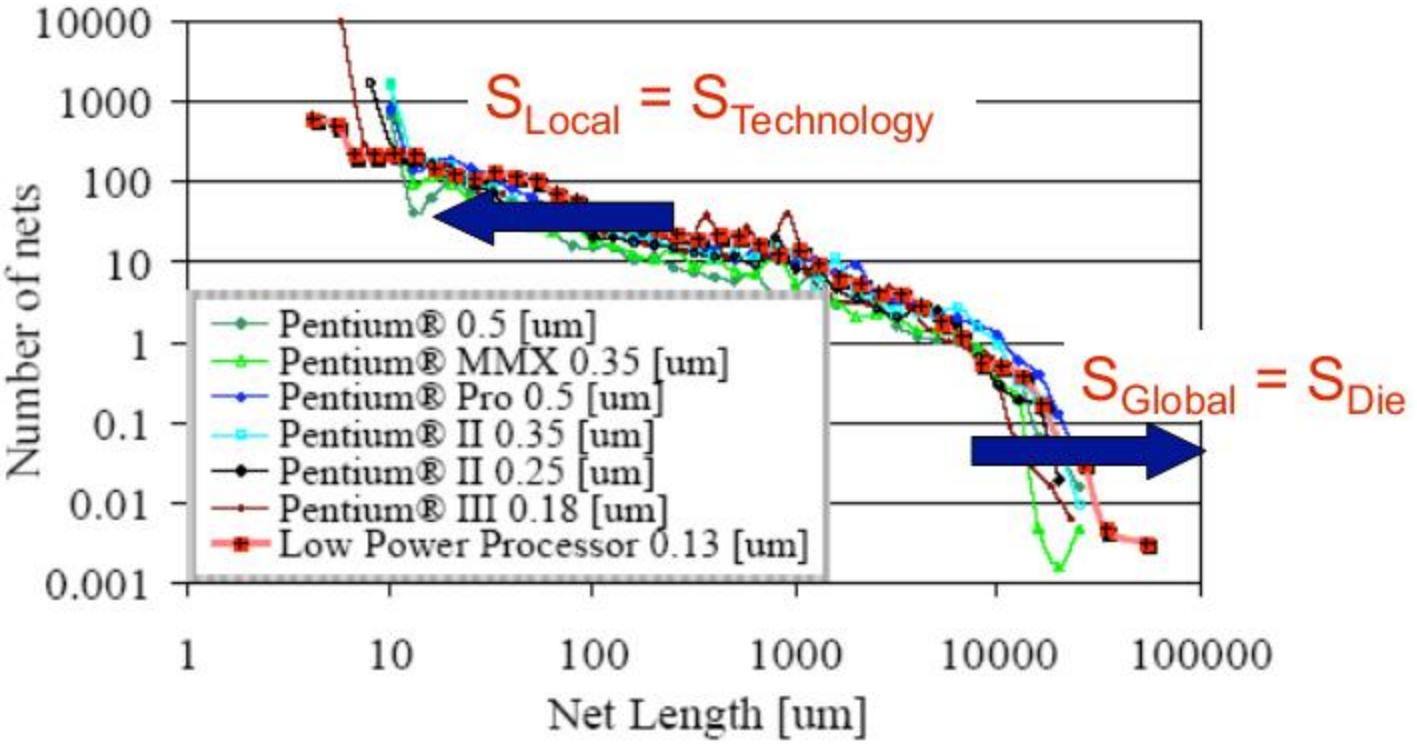


Capacitance-only

Impact of Interconnect Parasitics

- Interconnect and its parasitics can affect all of the metrics we care about
  - Cost, reliability, performance, power consumption
- Parasitics associated with interconnect:
  - Capacitance
  - Resistance
  - Inductance

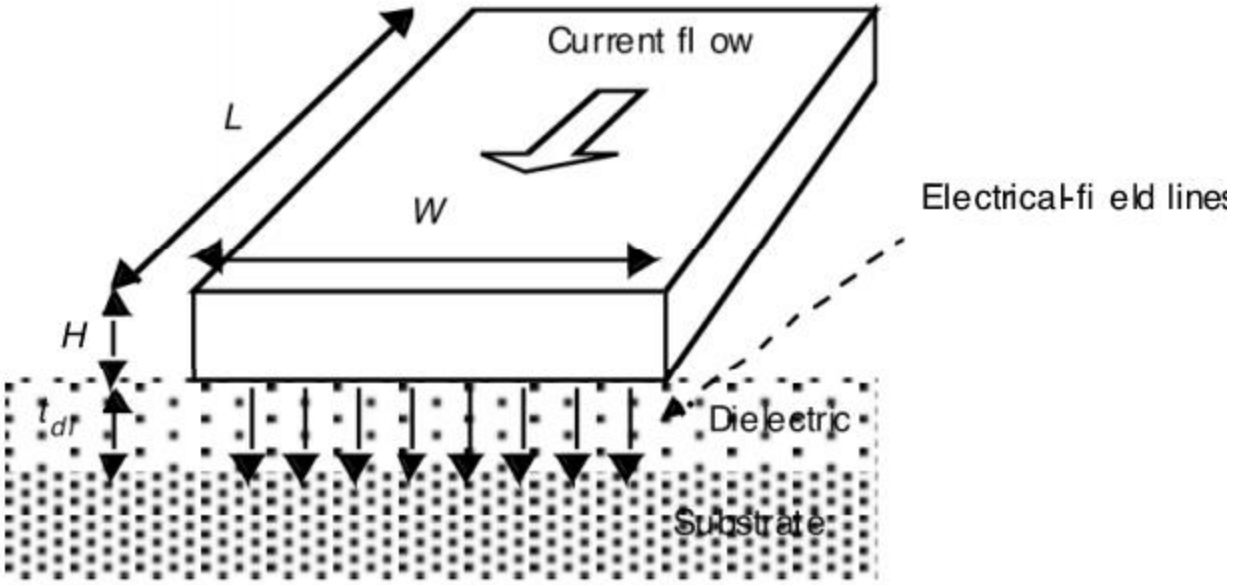
Interconnect Length Distribution



From Magen et al., "Interconnect Power Dissipation in a Microprocessor"

Buses, clock wire, global communication --- do not scale with technology

Capacitance: The Parallel Plate Model



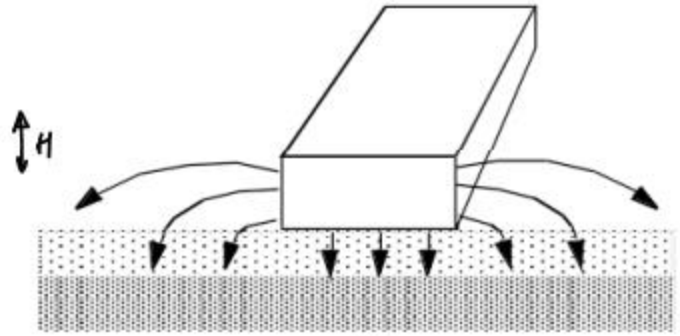
$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

Permittivity

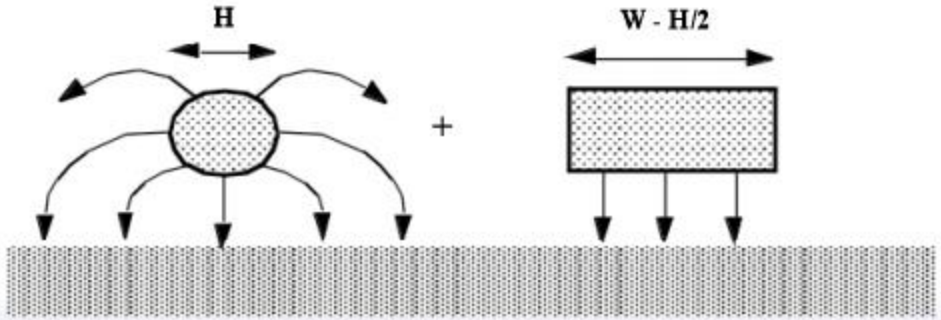
Material	ε_r
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

Fringing Capacitance

$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$



(a)

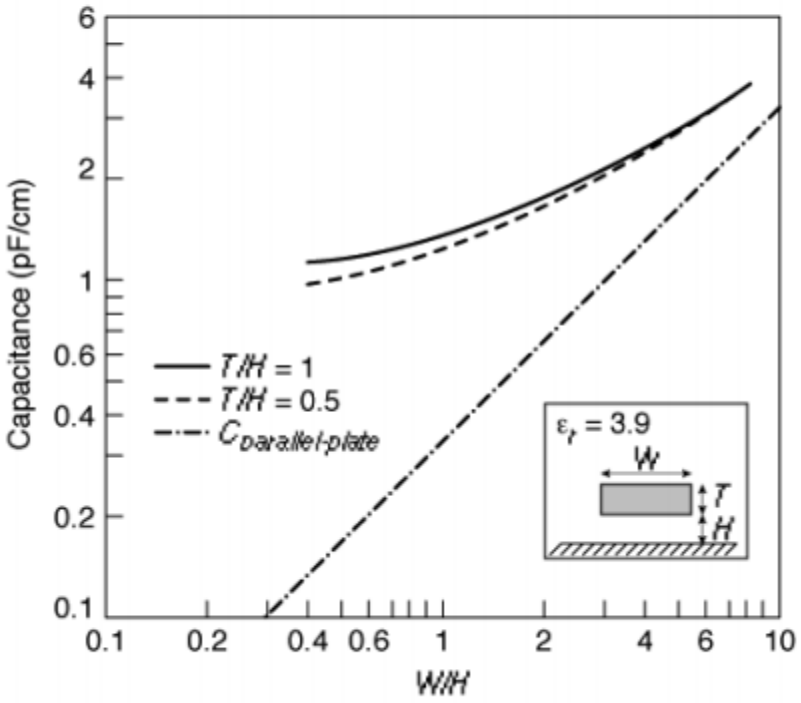


(b)

$$C = C_{pp} \cdot W \cdot L + 2 C_{fringe} L$$

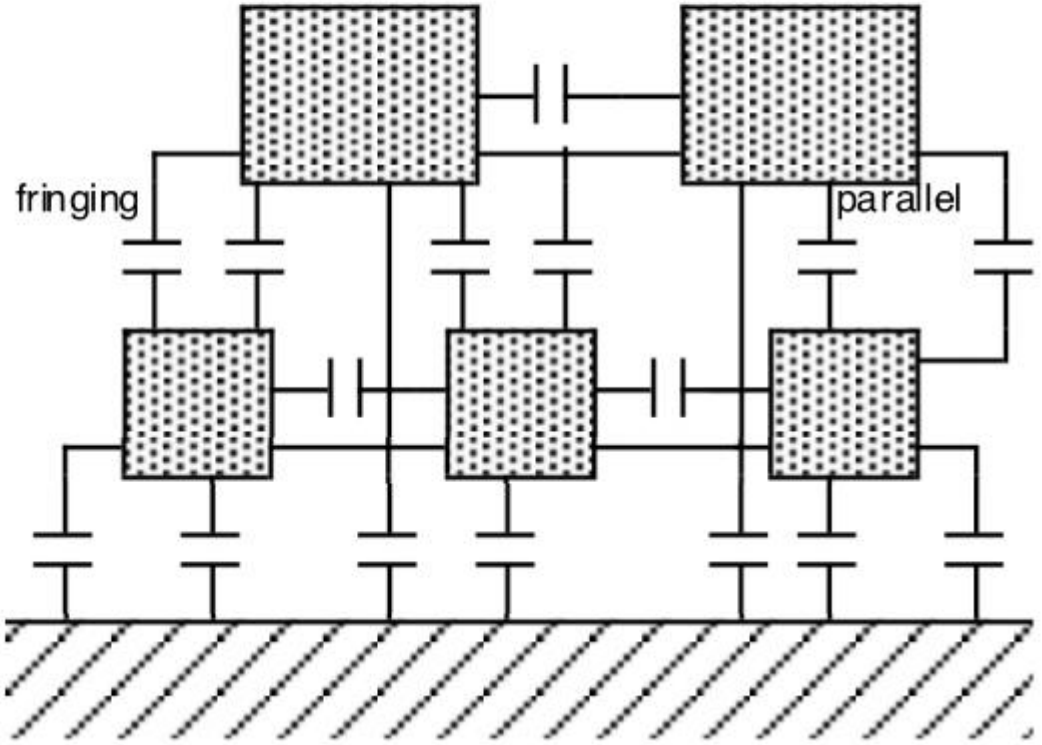
Fringing versus Parallel Plate

Fringe is dominant

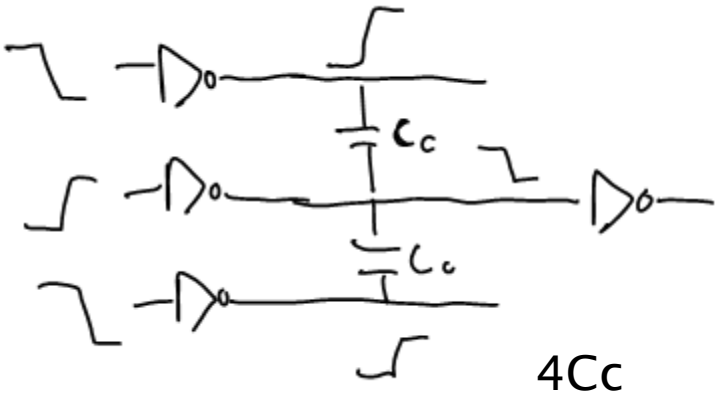


(from [Bakoglu89])

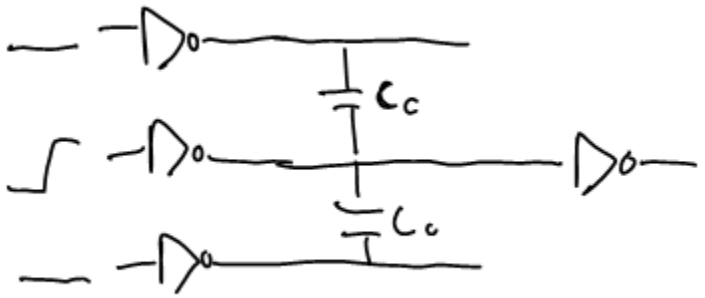
Interwire Capacitance



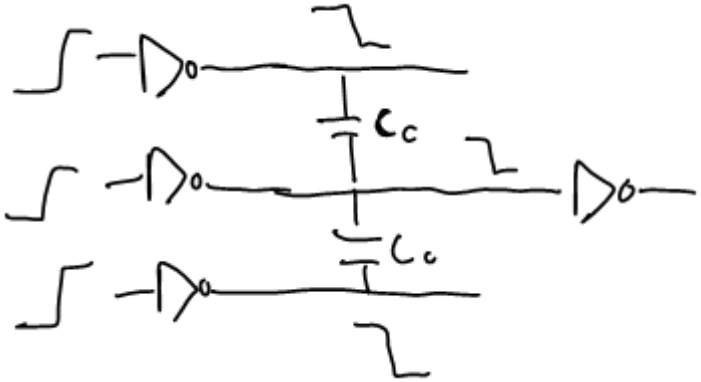
Coupling Capacitance and Delay



4Cc

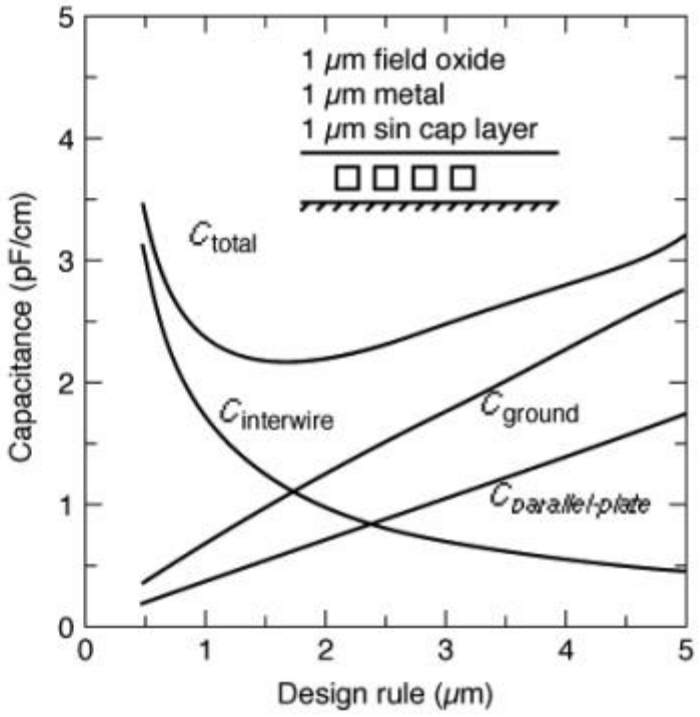


$C_{c,\,eff} =$ 2Cc



zero

Impact of Interwire Capacitance



(from [Bakoglu89])

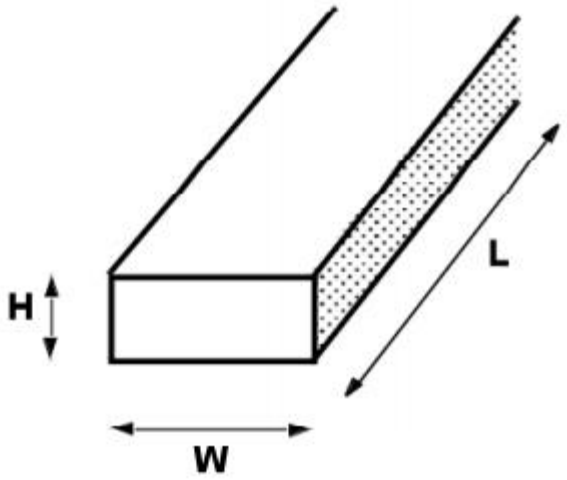
Wiring Capacitances (0.25 μm CMOS)

Bottom plate

Top plate

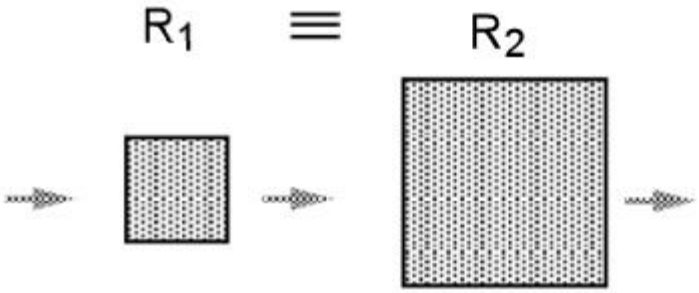
	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88	aF/μm²					
	54	aF/μm					
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

Wire Resistance



$$R = \rho \frac{L}{H W}$$

Sheet Resistance
R_o



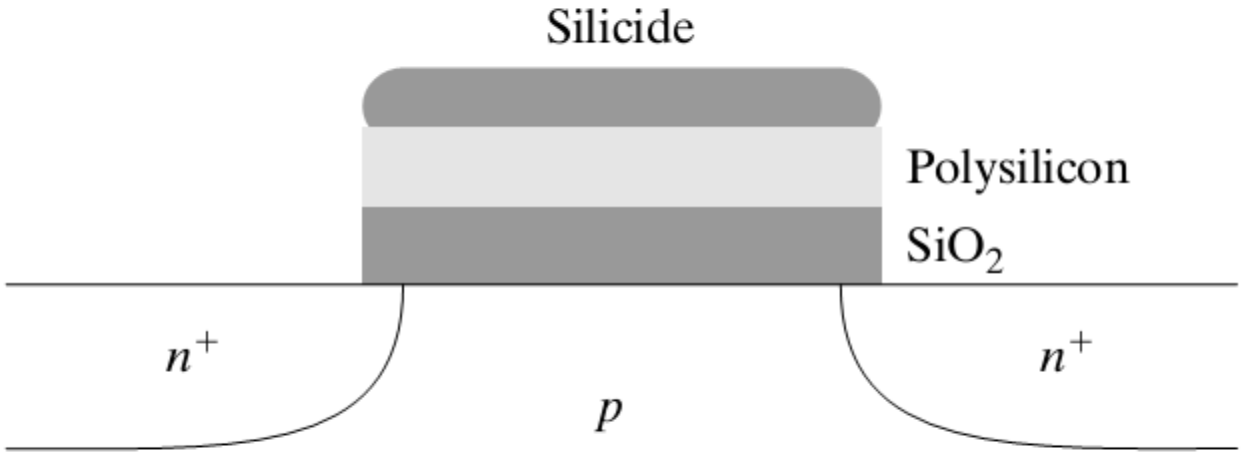
Interconnect Resistance

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Dealing with Resistance

- **Use Better Interconnect Materials**
  - e.g. copper, silicides
- **More Interconnect Layers**
  - reduce average wire-length
- **Selective Technology Scaling**

Polycide Gate MOSFET



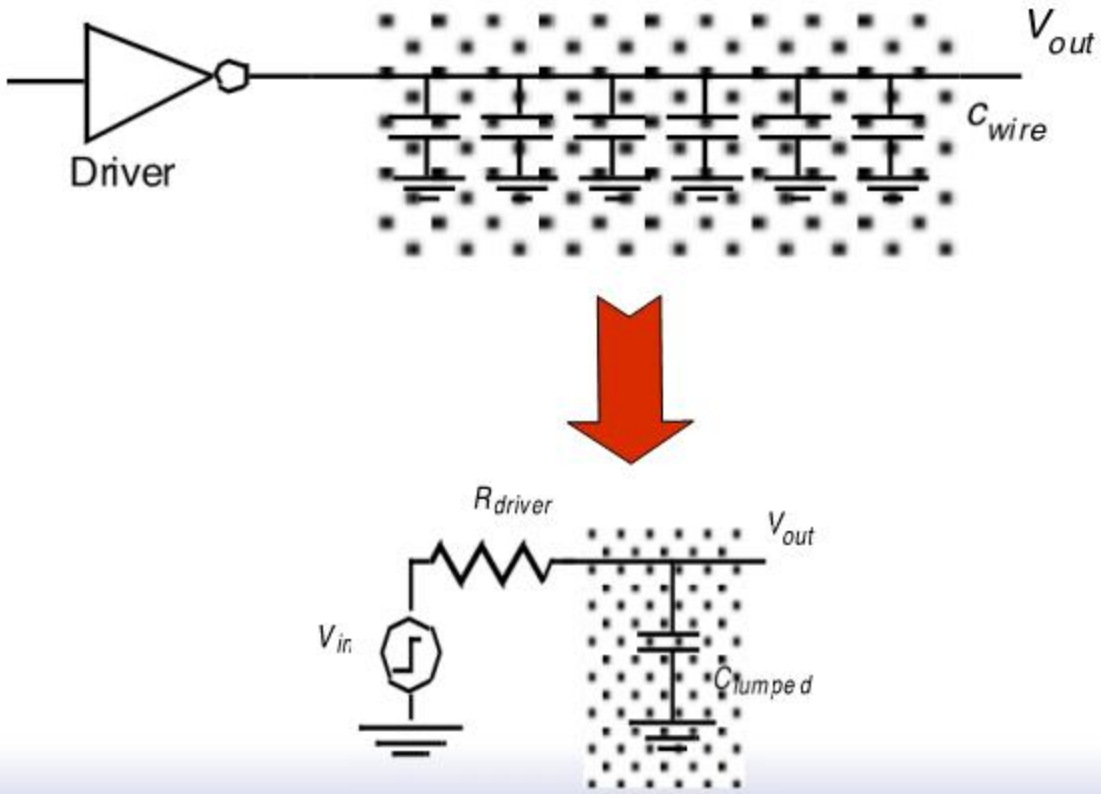
Silicides: WSi_2, $TiSi_2$, $PtSi_2$ and TaSi

Conductivity: 8-10 times better than Poly

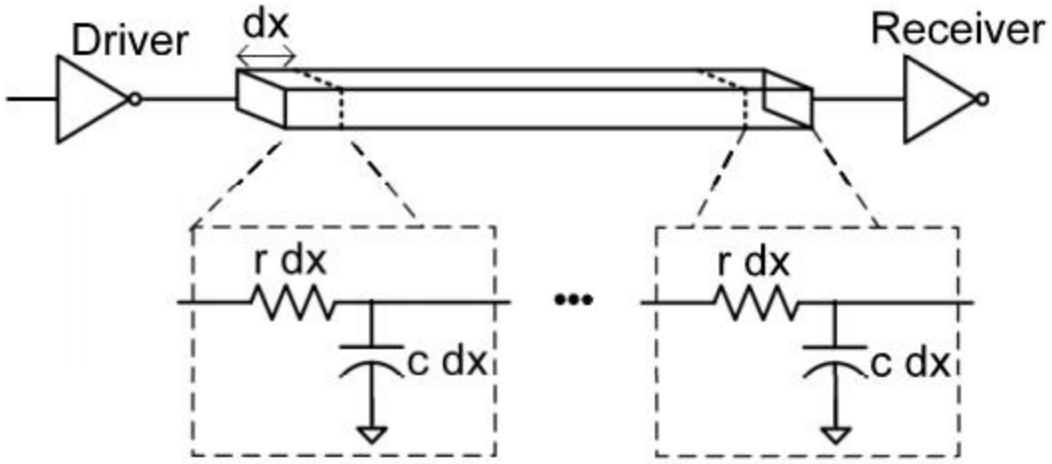
Sheet Resistance

Material	Sheet Resistance (Ω/❑)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

The Lumped Model

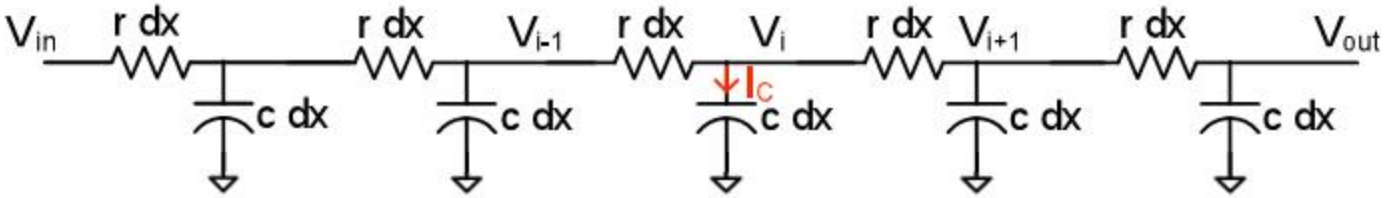


The Distributed RC-line



- Analysis method:
  - Break the wire up into segments of length dx
  - Each segment has resistance (r dx) and capacitance (c dx)

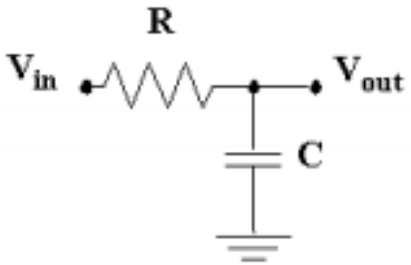
The Distributed RC-line



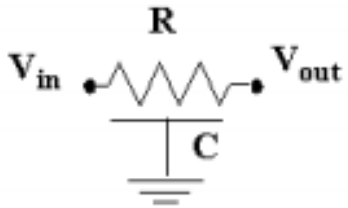
$$I_C = c\Delta L\frac{\partial V}{\partial t} = \frac{(V_{i-1} - V_i) - (V_i - V_{i+1})}{r\Delta L} \longrightarrow \boxed{rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}}$$

$$\boxed{\tau = \frac{L^2}{2}rc}$$

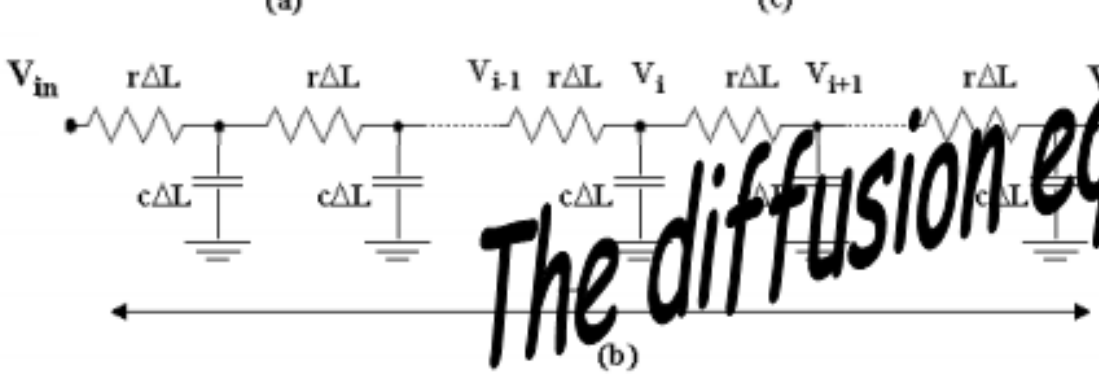
The Distributed RC Line



(a)



(c)



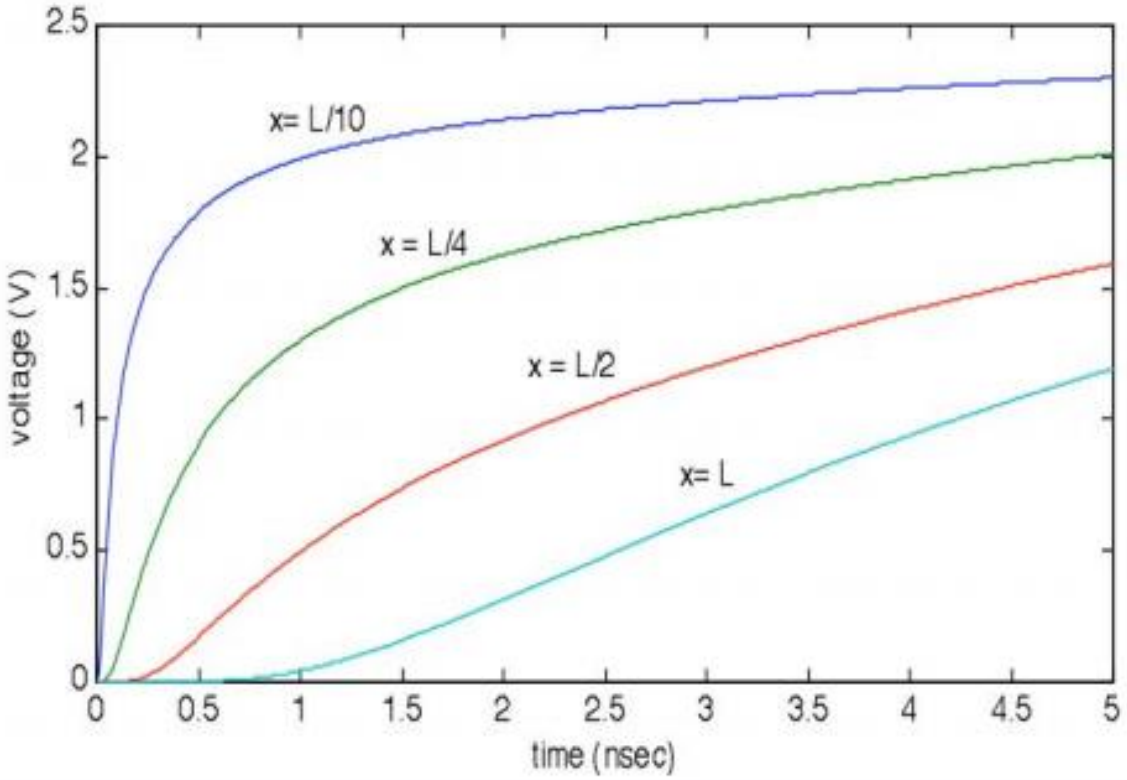
(b)

The diffusion equation

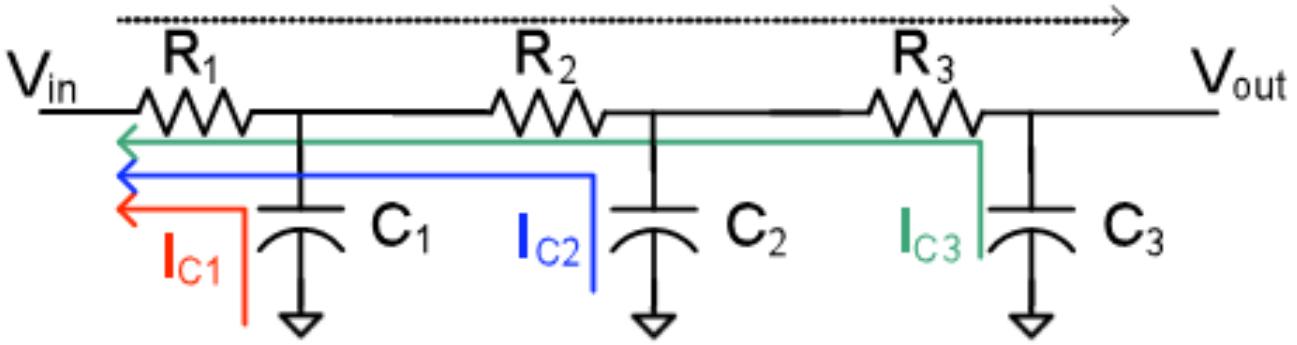
$$rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}$$

$$\tau(V_{out}) = \frac{rc\,L^2}{2}$$

Step-response of RC wire as a function of time and space

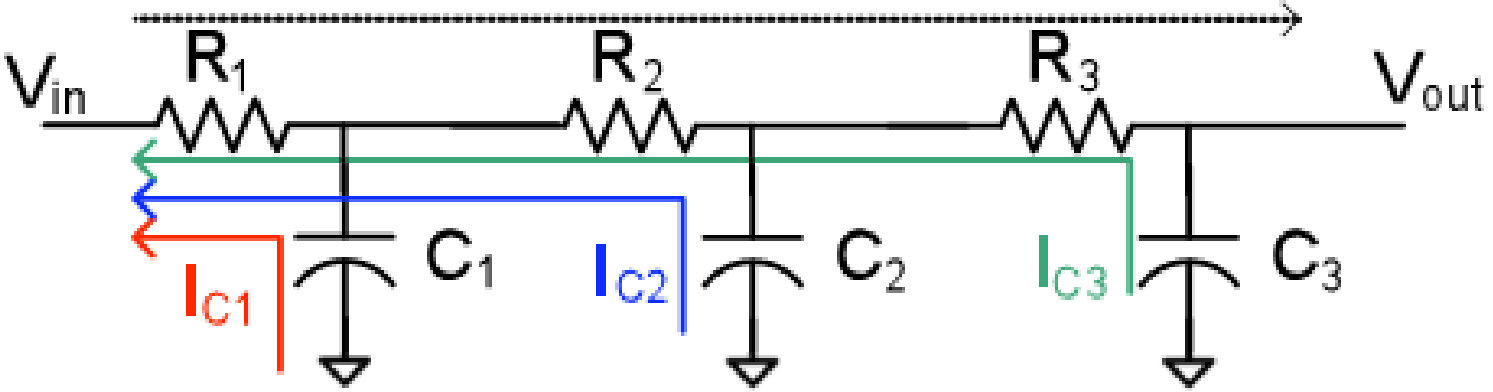


Simplified Model: Elmore Delay



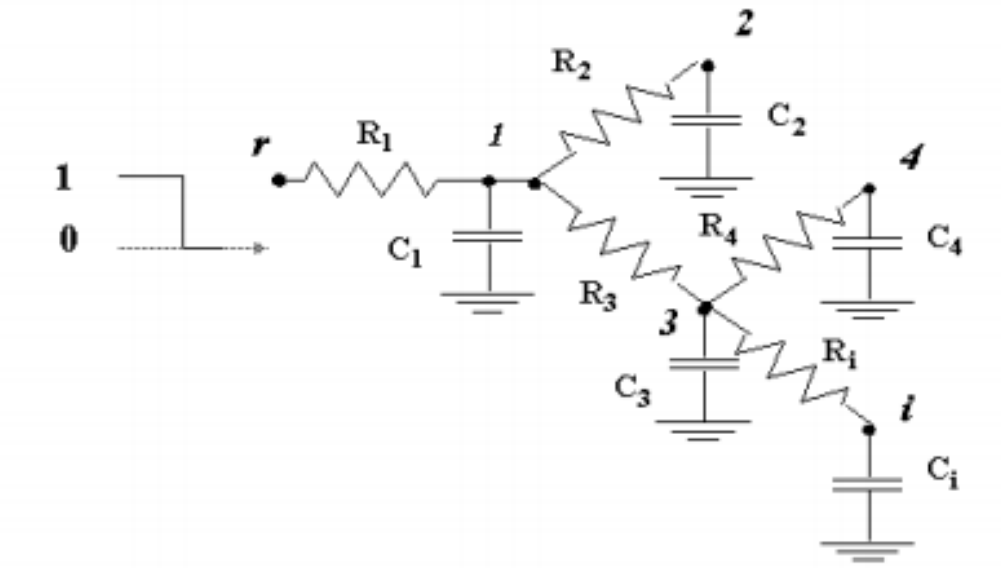
- "Elmore delay": approximation for delay of arbitrary (complex) RC circuits
- To find "Elmore time constant":
  - For each capacitor, draw path of current from cap to input
  - Multiply C by sum of R's on current path that are common with path from V_{in} to V_{out}
  - Add up RC products from all capacitors

Simplified Model: Elmore Delay



$$\tau_{Elmore} = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3$$

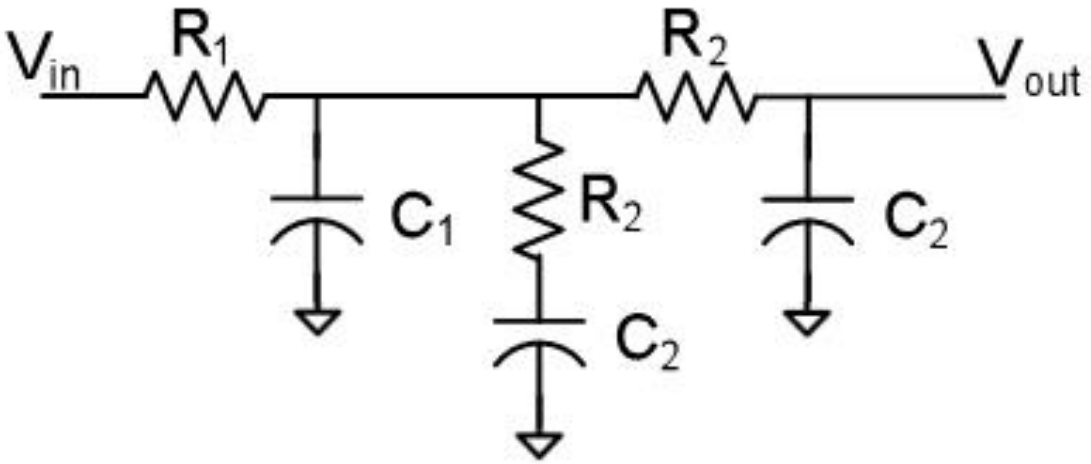
Elmore Delay - Extended



$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \to i) \cap path(s \to k)])$$

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

Another Elmore Delay Example



$$\tau_{Elmore} =$$

Wire Model

Model the wire with N equal-length segments:

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \ldots + Nrc) = (rcL^2)\frac{N(N+1)}{2N^2} = RC\frac{N+1}{2N}$$

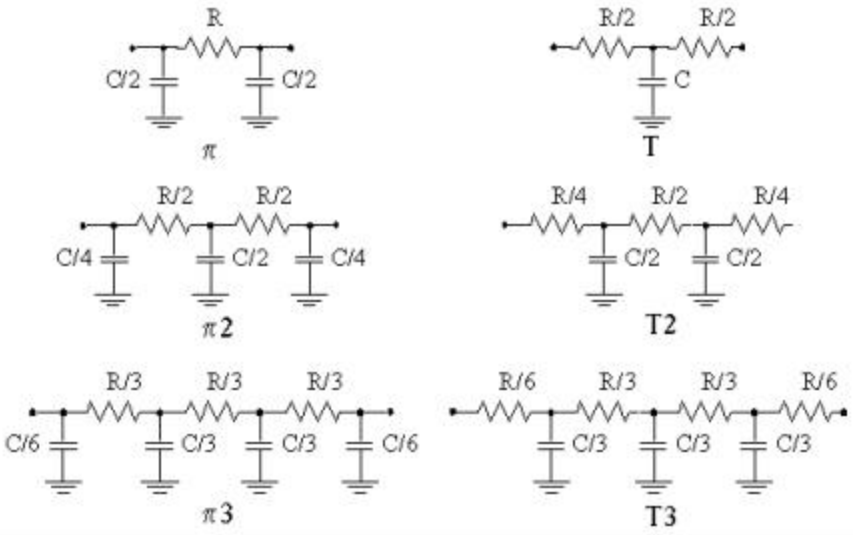
For large values of N:

$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

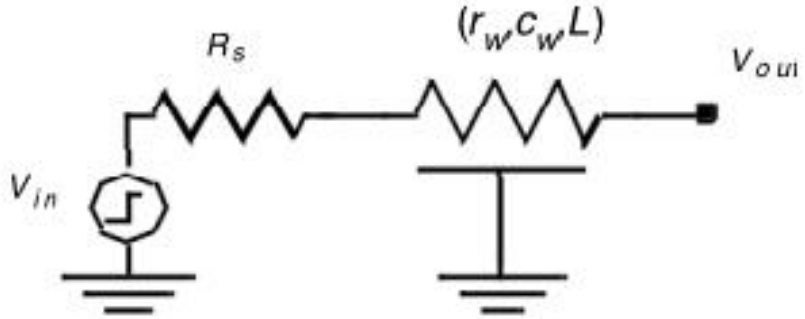
RC-Models

Voltage Range	Lumped RC-network	Distributed RC-network
0→50% (t_p)	0.69 RC	0.38 RC
0→63% (τ)	RC	0.5 RC
10%→90% (t_r)	2.2 RC	0.9 RC

Step Response of Lumped and Distributed RC Networks: Points of Interest.



Driving an RC-line



$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

$$t_p = 0.69 R_s C_w + 0.35 R_w C_w$$

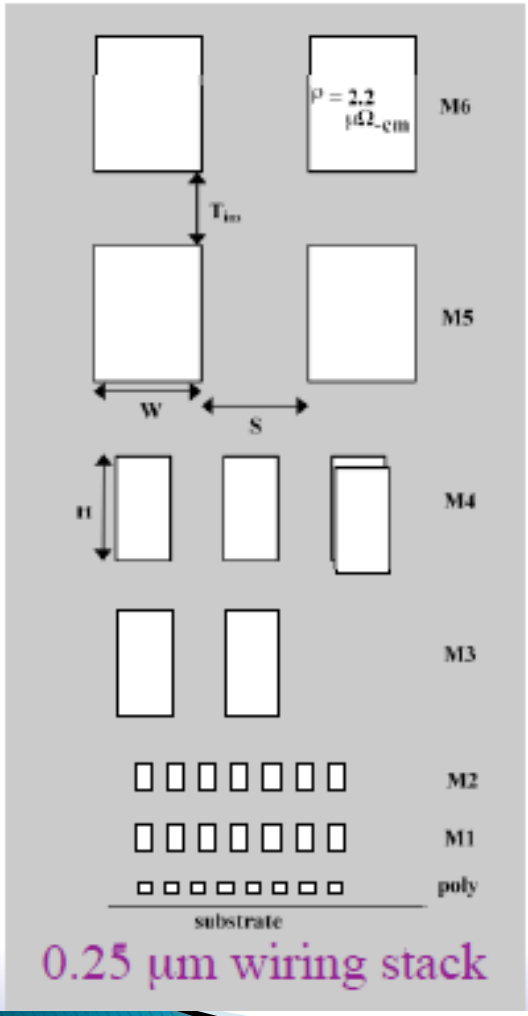
The Global Wire Problem

$$T_d = 0.35\, R_w C_w + 0.693\left(R_d C_{out} + R_d C_w + R_w C_{out}\right)$$

Challenges

- No further improvements to be expected after the introduction of Copper (superconducting, optical?)
- Design solutions
  - Use of fat wires
  - Efficient chip floorplanning
  - Insert repeaters

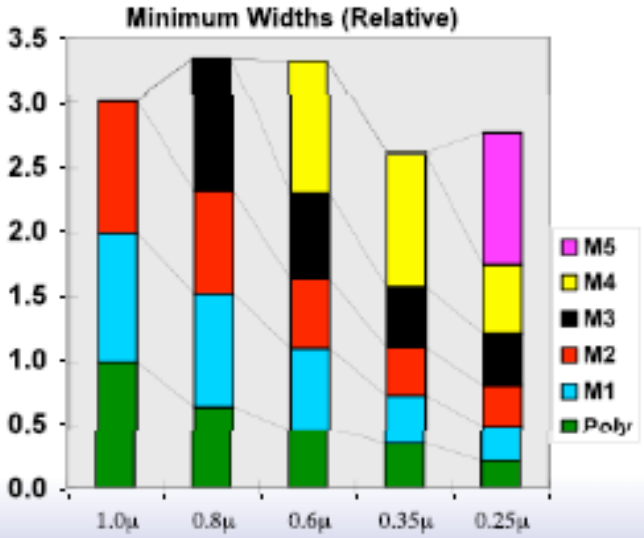
Interconnect: # of Wiring Layers

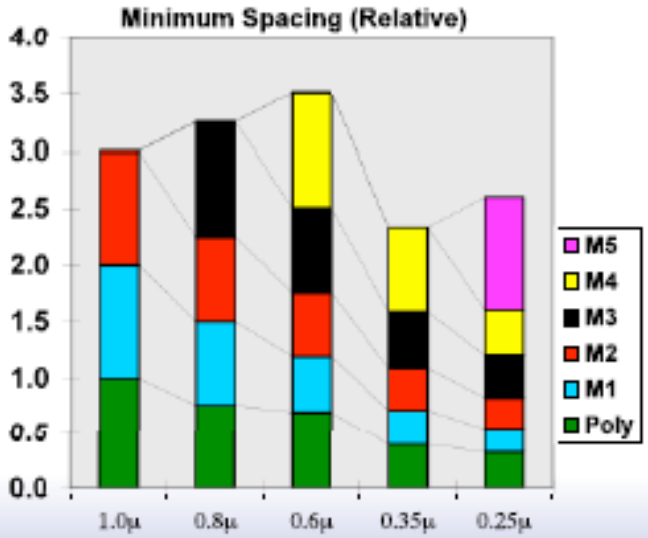


0.25 μm wiring stack

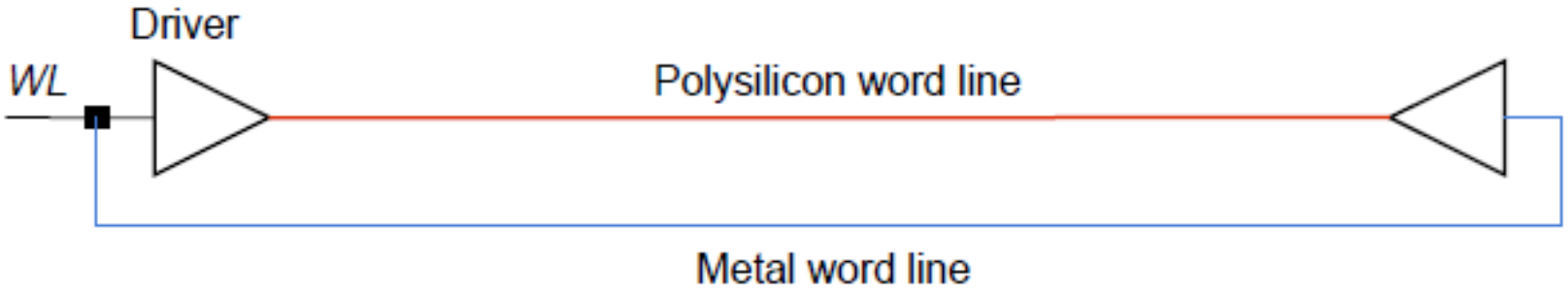
# of metal layers is steadily increasing due to:

- Increasing die size and device count: we need more wires and longer wires to connect everything
- Rising need for a hierarchical wiring network; local wires with high density and global wires with low RC

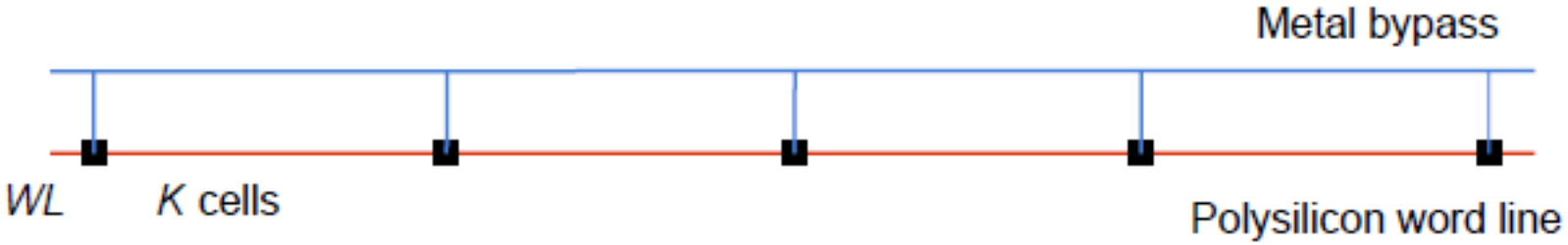




Using Bypasses

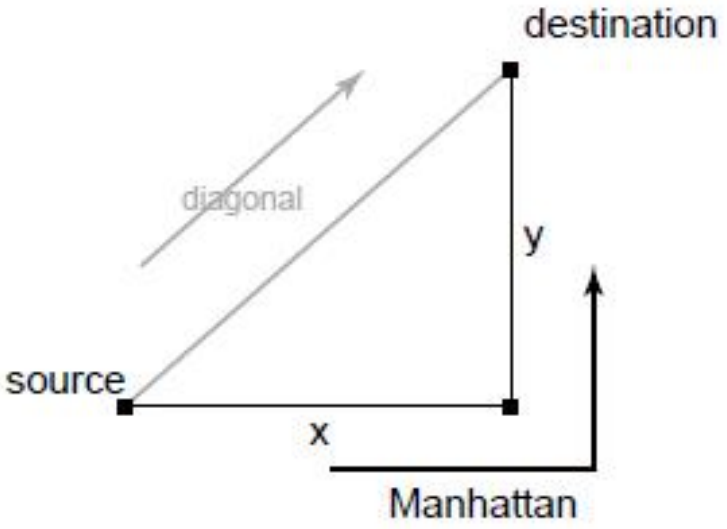


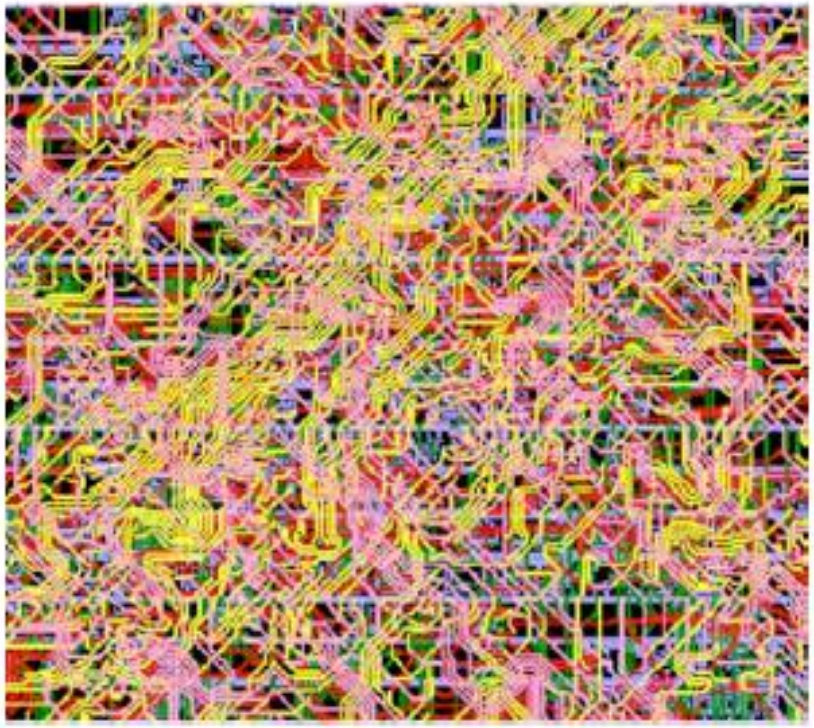
Driving a word line from both sides



Using a metal bypass

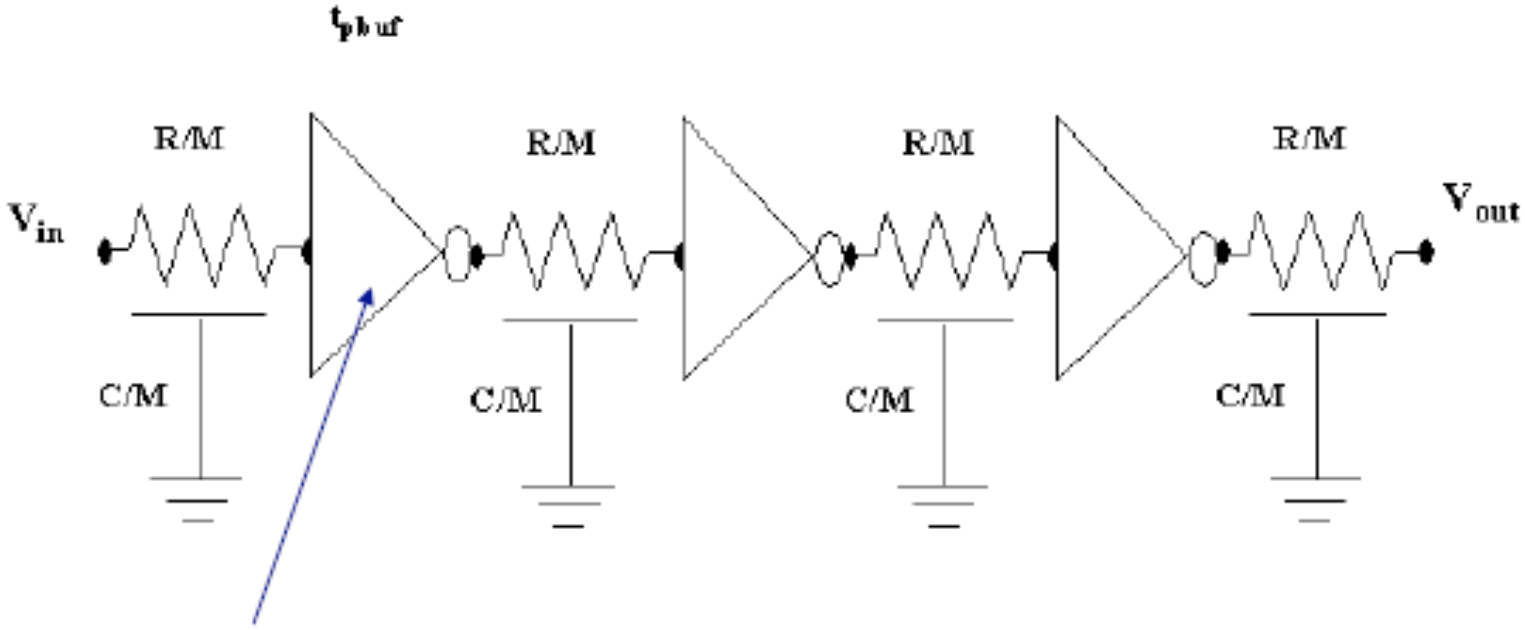
Diagonal Wiring



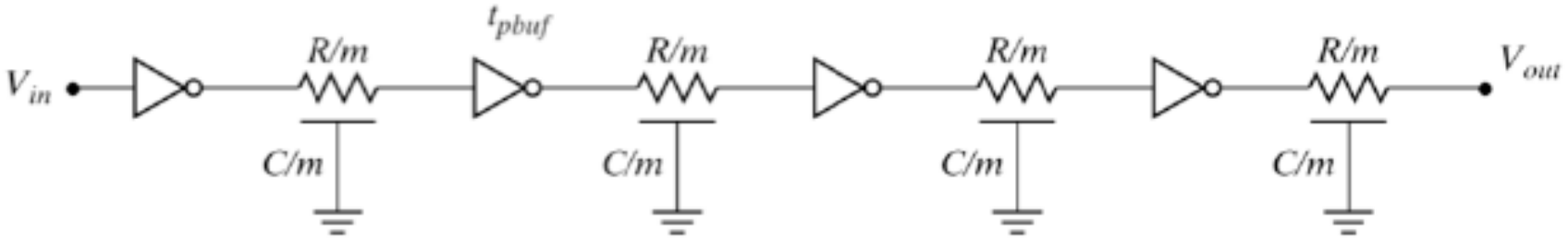


- 20+% Interconnect length reduction
- Clock speed
  Signal integrity
  Power integrity
- 15+% Smaller chips
  plus 30+% via reduction

Reducing RC-delay Using Repeaters



Repeaters



$$t_p = m\left(0.69\frac{R_d}{s}\left(s\gamma C_d + \frac{cL}{m} + sC_d\right) + 0.69\left(\frac{rL}{m}\right)(sC_d) + 0.38rc\left(\frac{L}{m}\right)^2\right)$$

$$m_{opt} = L\sqrt{\frac{0.38rc}{0.69R_dC_d(\gamma+1)}} = \sqrt{\frac{t_{pwire(unbuffered)}}{t_{p1}}}$$

$$s_{opt} = \sqrt{\frac{R_dc}{rC_d}}$$

Repeater Insertion (Revisited)

Taking the repeater loading into account

$$m_{opt} = L\sqrt{\frac{0.38rc}{0.69R_dC_d(\gamma+1)}} = \sqrt{\frac{t_{pwire(unbuffered)}}{t_{p1}}}$$

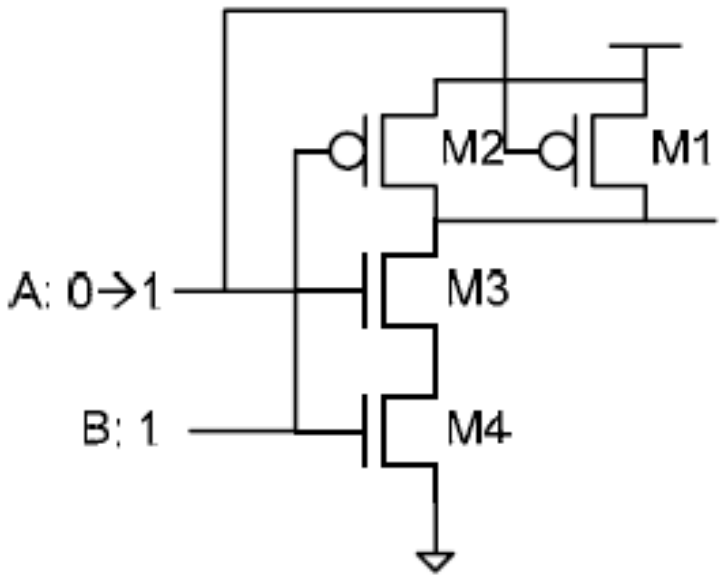
$$s_{opt} = \sqrt{\frac{R_d c}{rC_d}}$$

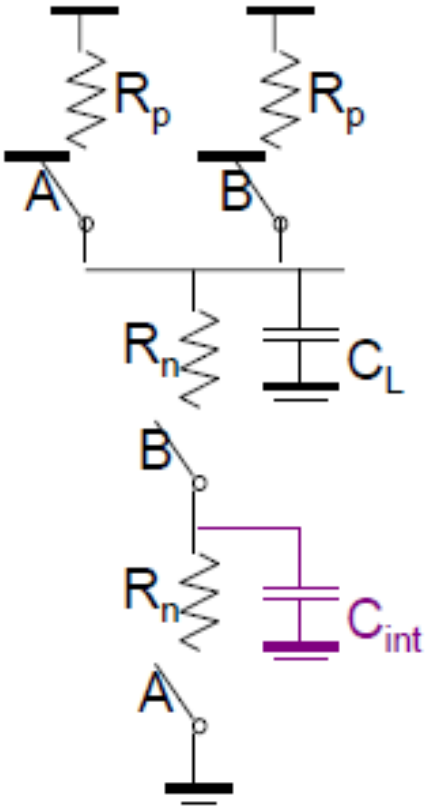
For a given technology and a given interconnect layer, there exists an optimal length of the wire segments between repeaters. The delay of these wire segments is independent of the routing layer!

$$L_{crit} = \frac{L}{m_{opt}} = \sqrt{\frac{t_{p1}}{0.38rc}} \qquad t_{p,crit} = \frac{t_{p,min}}{m_{opt}} = 2\left(1+\sqrt{\frac{0.69}{0.38(1+\gamma)}}\right)t_{p1}$$

Complex Gate Delay

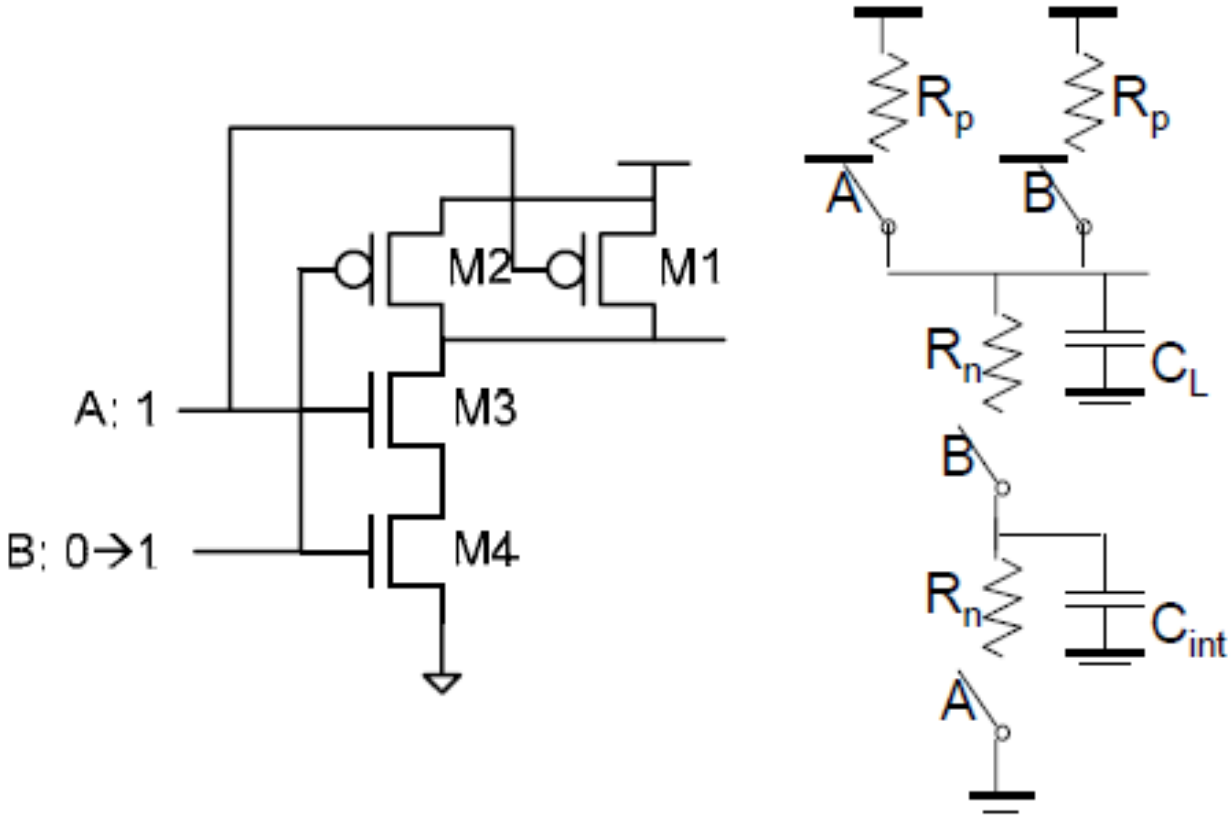
- Use RC model to estimate delay:





Complex Gate Delay (2)

- What is the delay in this case?



PROBLEM……

PROBLEM 2: Complex Gate Delay

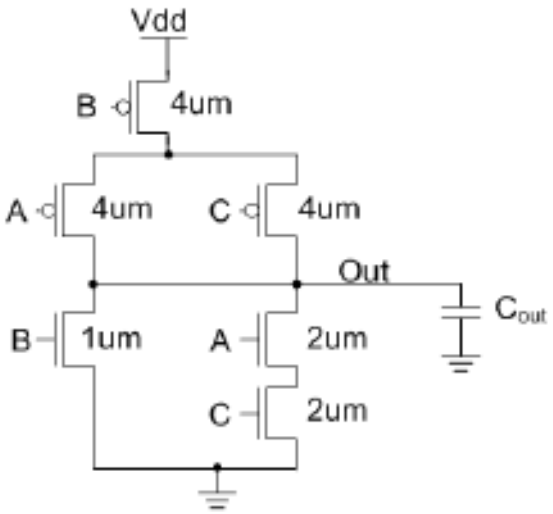
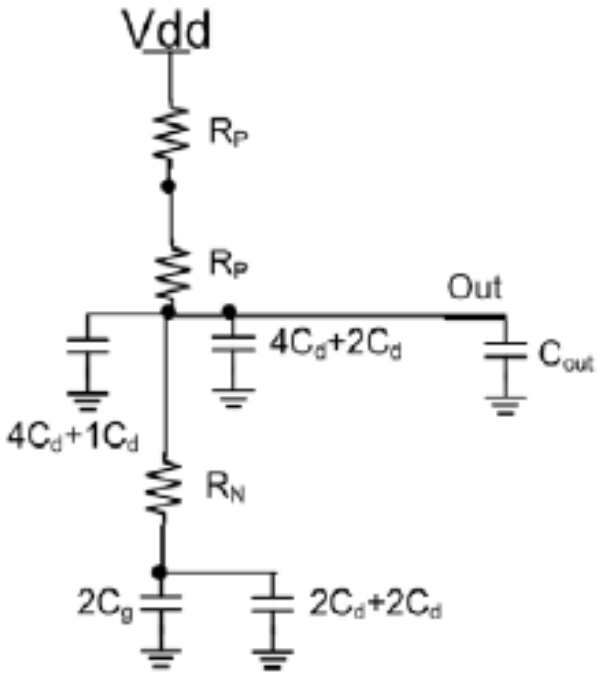


Figure 3.

For this problem you should assume that L_{min} = 100nm, C_g=2 fF/μm, C_d=1.6 fF/μm, R_p=20 kΩ/□, and R_n=10 kΩ/□, C_{out} = 12fF.

a) If A = 1 and B = 0, draw the switch model you would use to calculate the delay of the gate when C transitions from 1 to zero (i.e., the output going high).

Using the switch model, the equivalent RC circuit we would use to calculate the delay when A = 1, B = 0, and C transitions from 1 to zero is shown below.



b) What is the delay of the gate in this case?

Solution:

Using Elmore delay, the time constant for this circuit is:

$$\tau_{LH} = 2R_P\left(5C_d + 6C_d + 2C_g + 4C_d + C_{out}\right)$$

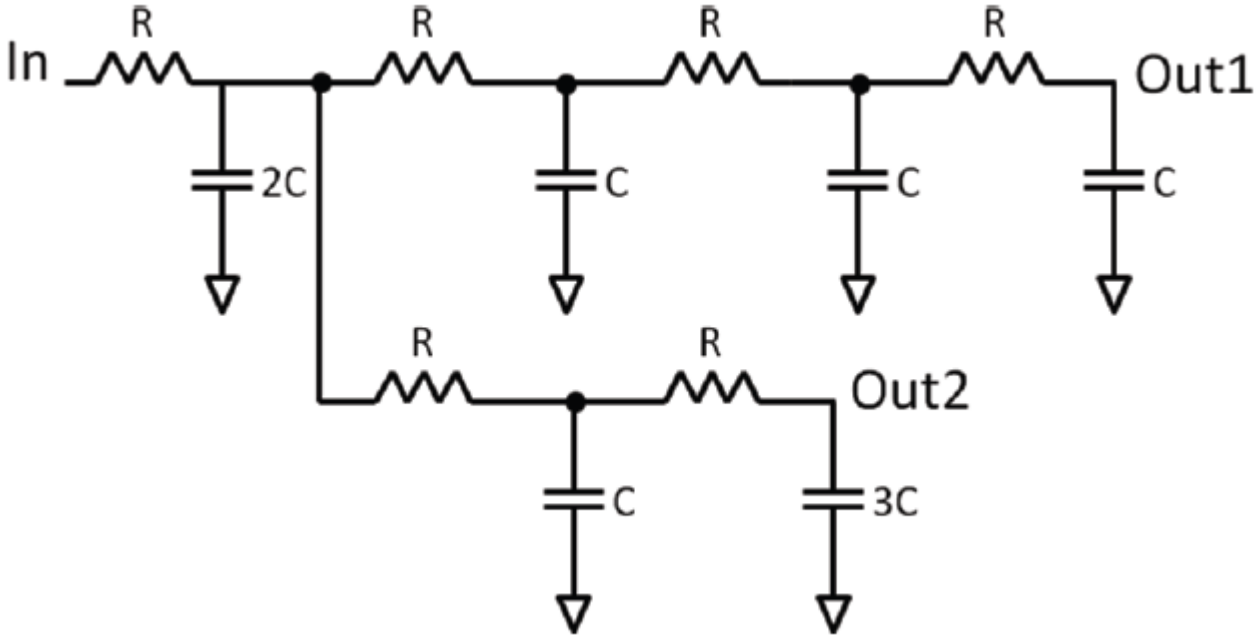
Where the resistance of each PMOS transistor is:

$$R_P = R_p\frac{L}{W} = 20k\Omega\frac{0.1\mu m}{4\mu m} = 500\Omega$$

Therefore, t_{pLH} for the gate will be:

$$t_{pLH} = ln2 \times \tau_{LH} = ln2 \times 2 \times 500\Omega \times (5 \times 1.6fF + 6 \times 1.6fF + 2 \times 2fF + 4 \times 1.6fF + 12fF\ ) \approx 27.73ps$$

Calculate Elmore delay from In to out1 and from In to out2?



Solution:
Elmore to out1 is 15RC
Elmore to out2 is 16RC