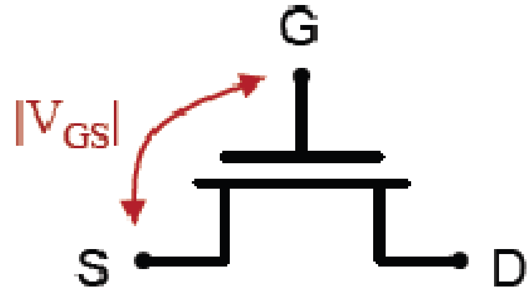
Design Metrics

Textbook: 2.1, 2.2

What is a Transistor?

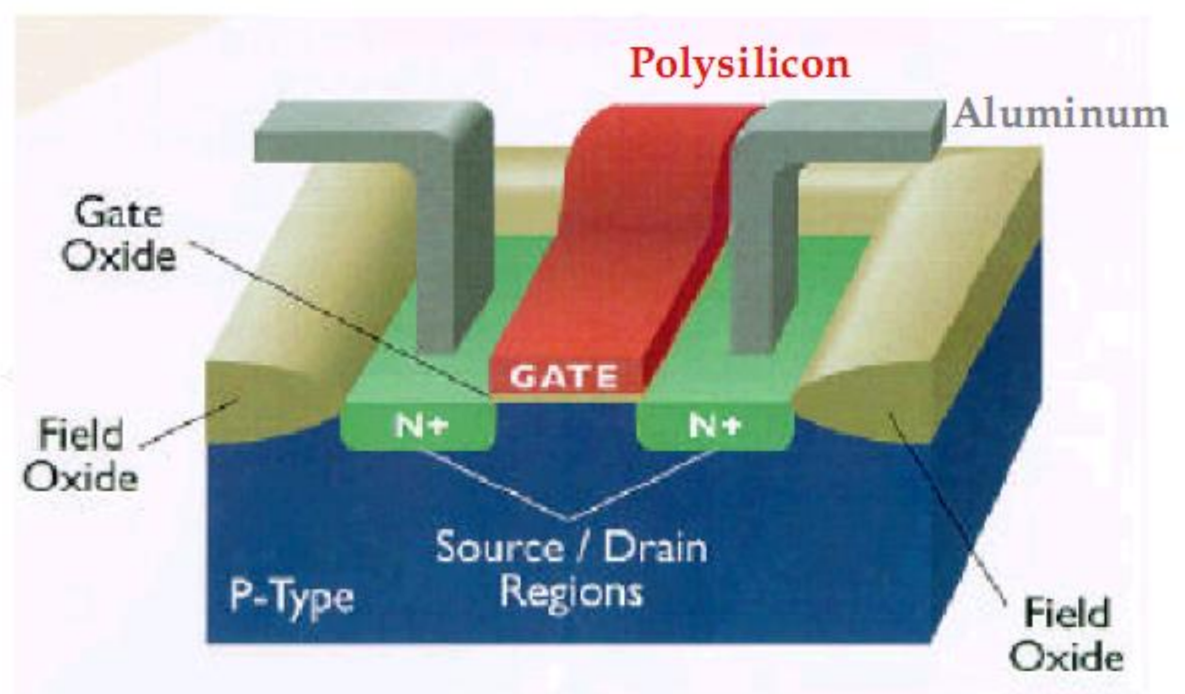
An MOS Transistor ⟷ A Switch!



Design Metrics

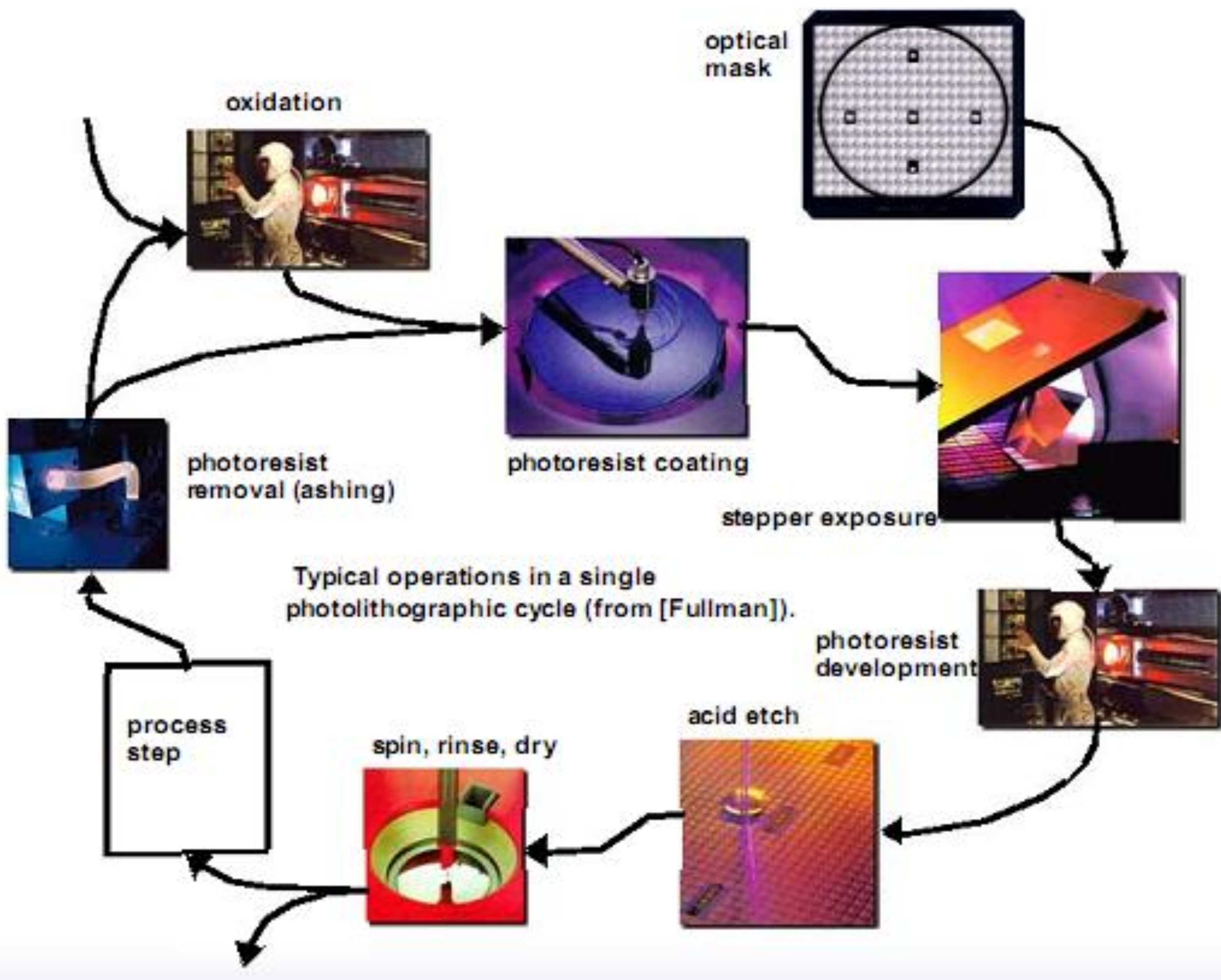
- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Speed/Performance (delay, frequency)
  - Power

Introduction to IC CMOS Manufacturing

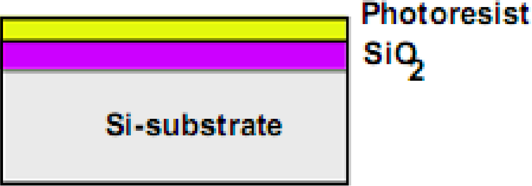


CMOS Manufacturing Process

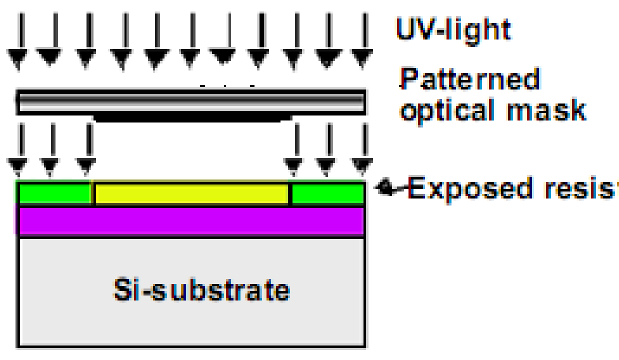
Photo-Lithographic Process



Patterning of SiO_2

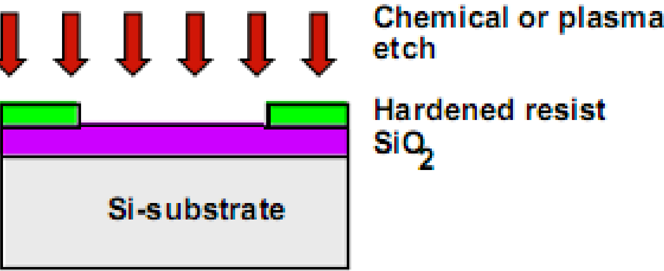


(a) Silicon base material

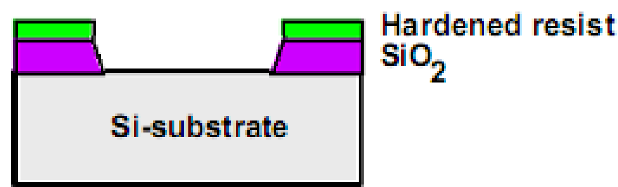


(b) After oxidation and deposition of negative photoresist

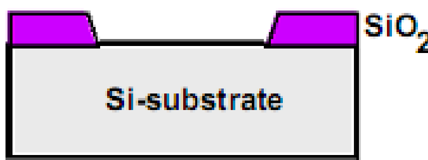
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2

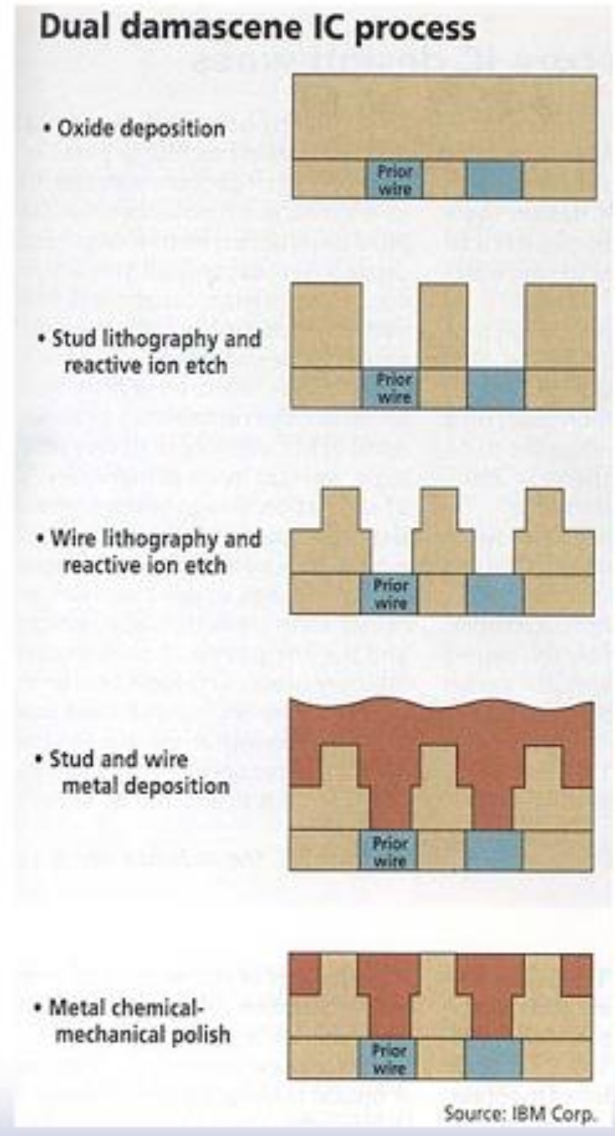


(e) After etching

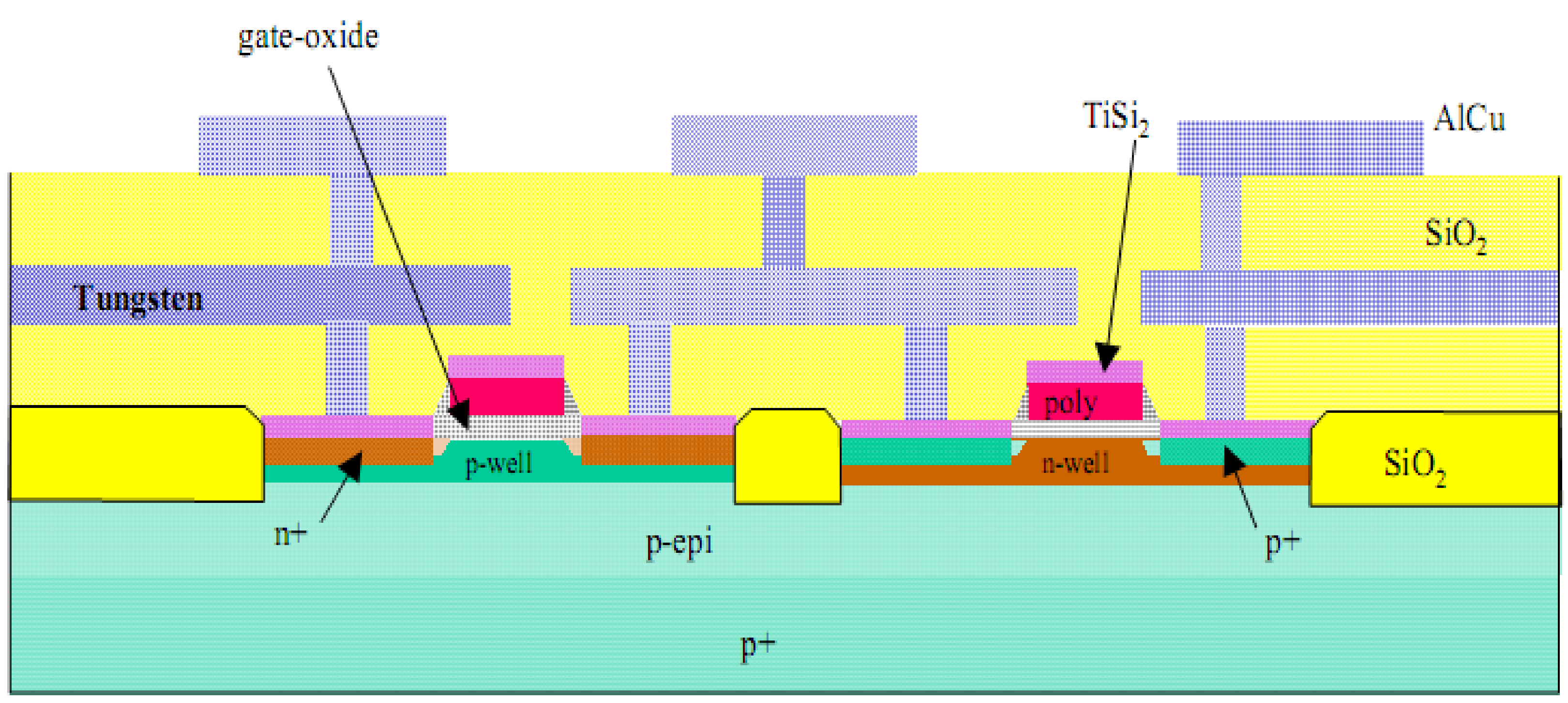


(f) Final result after removal of resist

Advanced Metallization

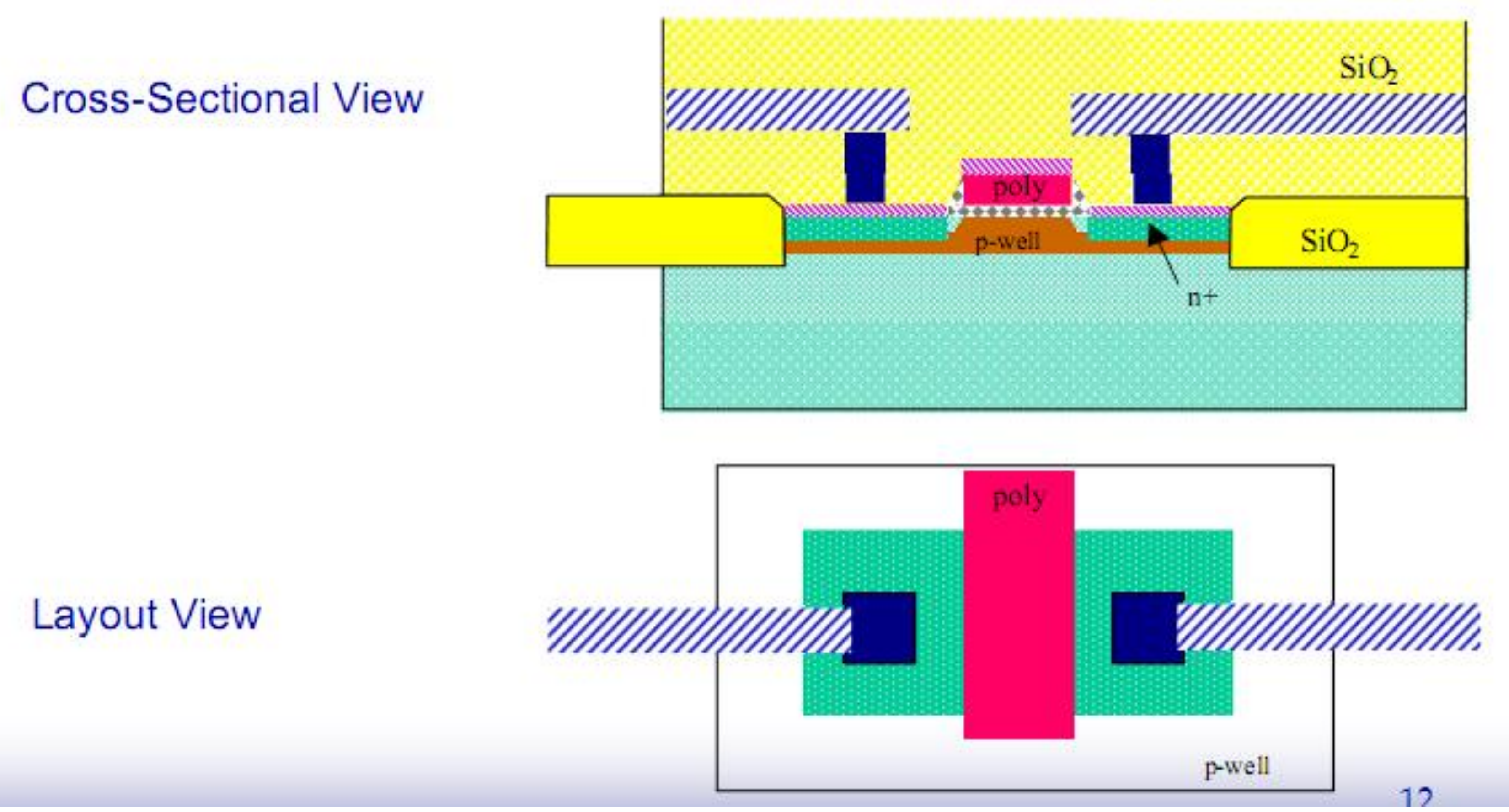


A "Modern" CMOS Process



Dual-Well Shallow-Trench-Isolated CMOS Process

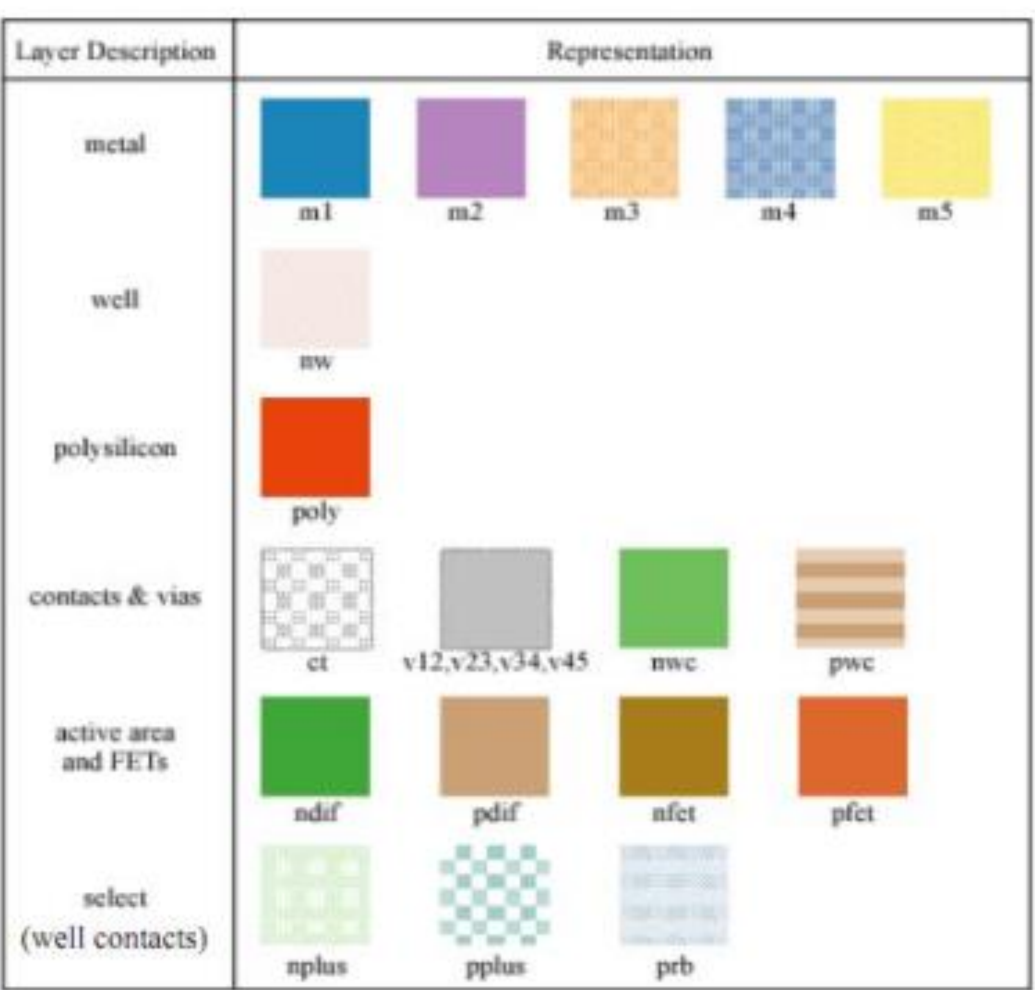
Transistor Layout



CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Well contact (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Layers in 0.25 μm CMOS process



Layer Description	Representation
metal	m1, m2, m3, m4, m5
well	nw
polysilicon	poly
contacts & vias	ct, v12,v23,v34,v45, nwc, pwc
active area and FETs	ndif, pdif, nfet, pfet
select (well contacts)	nplus, pplus, prb

Design Rules

- Intra-layer
  - Widths, spacing, area
- Inter-layer
  - Enclosures, distances, extensions, overlaps
- Special rules (sub-0.25μm)
  - Antenna rules, density rules, (area)

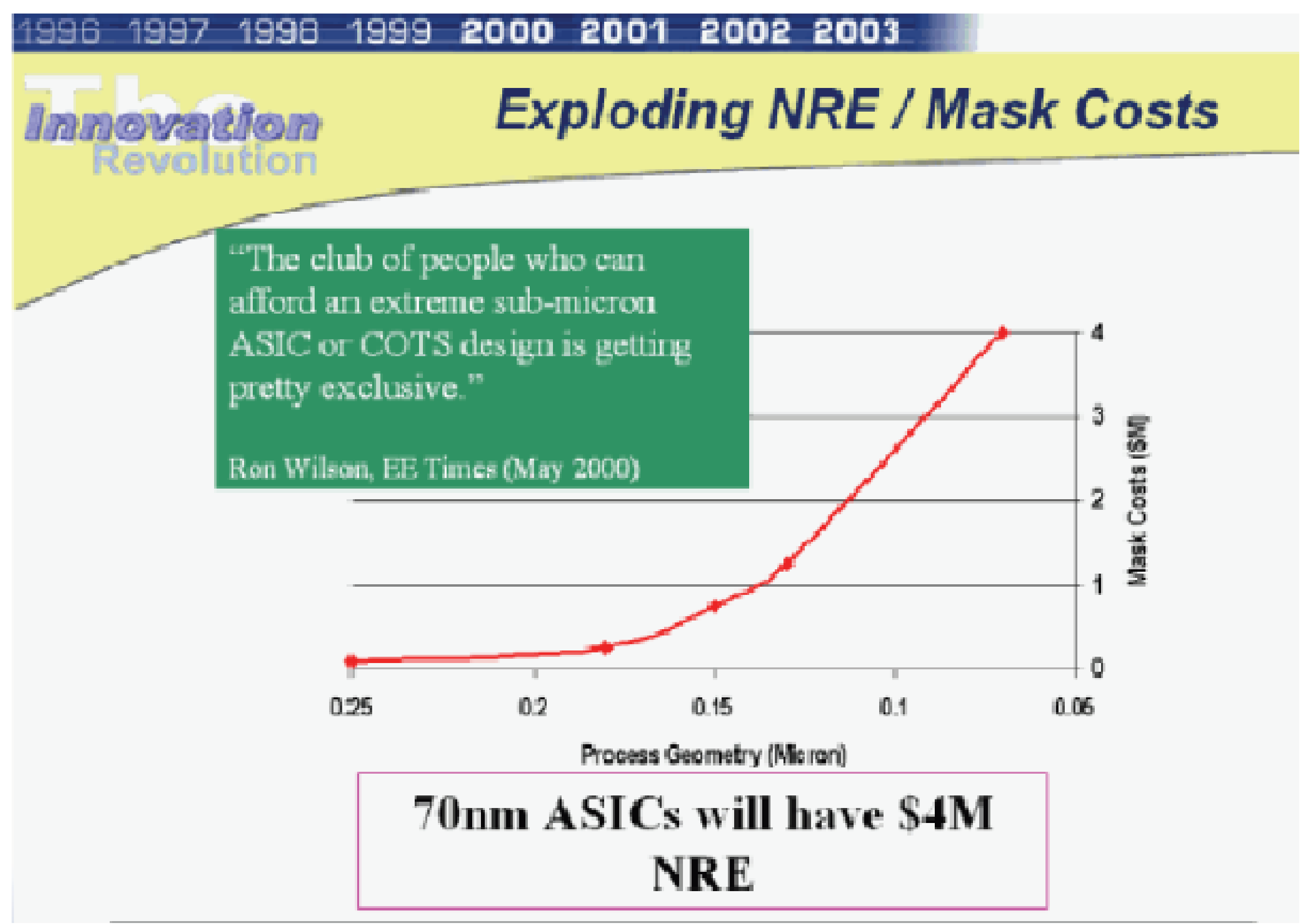
Design Rules

- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions: micron rules
- Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- A complete set includes
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers

Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs - fixed
  - Independent of volume (i.e., number of units made/sold)
  - Examples: design time and effort, mask generation, equipment, etc.
- Recurrent costs - variable
  - proportional to volume
  - Examples: silicon processing, packaging, test
  - Most of these proportional to chip area

NRE Cost is Increasing



Total Cost

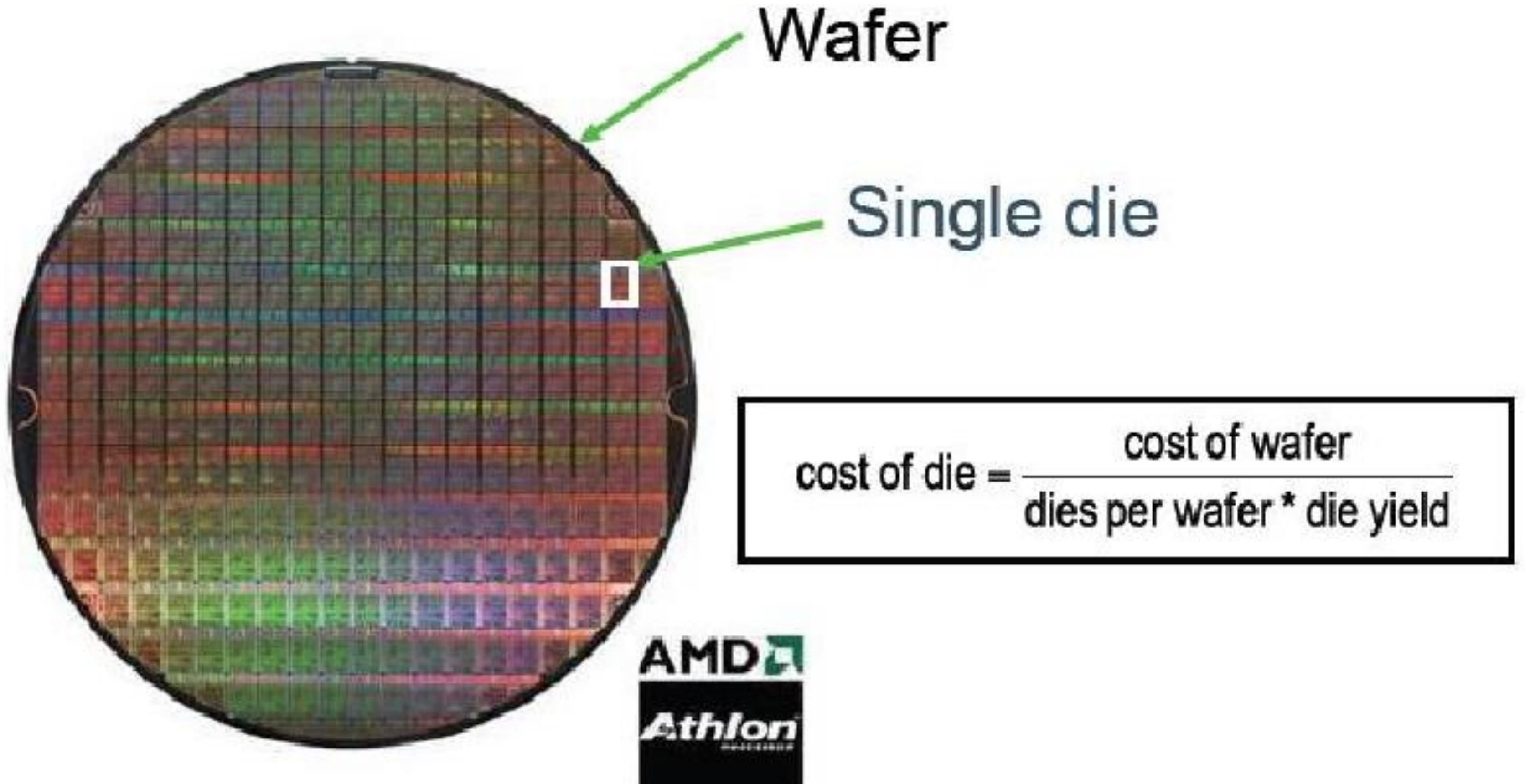
- Cost per IC

$$\text{cost per IC} = \text{variable cost per IC} + \frac{\text{fixed cost}}{\text{volume}}$$

- Variable cost

$$\text{variable cost} = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}$$

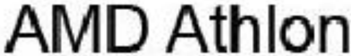
Die Cost

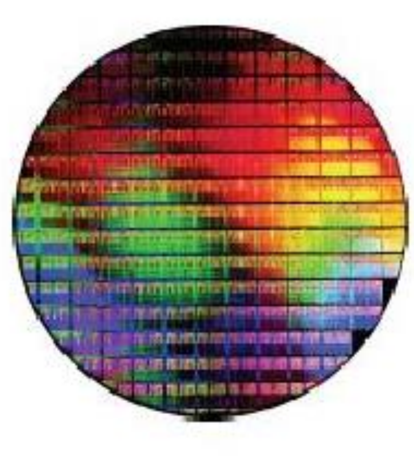


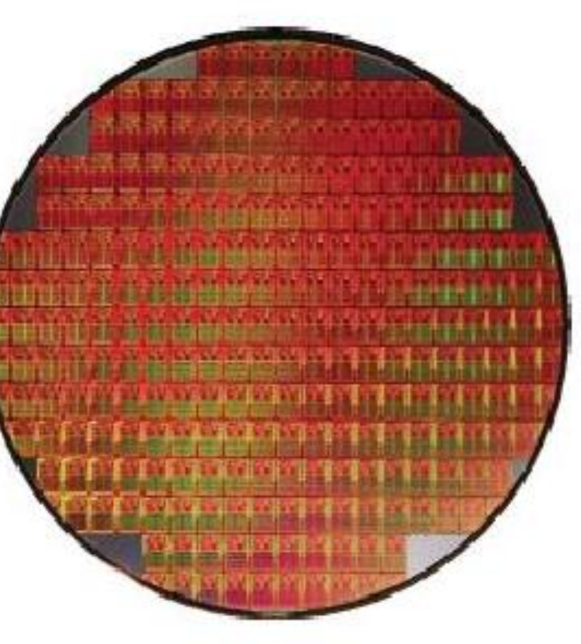
$$\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} * \text{die yield}}$$

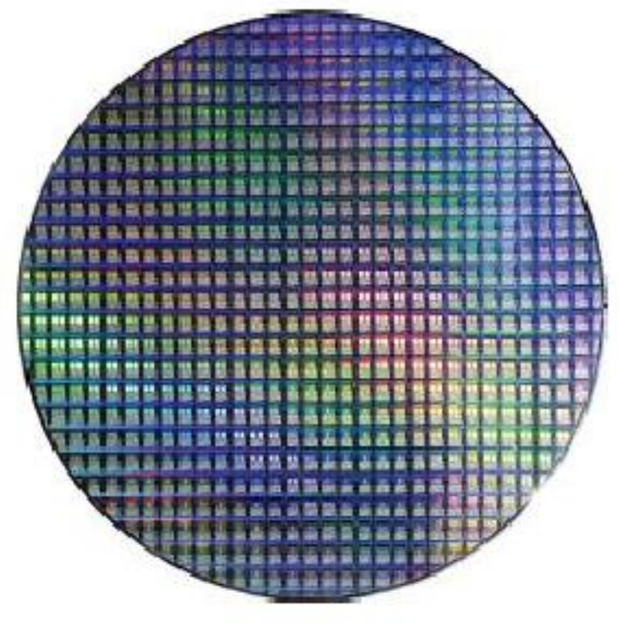
From: http://www.amd.com

Wafer size









8" (200mm)
90nm CMOS

12" (300mm)
90nm CMOS

12" (300mm)
65nm CMOS

Next: 18" Wafers?

Projected 2000 Wafer, circa 1975

Moore was not always accurate

G. Moore, Keynote Address ISSCC 2003

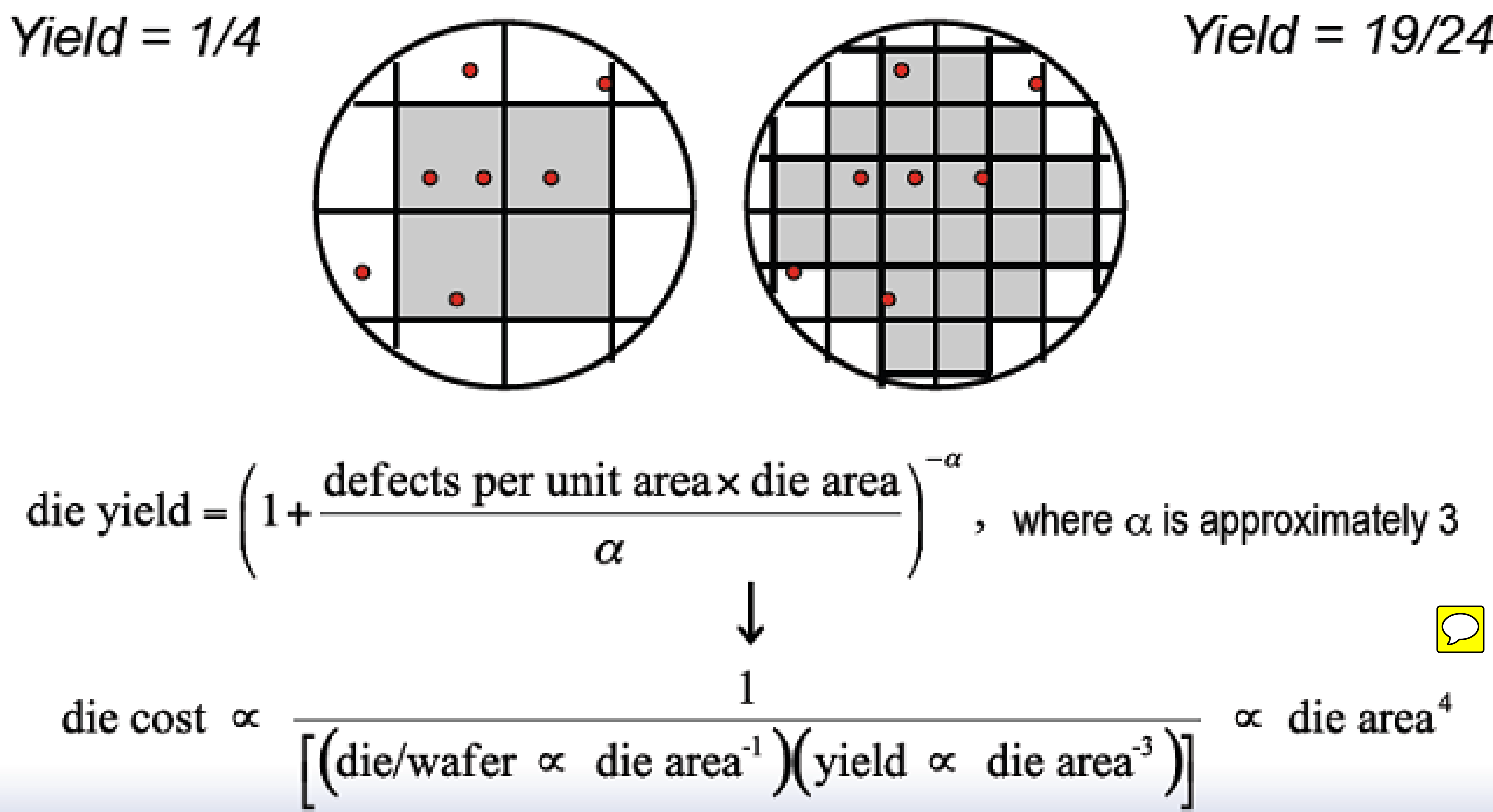
Yield

$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

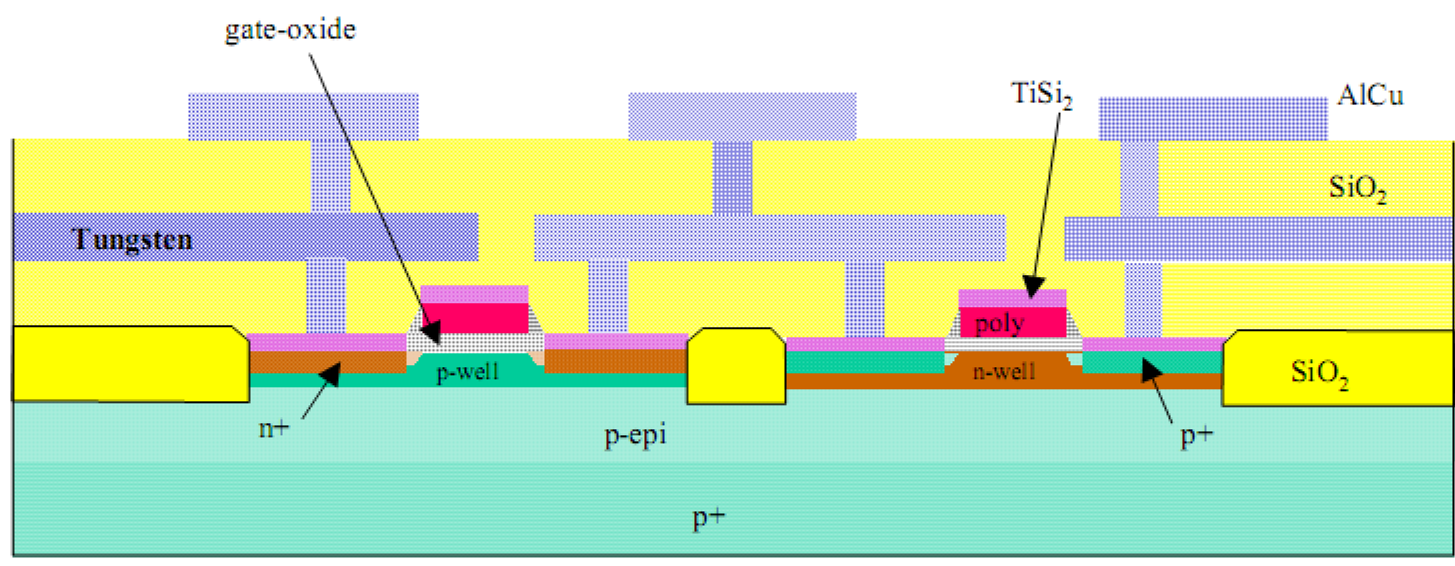
$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$

Defects



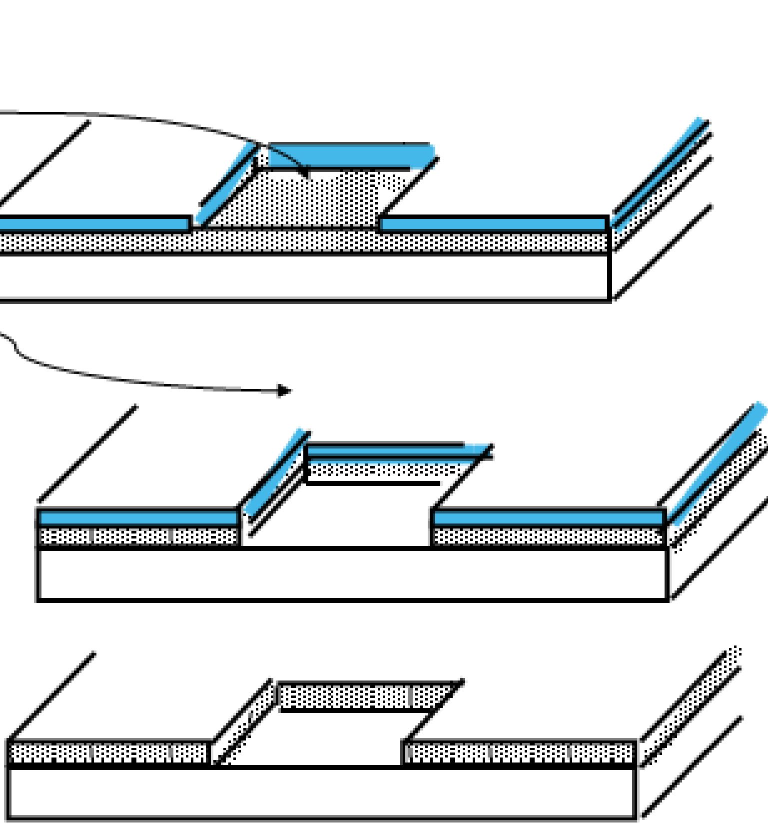
A "Modern" CMOS Process



Dual-Well Shallow-Trench-Isolated CMOS Process

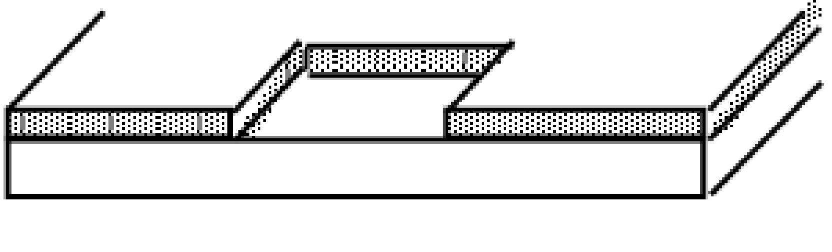
Patterning – Photolithography

1. Oxidation
2. Photoresist (PR) coating
3. Stepper exposure
4. Photoresist development and bake
5. Acid etching
   Unexposed (negative PR)
   Exposed (positive PR)
6. Spin, rinse, and dry
7. Processing step
   Ion implantation
   Plasma etching
   Metal deposition
8. Photoresist removal (ashing)

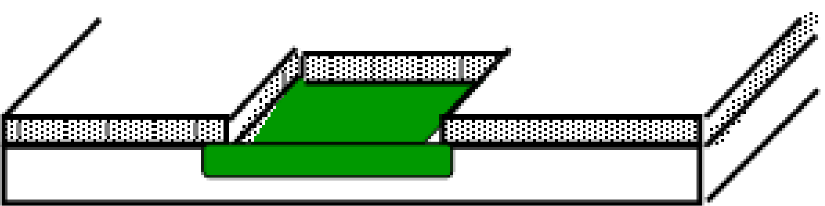


Diffusion and Ion Implantation

1. Area to be doped is exposed (photolithography)



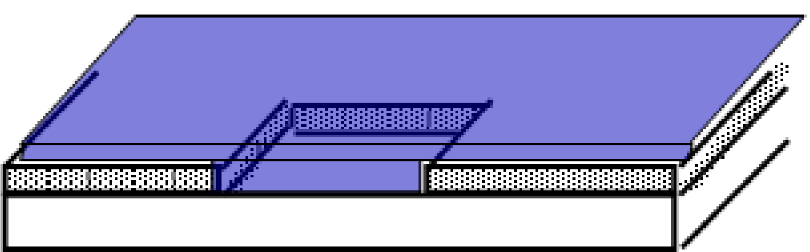
2. Diffusion
   or
   Ion implantation



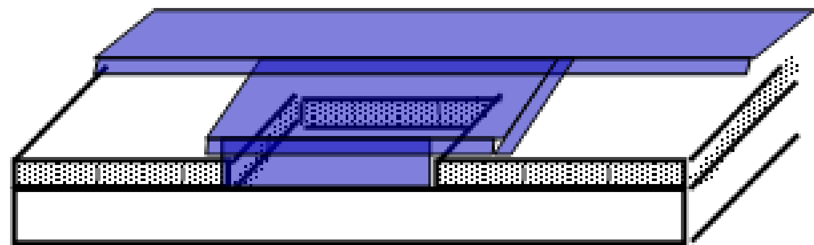
Deposition and Etching

1. Pattern masking (photolithography)

2. Deposit material over entire wafer
   - CVD (Si_3N_4)
   - chemical deposition (polysilicon)
   - sputtering (Al)



3. Etch away unwanted material
   - wet etching
   - dry (plasma) etching



Deposition and Etching

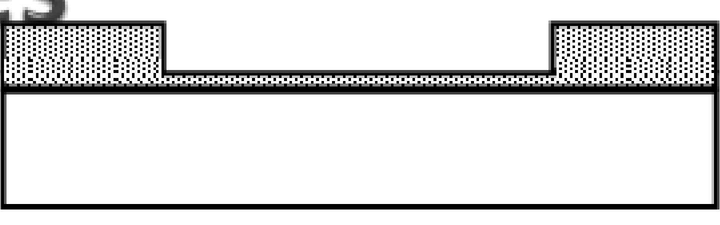
- Needed for insulating SiO2, silicon nitride (sacrificial buffer), polysilicon, metal interconnect
- CVD – chemical vapor deposition uses a gas-phase reaction with energy supplied by heat at around 850C. Use for, eg, silicon nitride
- Chemical deposition – used for polysilicon. flow silane gas over the heated wafer (coated with SiO2) at approx. 650C. Resulting reaction produces a non-crystaline material – polysilicon. Followed by an implant step to increase its conductivity.
- Sputtering – used for aluminum. Al evaporated in a vacuum, heat for evaporation delivered by e-beam bombarding.
- Etching is then used to selectively form patterns (wires, contact holes). Wet etching using acid or basic solutions – hydrofluoric acid buffered with fluoride is used to etch SiO2. Plasma etching becoming more common. Use plasma molecules in heated chamber to "sandblast" the surface. Gives well-defined directionality to the etching action, creating patterns with sharp vertical contours.

Planarization: Polishing the Wafers

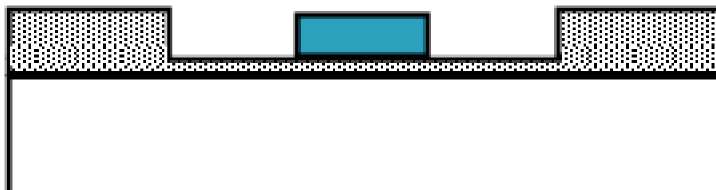
From *Smithsonian*, 2000

Self-Aligned Gates

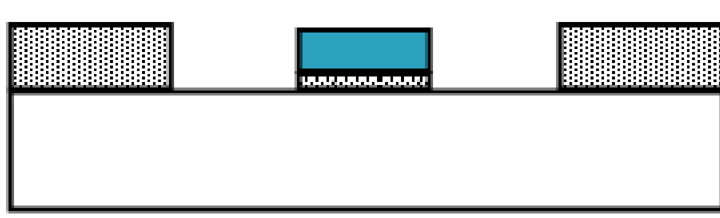
1. Create thin oxide in the "active" regions, thick elsewhere



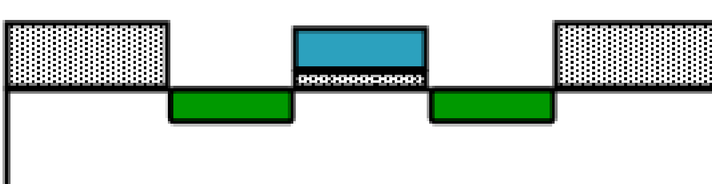
2. Deposit polysilicon



3. Etch thin oxide from active region (poly acts as a mask for the diffusion)



4. Implant dopant

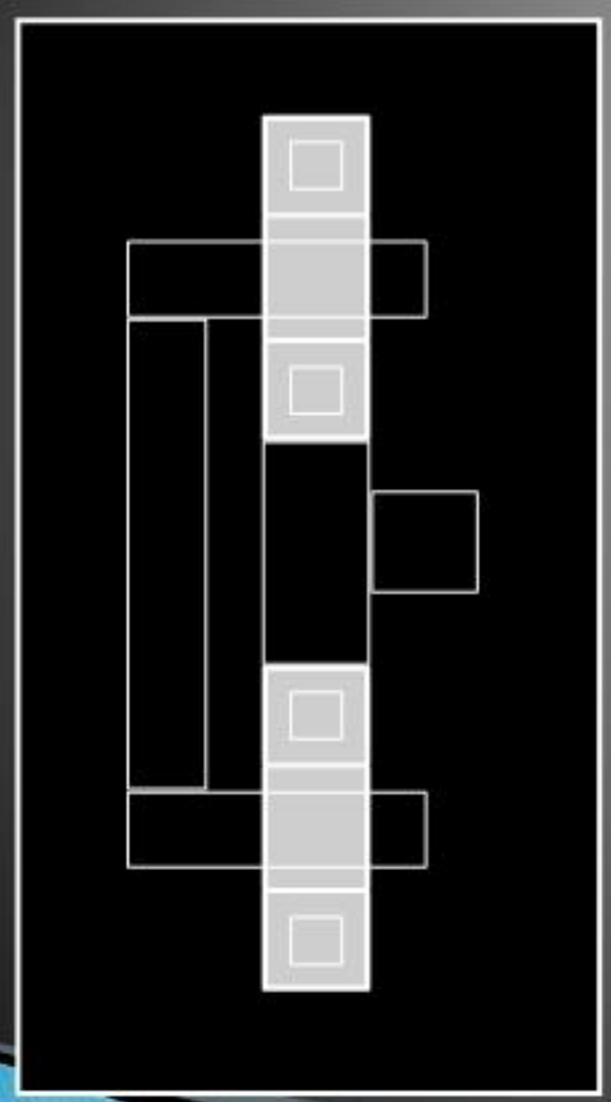


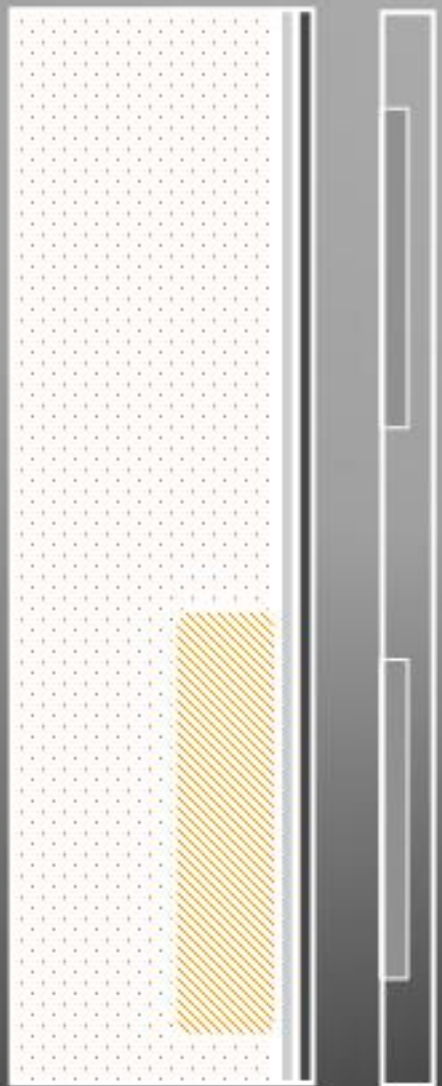
Simplified CMOS Inverter Process

cut line

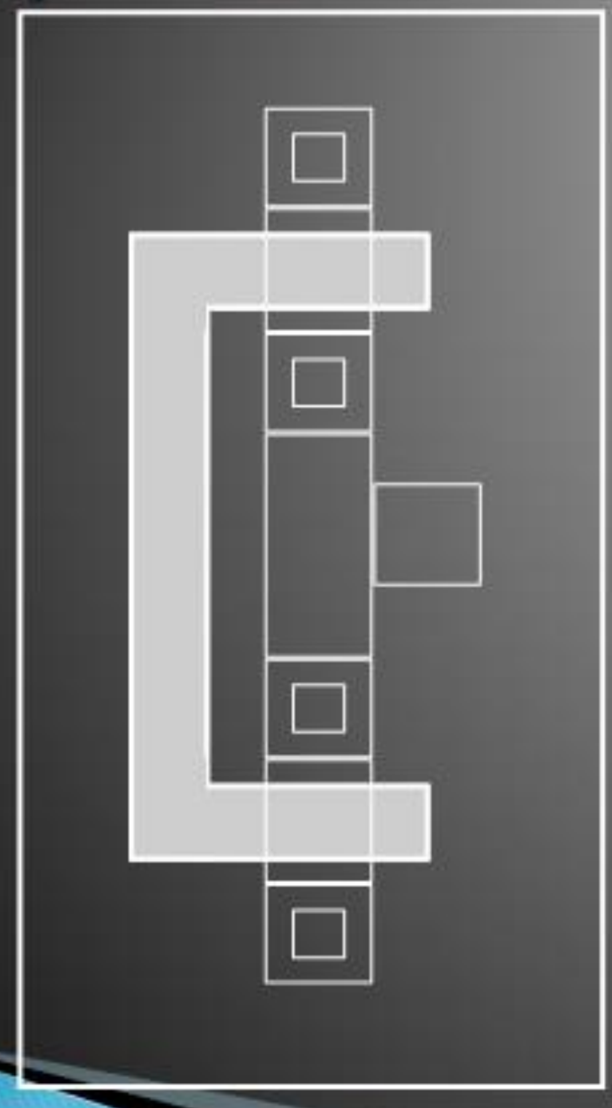
p well

Active Mask

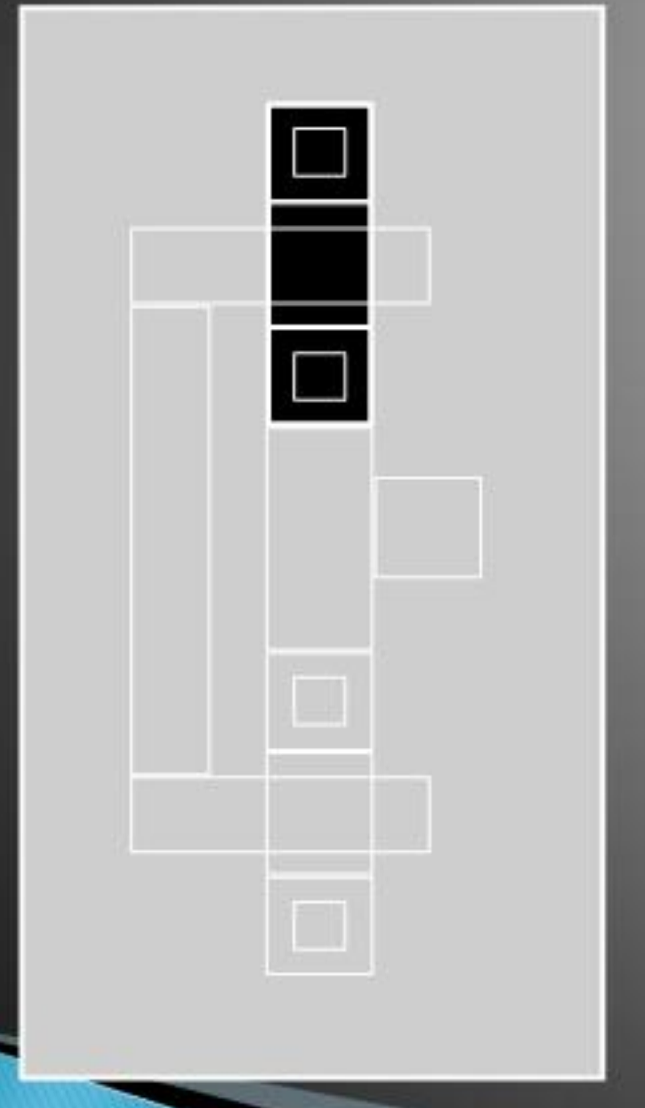


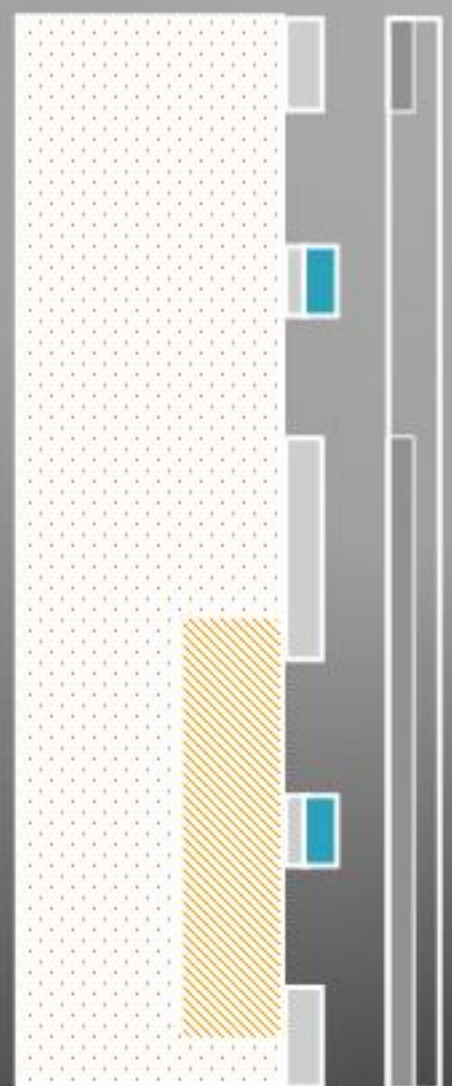


Poly Mask

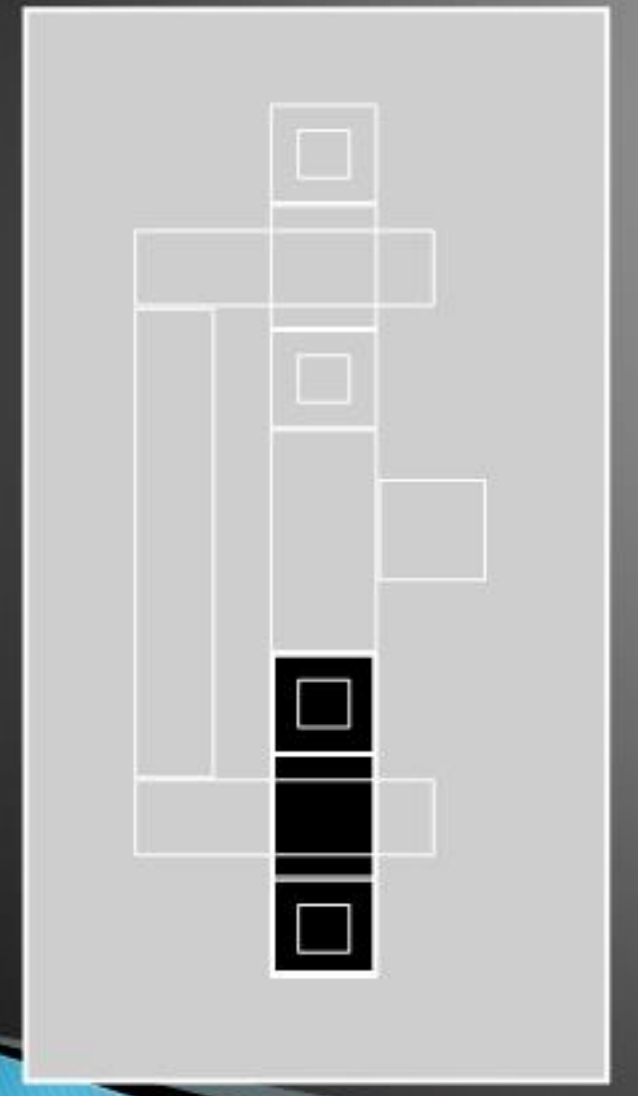


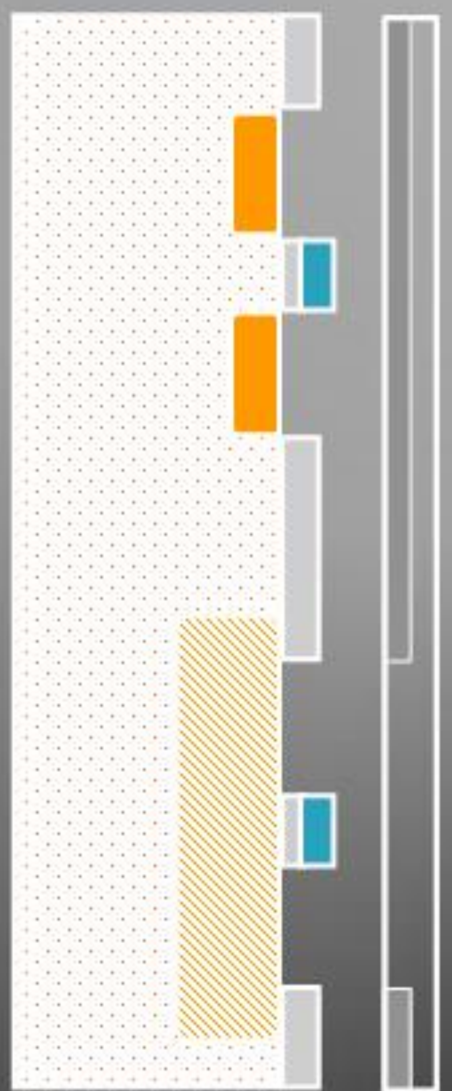
P+ Select Mask



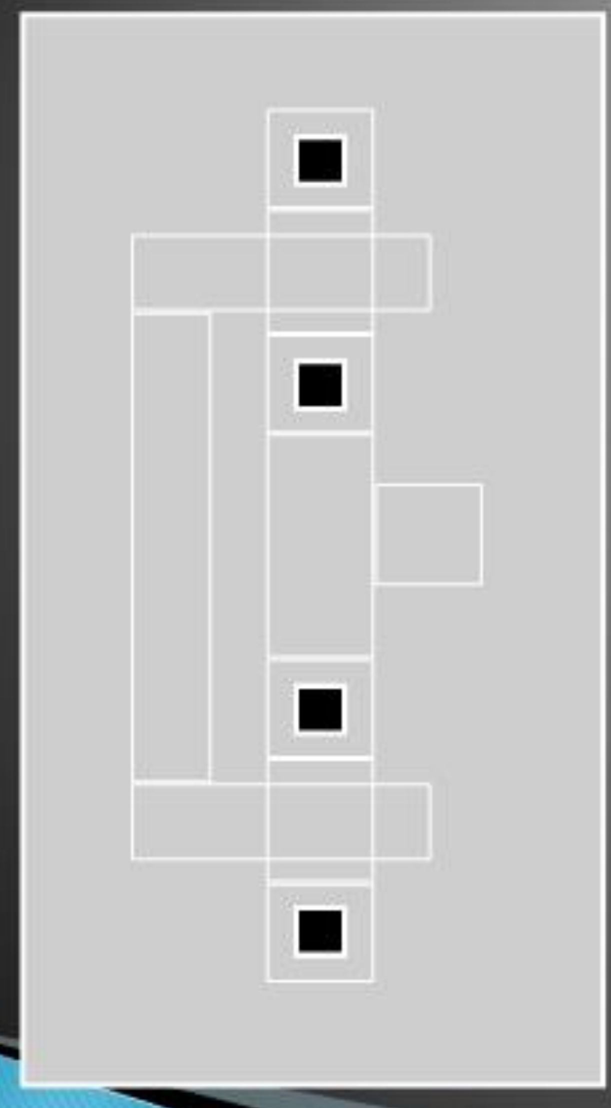


N+ Select Mask

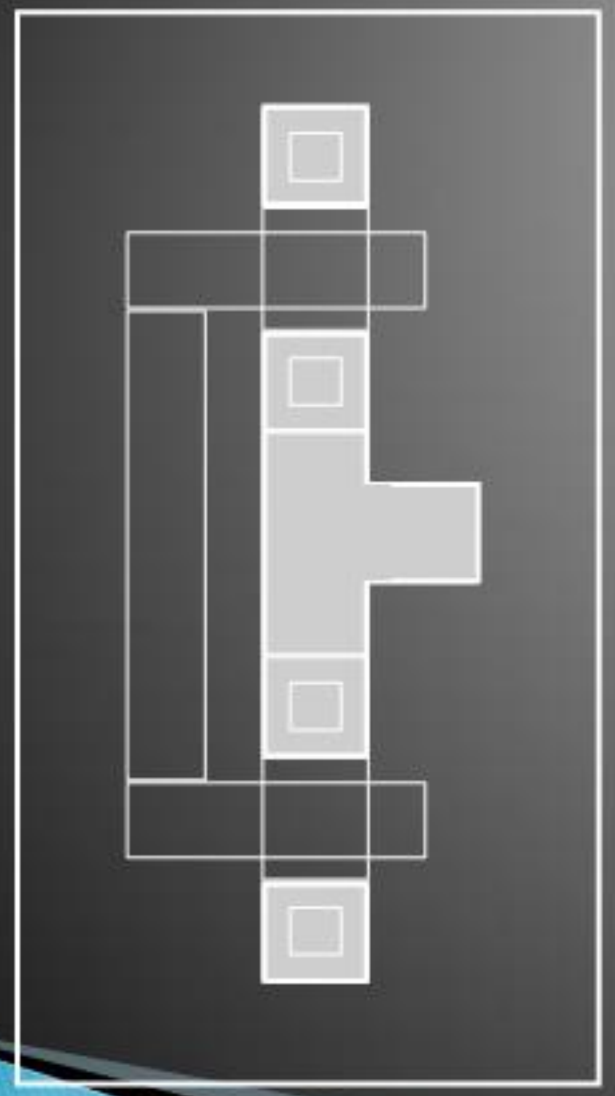


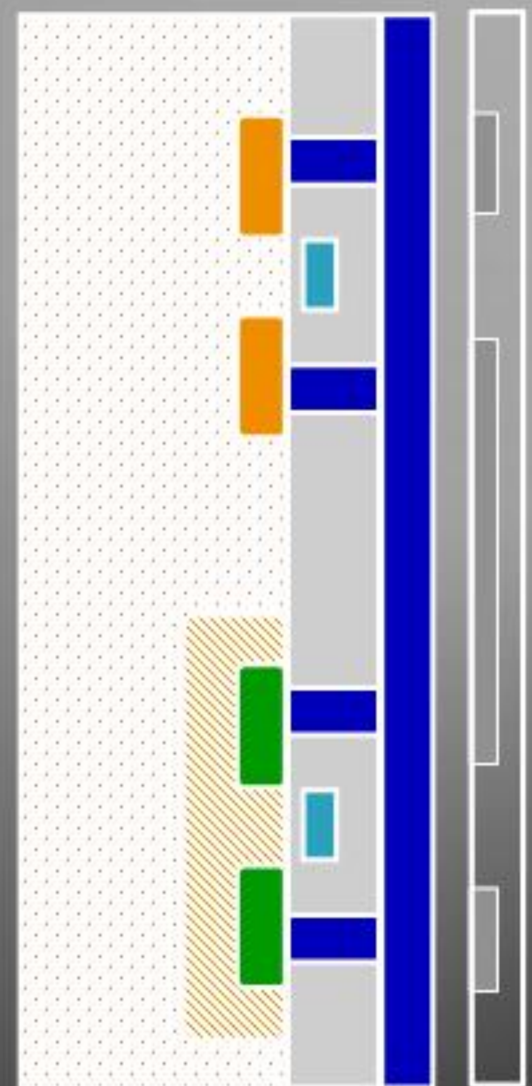


Contact Mask



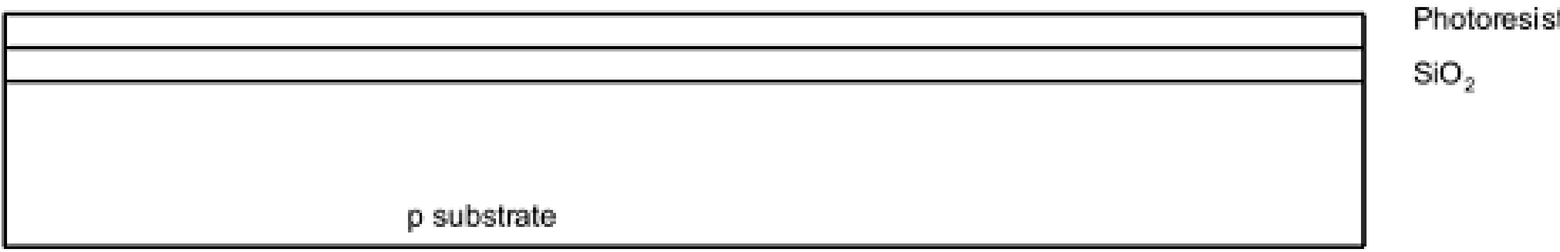
Metal Mask





Deposit silicon-oxide and photoresist

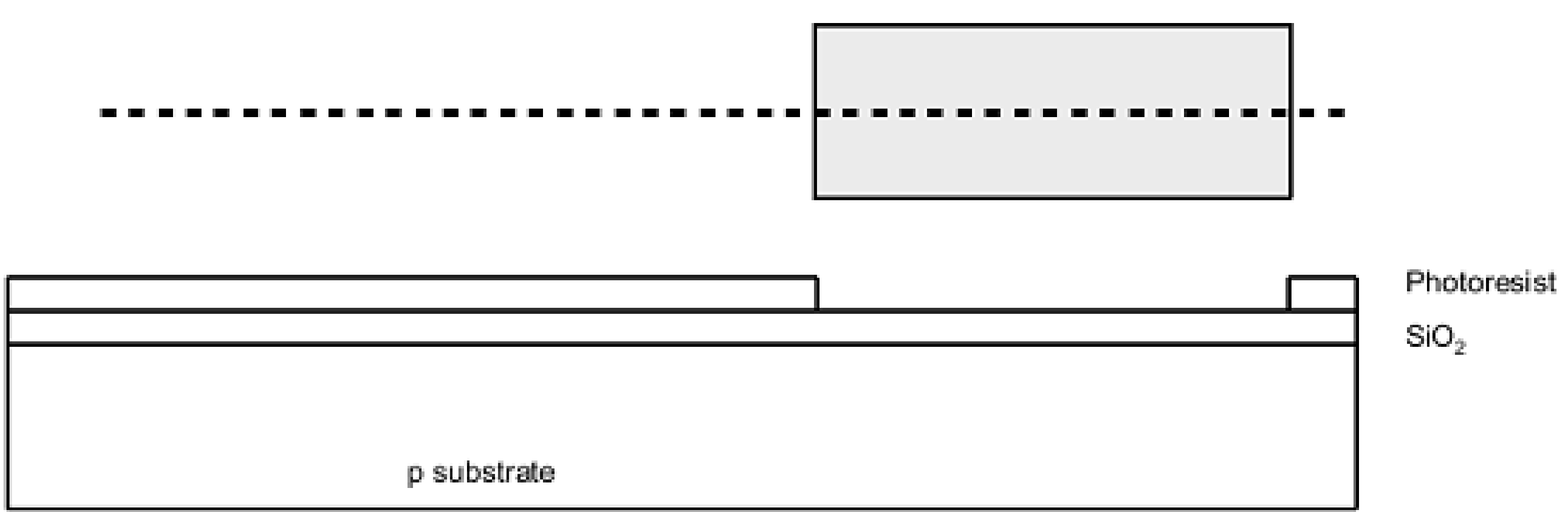
- Photoresist is a light-sensitive organic polymer
- Softens where exposed to light



NOTE: The silicon oxide is just to protect the wafer

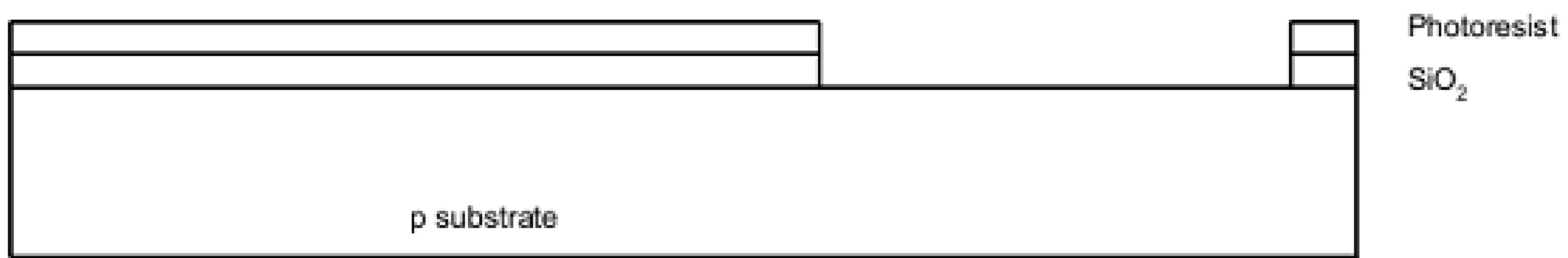
Photo-Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



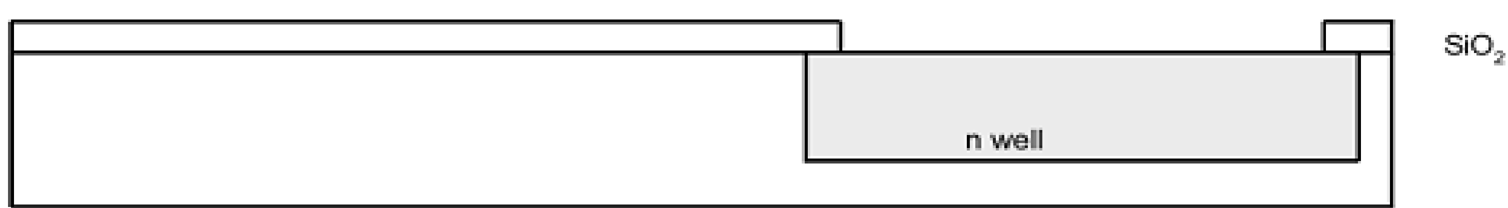
Etching

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone: nasty stuff!!!
- Only attacks oxide where resist has been exposed



The n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si

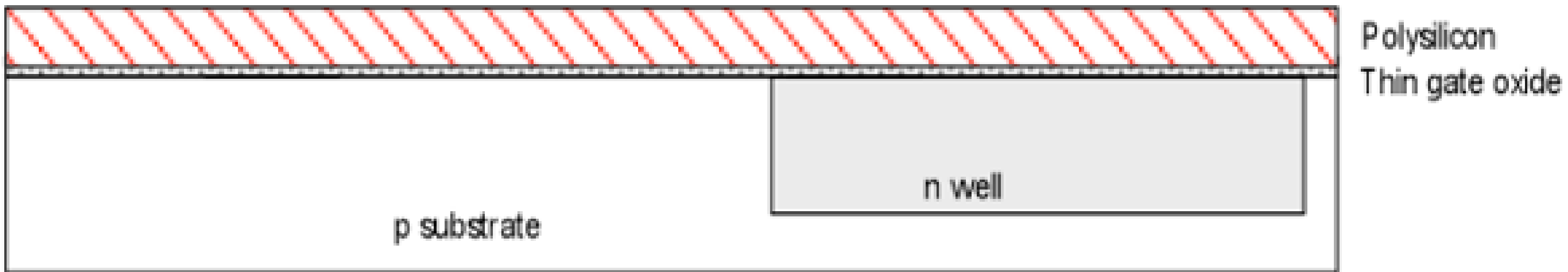


Strip protective oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

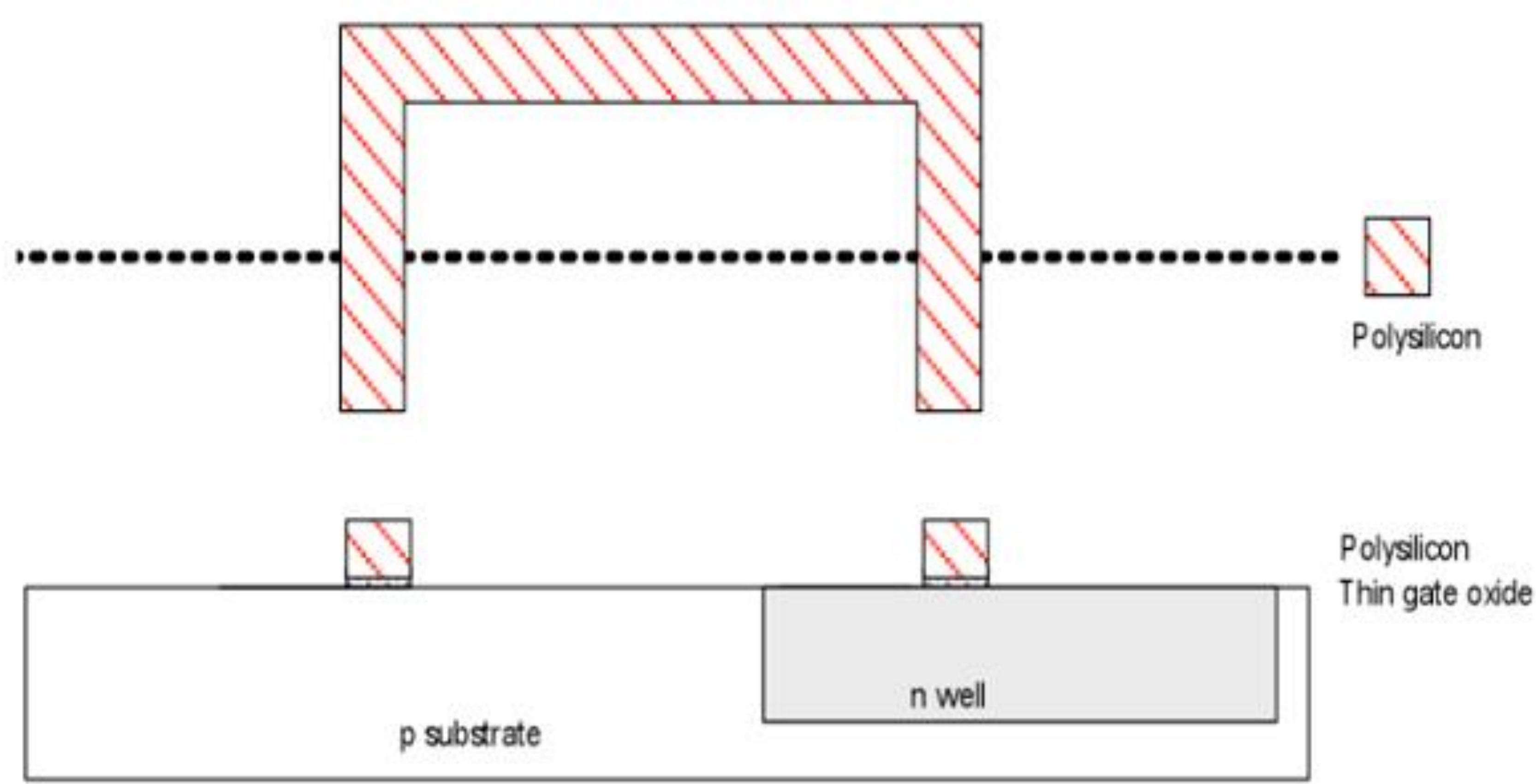
Gate oxide and Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



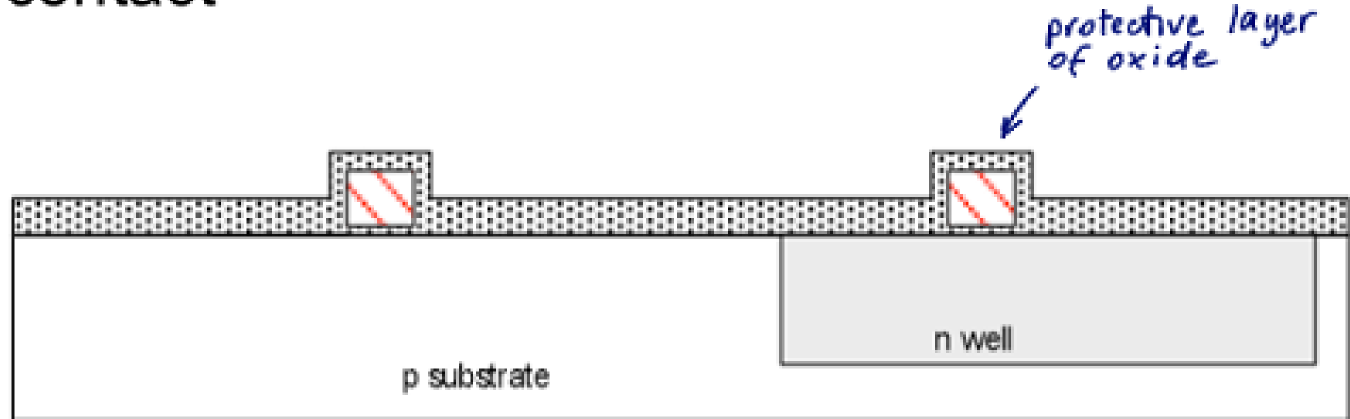
Polysilicon patterning

- Use same lithography process to pattern polysilicon



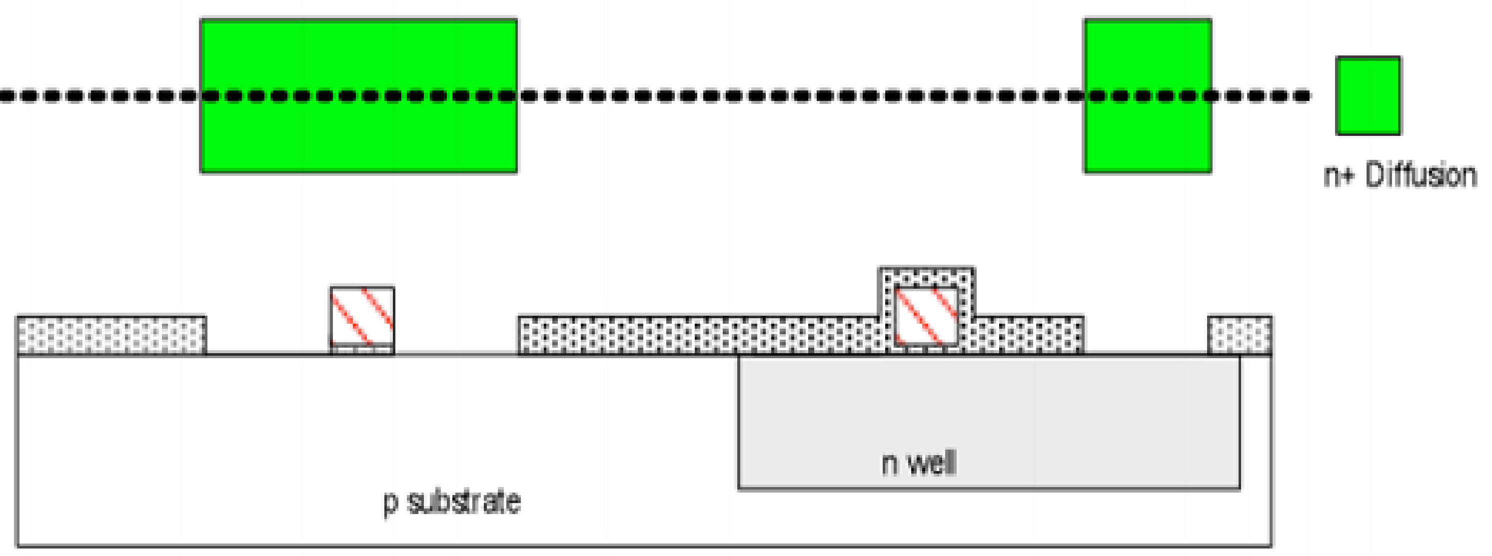
Self-aligned polysilicon gate process

- The polysilicon gate serves as a mask to allow precise alignment of the source and drain with the gate
- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- n-diffusion forms nMOS source, drain, and n-well contact



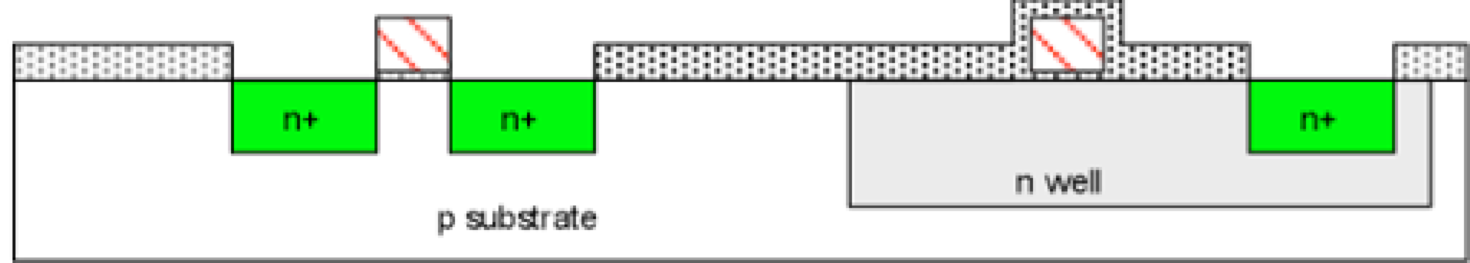
Formation of the n-diffusions

- Pattern oxide and form n+ regions
- *Self-aligned process* (poysilicon gate) “blocks” diffusion under the gate
- Polysilicon is better than metal for self-aligned gates because it doesn’t melt during later processing

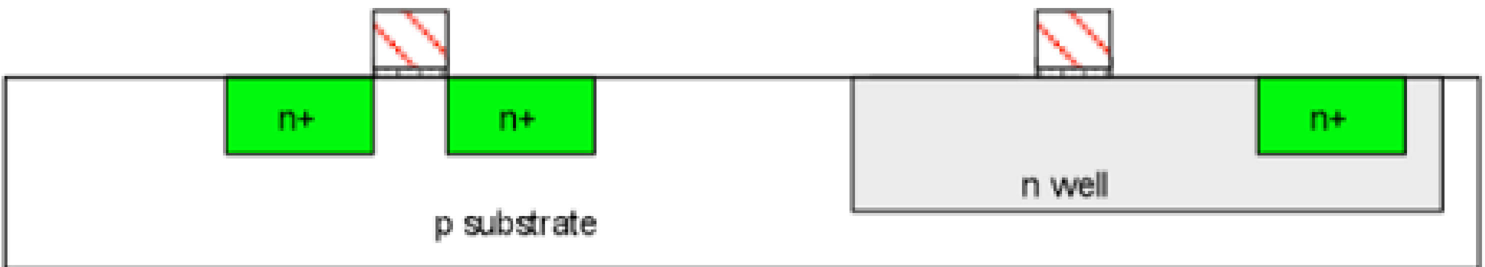


The n-diffusions

- Historically dopants were diffused
- Usually ion implantation today (but regions are still called diffusion)

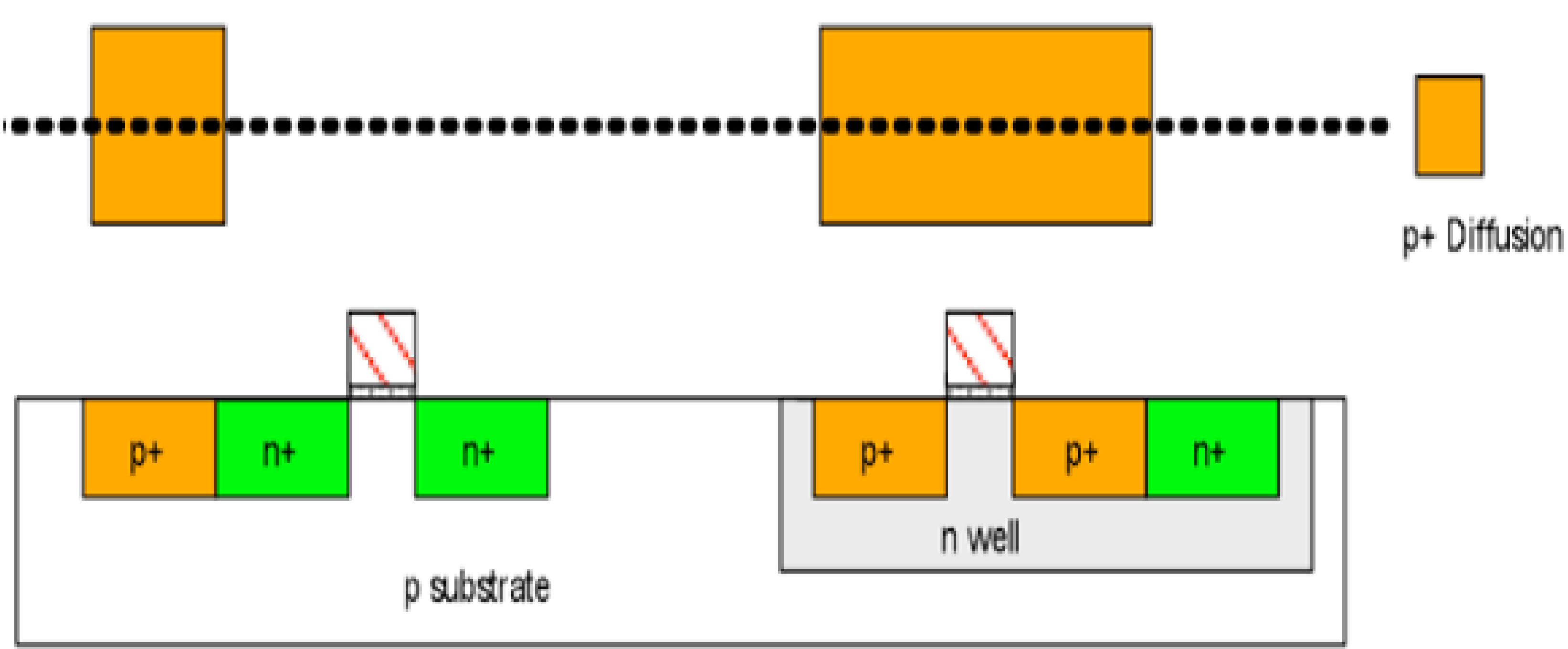


- Strip off oxide to complete patterning step



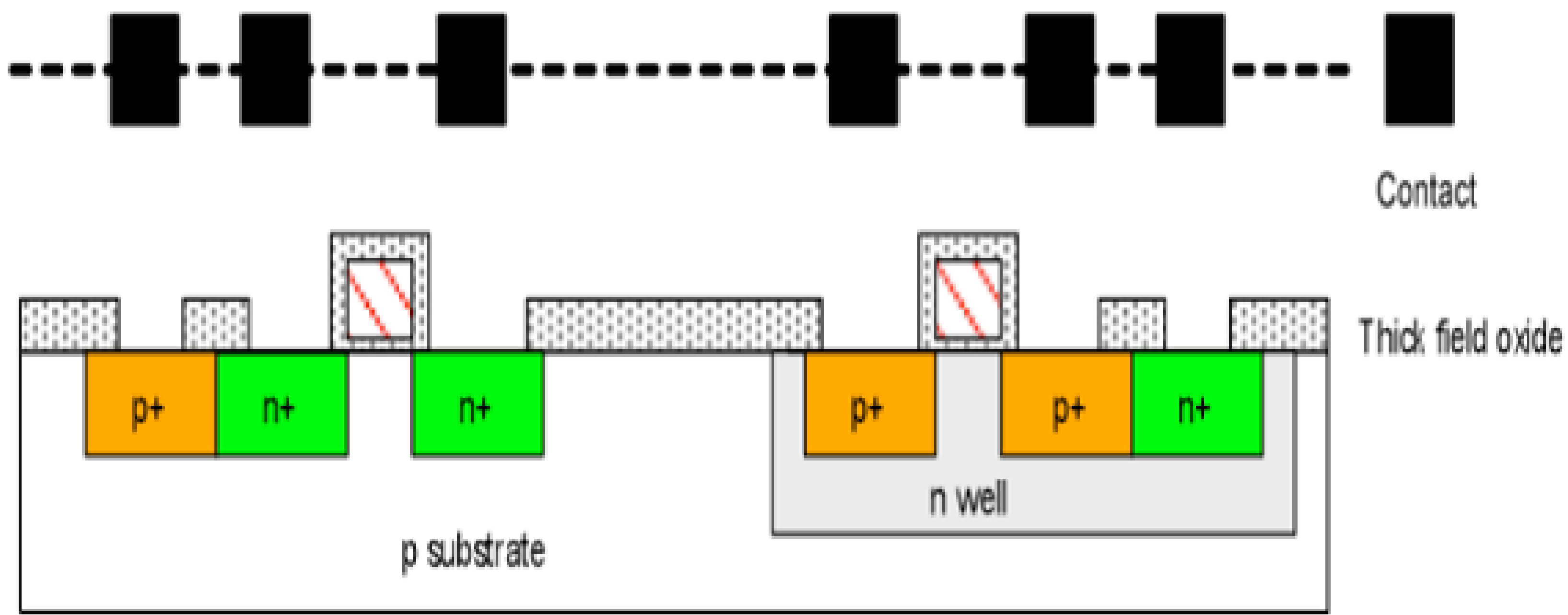
The p-diffusions

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



Contacts

- Now we need to create the devices' terminals
- Cover chip with thick field oxide (FOX)
- Etch oxide where contact cuts are needed



Metallization

- Sputter on aluminum over whole wafer, filling the contacts as well
- Pattern to remove excess metal, leaving wires