# Layout Rules

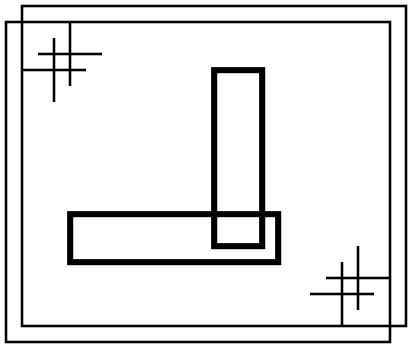
# Design Rules

- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions: micron rules
- Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- A complete set includes
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers

# Why Have Design Rules?

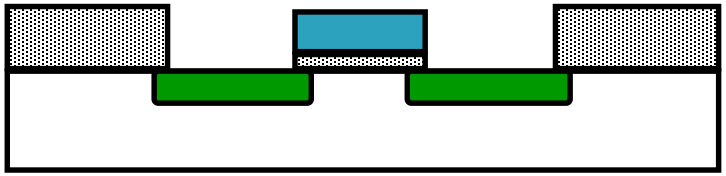
- To be able to tolerate some level of fabrication errors such as

1. Mask misalignment



2. Dust

3. Process parameters (e.g., lateral diffusion)

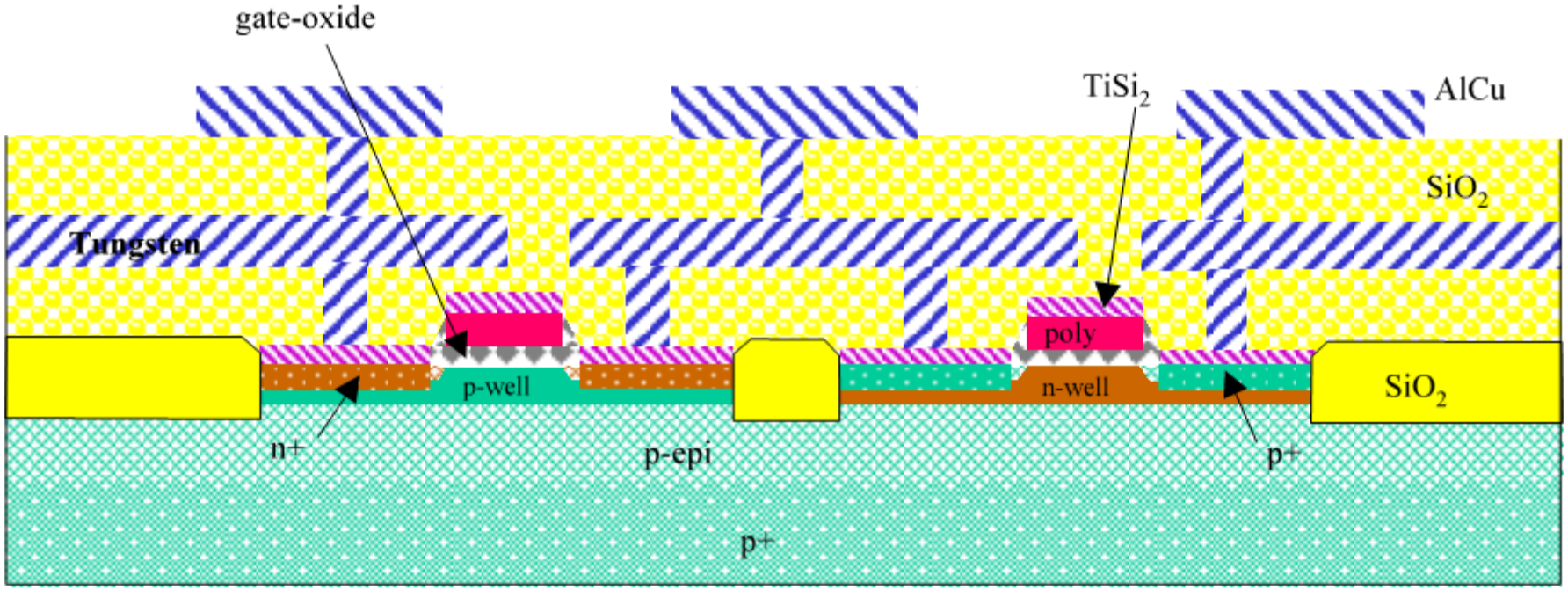


4. Rough surfaces

# Design Rules

- Intra-layer
  - Widths, spacing, area
- Inter-layer
  - Enclosures, distances, extensions, overlaps
- Special rules (sub-0.25μm)
  - Antenna rules, density rules, (area)

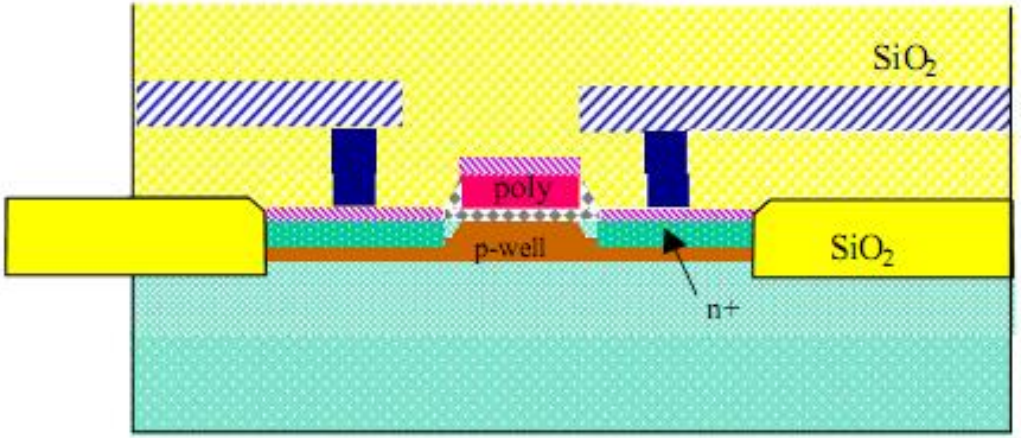
# A Modern CMOS Process



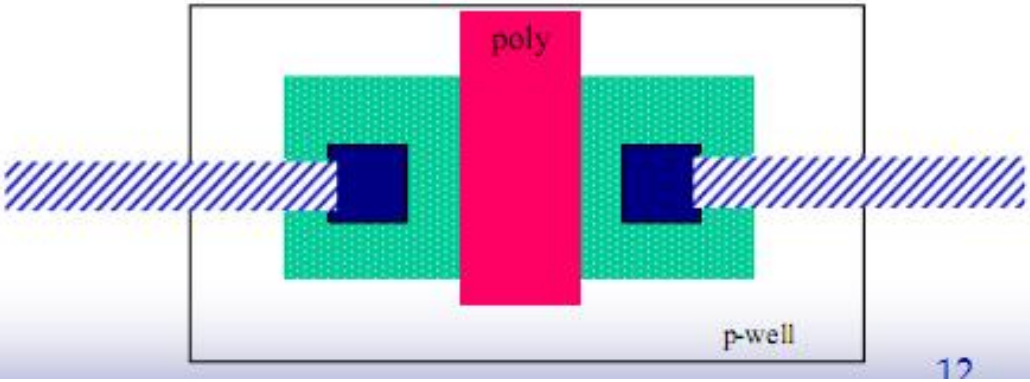

Dual-Well Shallow-Trench-Isolated CMOS Process

# Transistor Layout

Cross-Sectional View

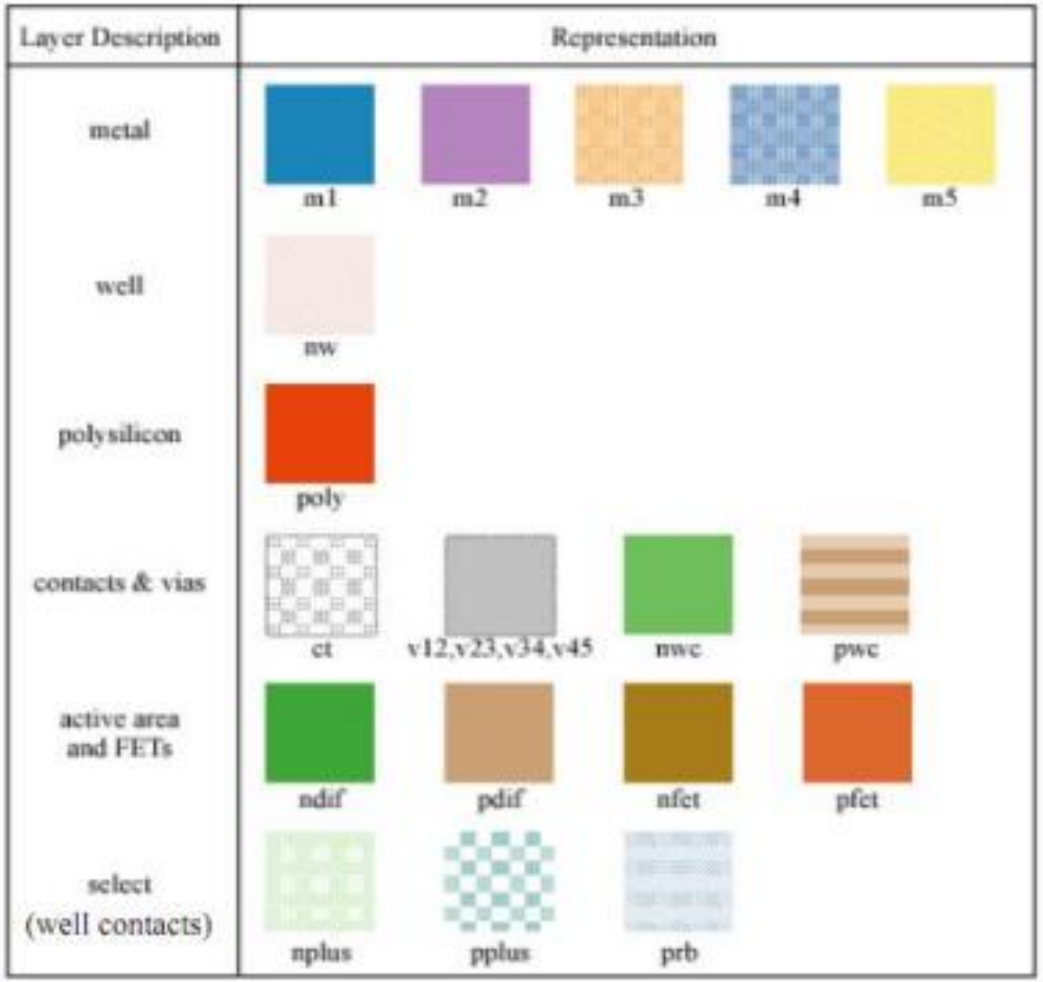



Layout View

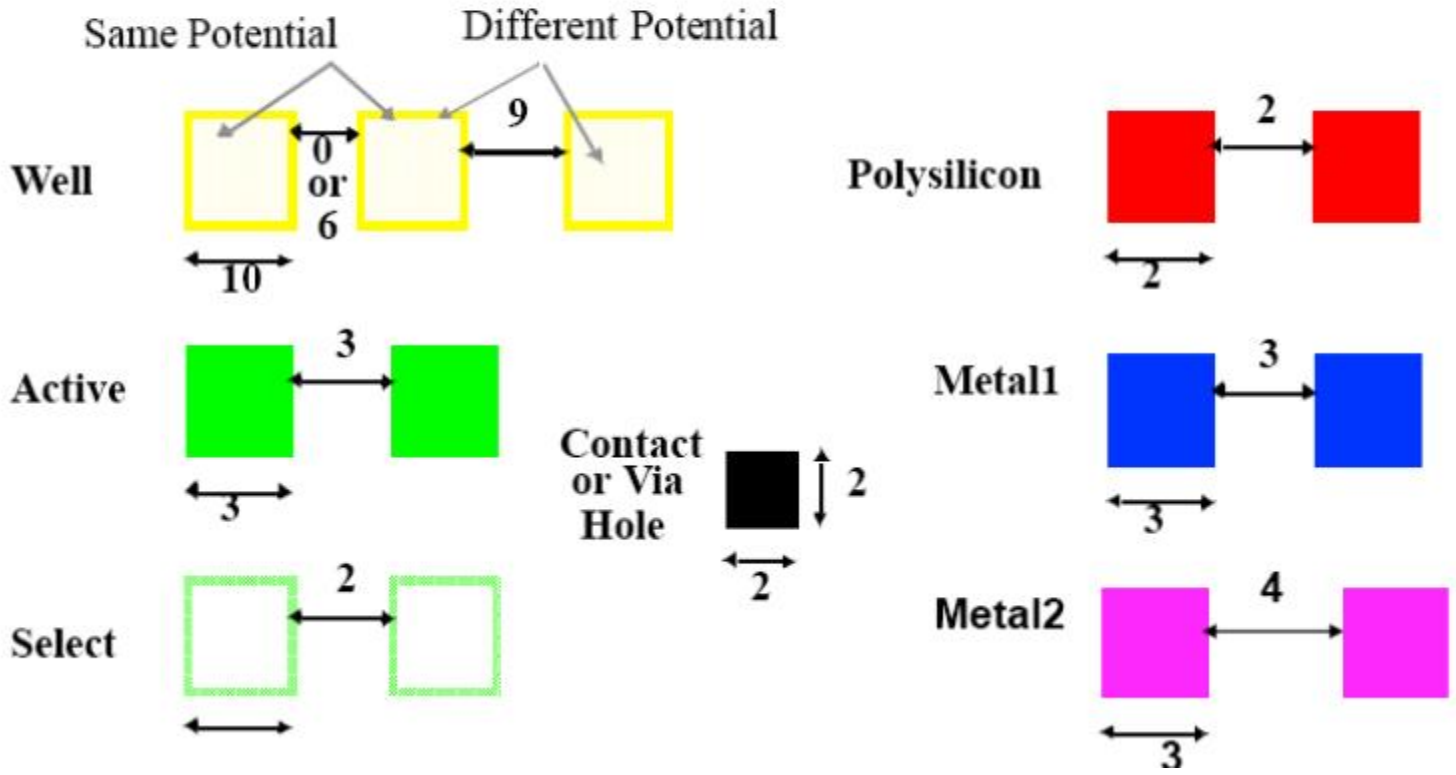



12

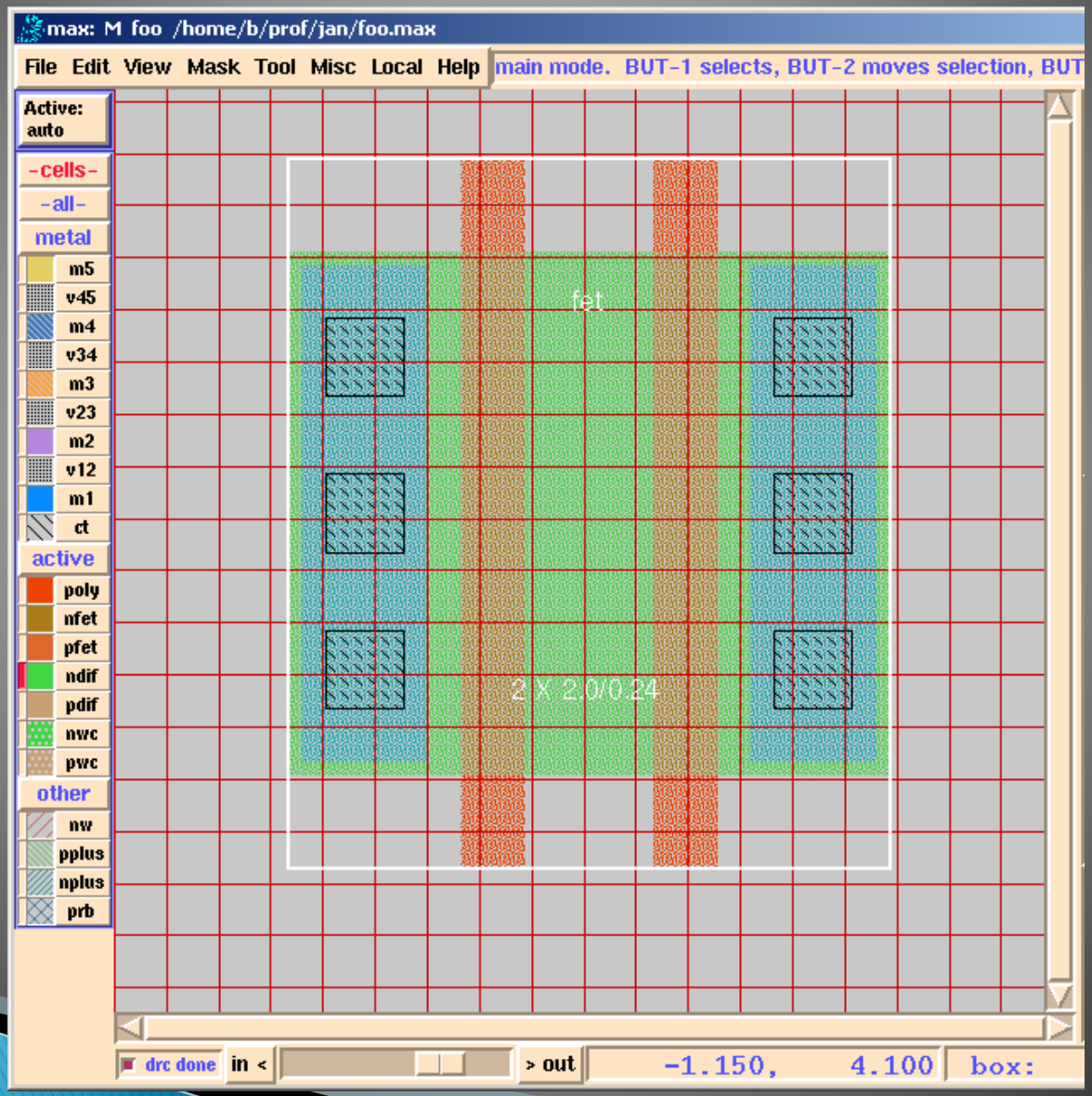
# Layers in 0.25 $\mu$m CMOS process



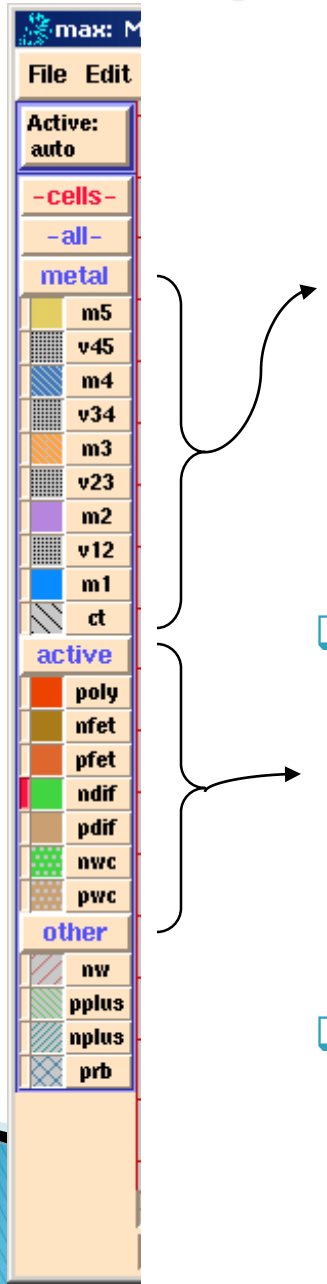
# Intra-Layer Design Rules



# Layout Editor: *max* Design Frame



# *max* Layer Representation

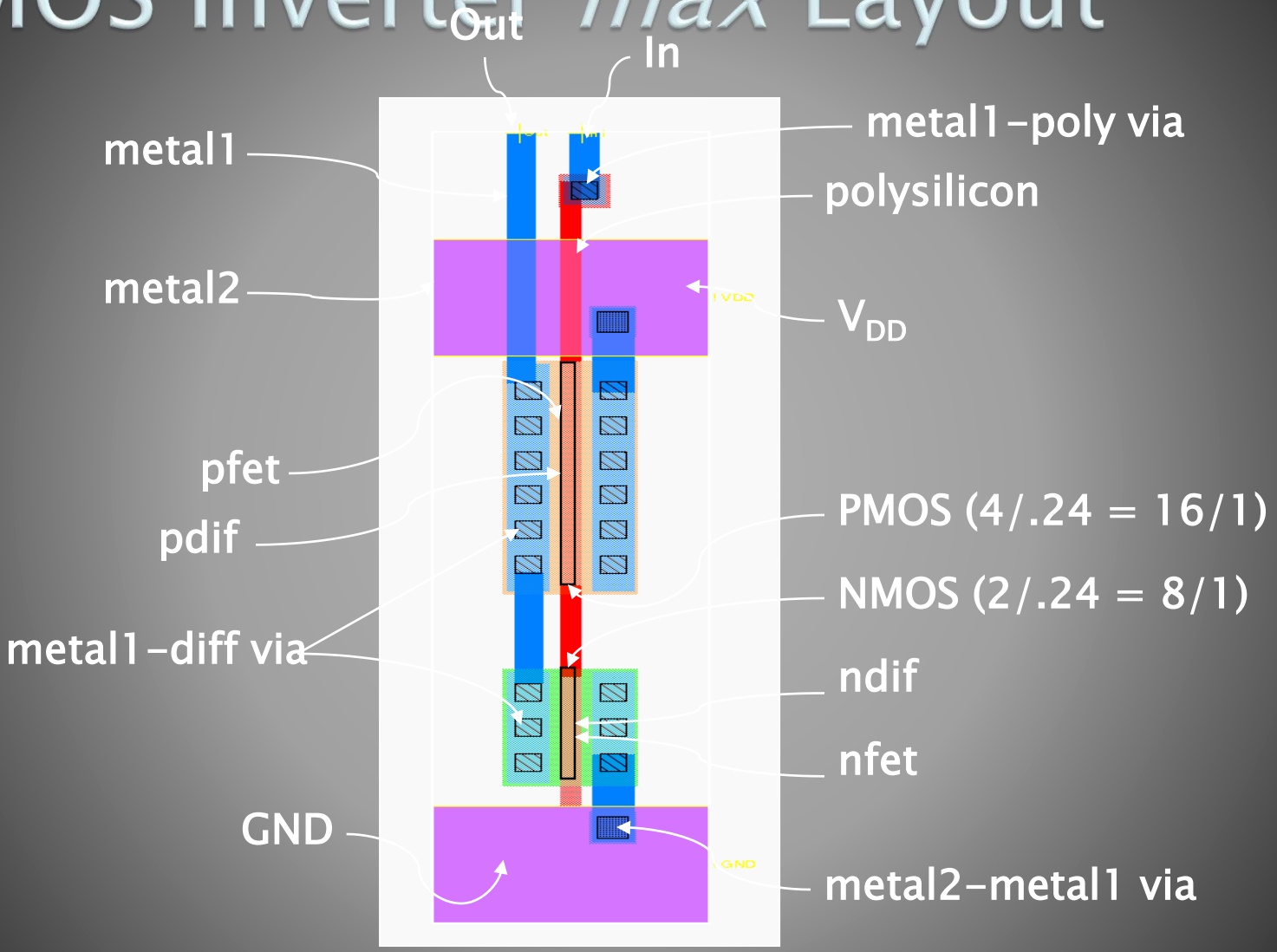



- Metals (five) and vias/contacts between the interconnect levels
  - Note that m5 connects only to m4, m4 only to m3, etc., and m1 only to poly, ndif, and pdif
  - Some technologies support "stacked vias"

- Active – active areas on/in substrate (poly gates, transistor channels (nfet, pfet), source and drain diffusions (ndif, pdif), and well contacts (nwc, pwc))

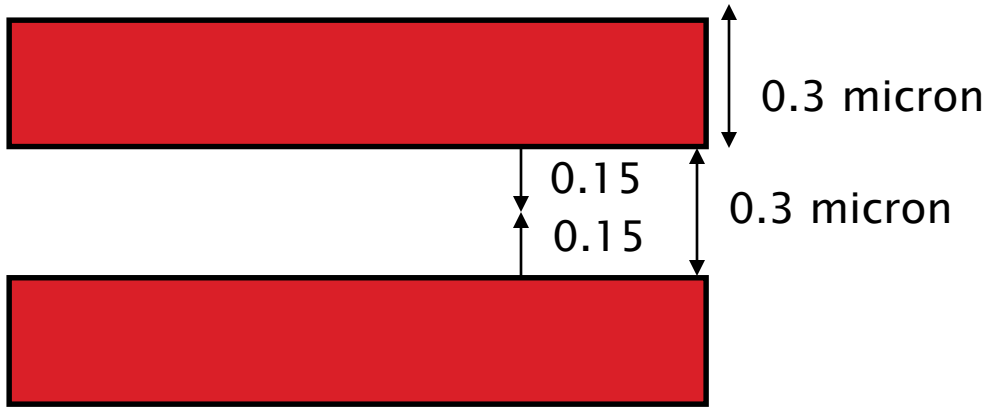
- Wells (nw) and other select areas (pplus, nplus, prb)

# CMOS Inverter *max* Layout



# Intra-Layer Design Rule Origins

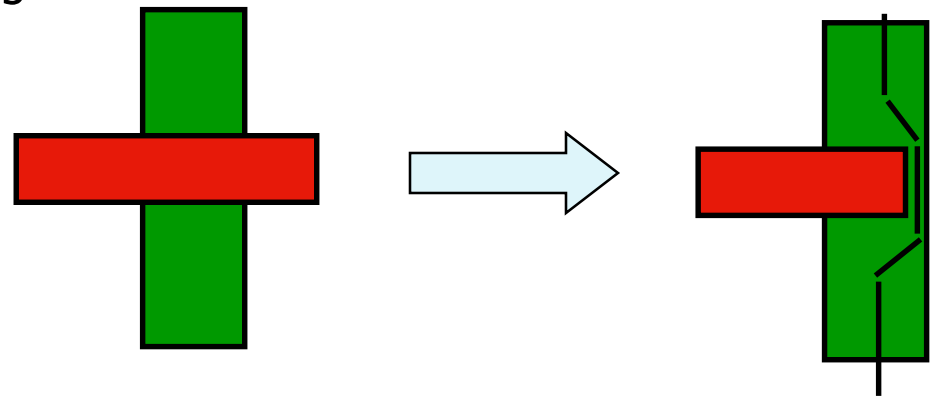
- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab



# Inter-Layer Design Rule Origins

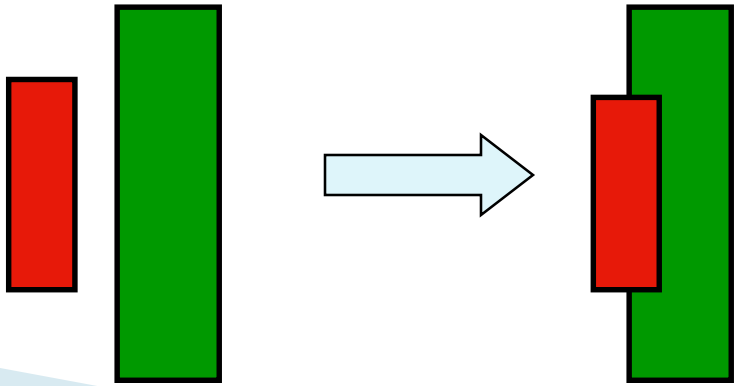
1. Transistor rules – transistor formed by overlap of active and poly layers

Transistors

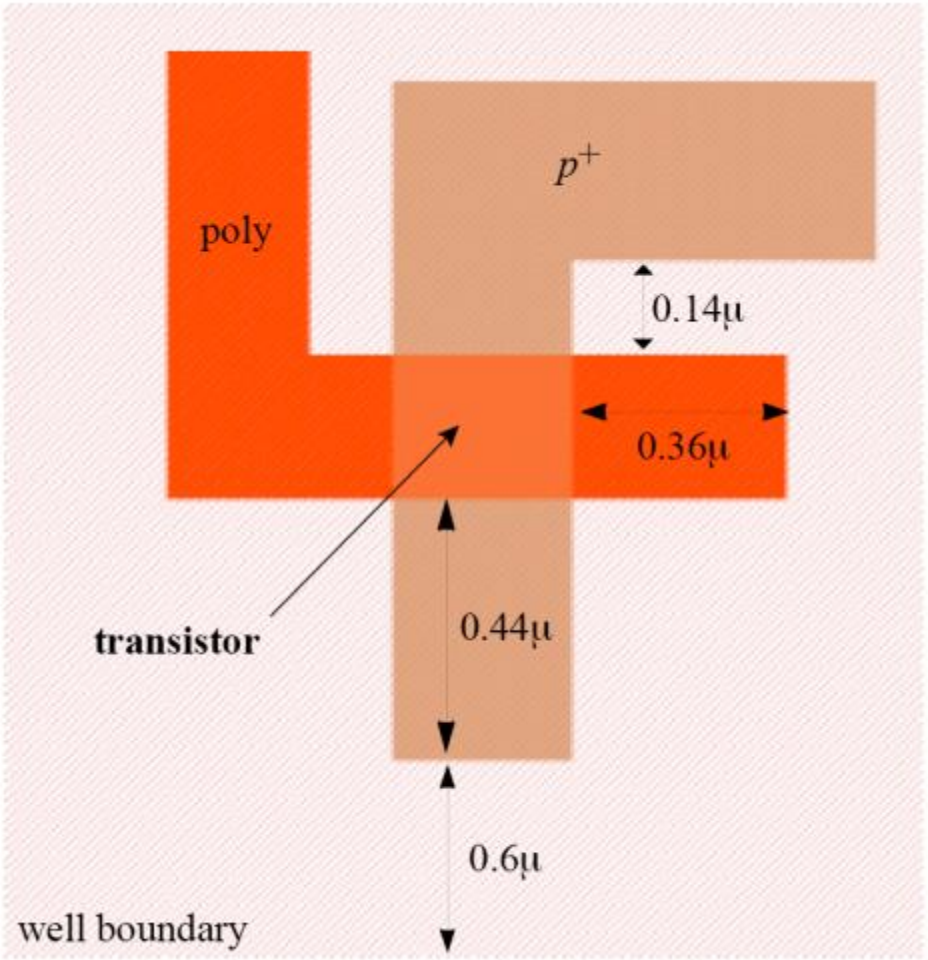


Catastrophic error

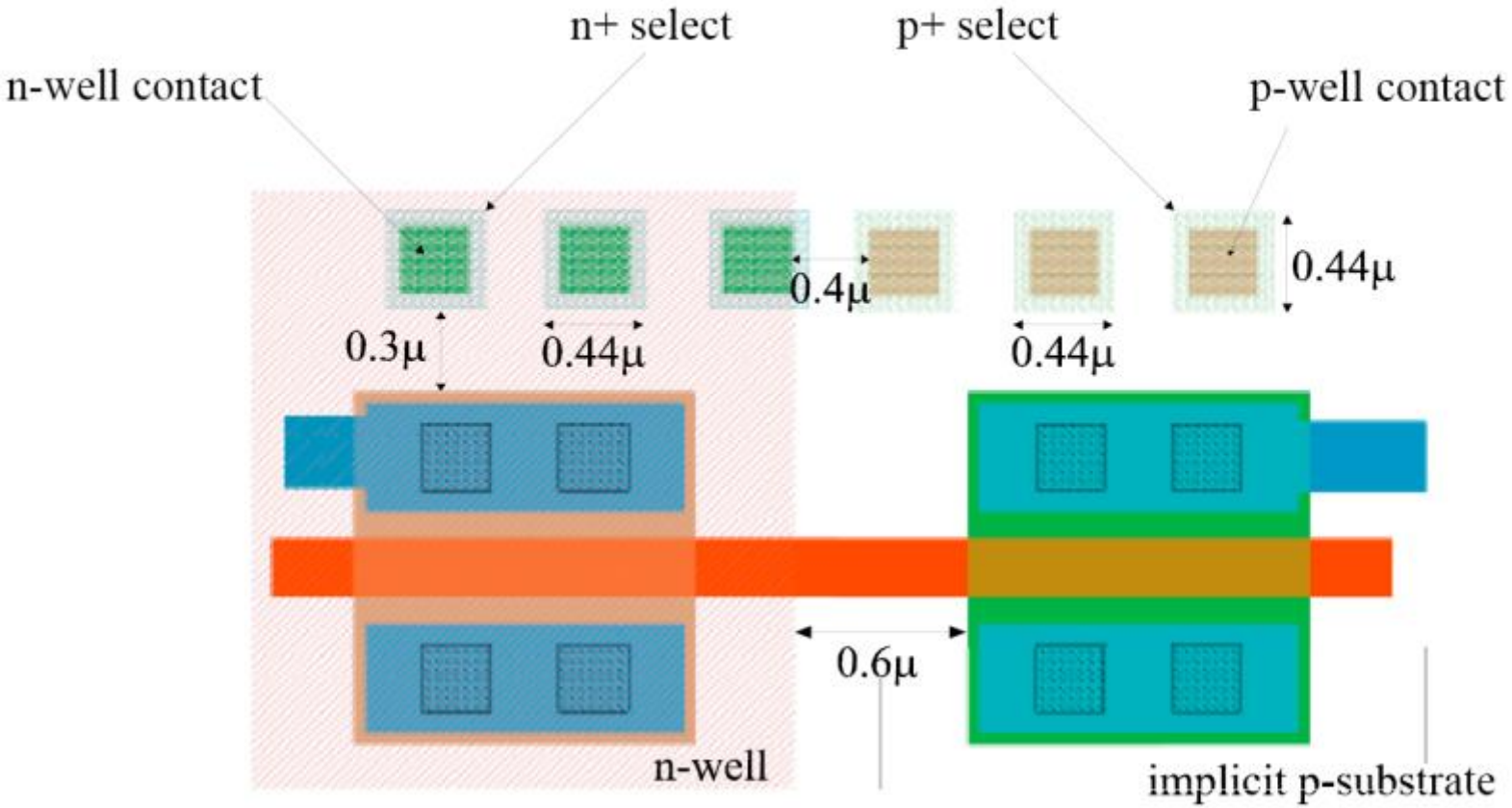
Unrelated Poly & Diffusion



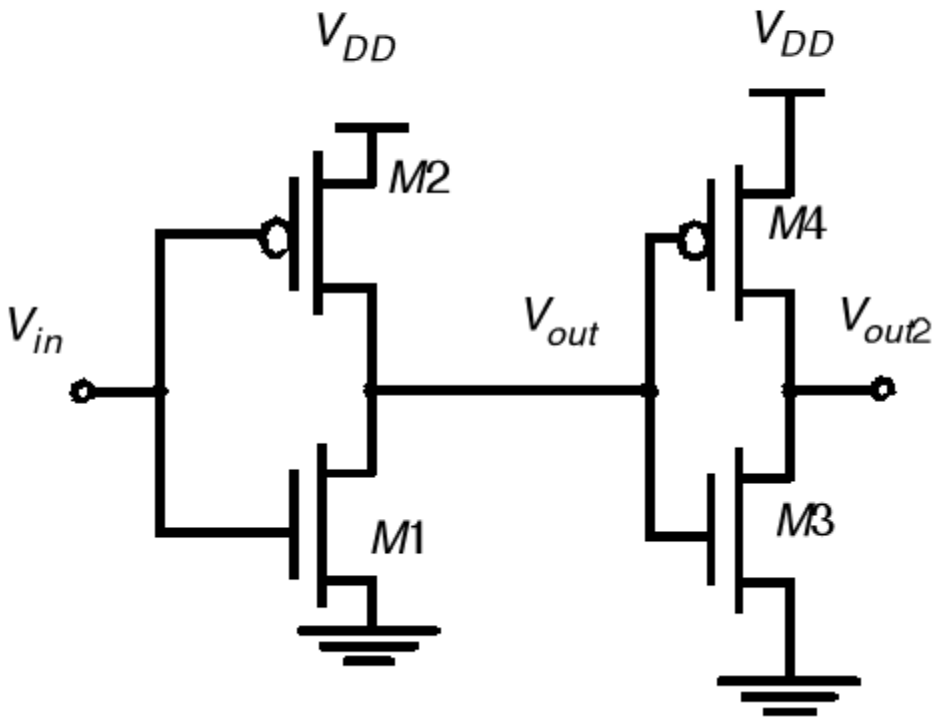
Thinner diffusion, but still working


poly
$p^+$
0.14μ
0.36μ
transistor
0.44μ
0.6μ
well boundary

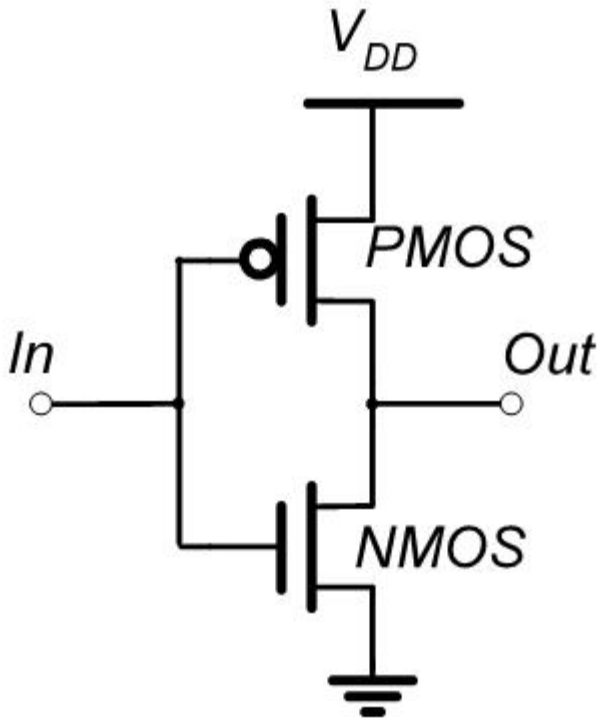
# Inter-Layer: Well and Substrate

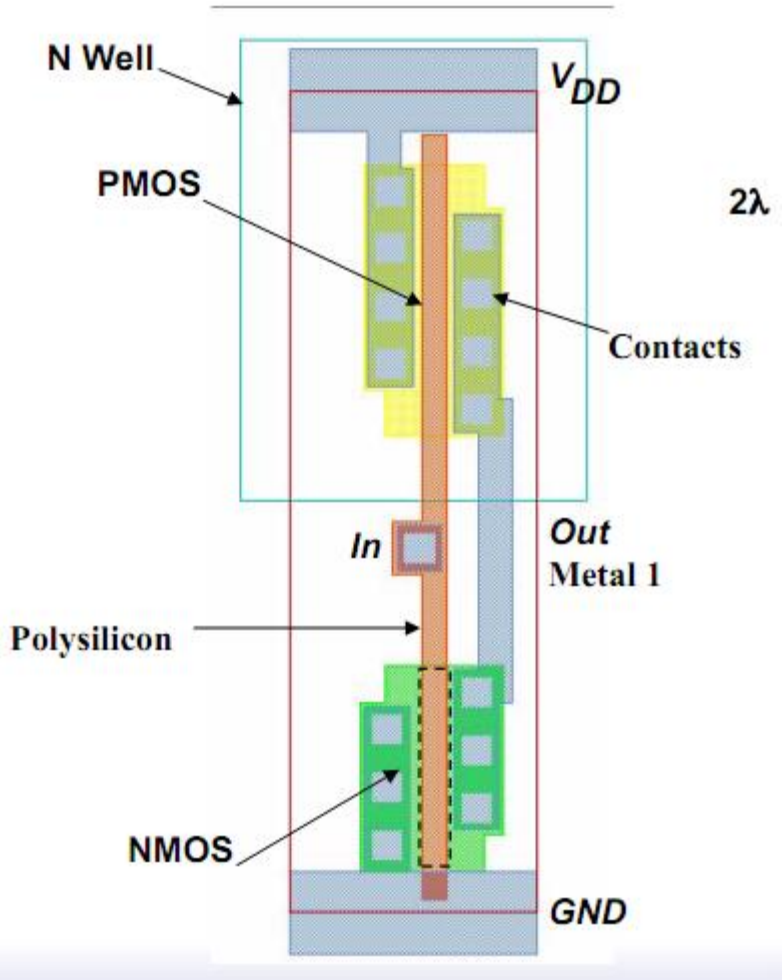


# Circuit Under Design



# CMOS Inverter

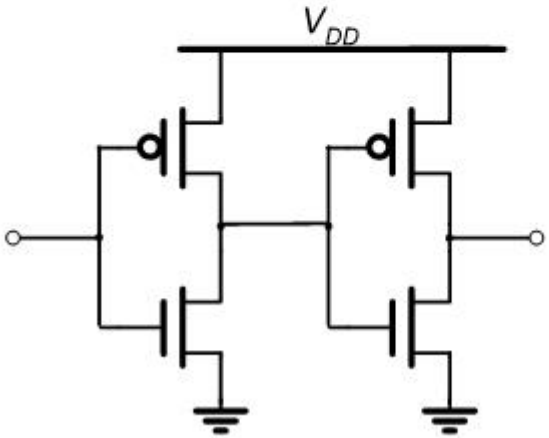


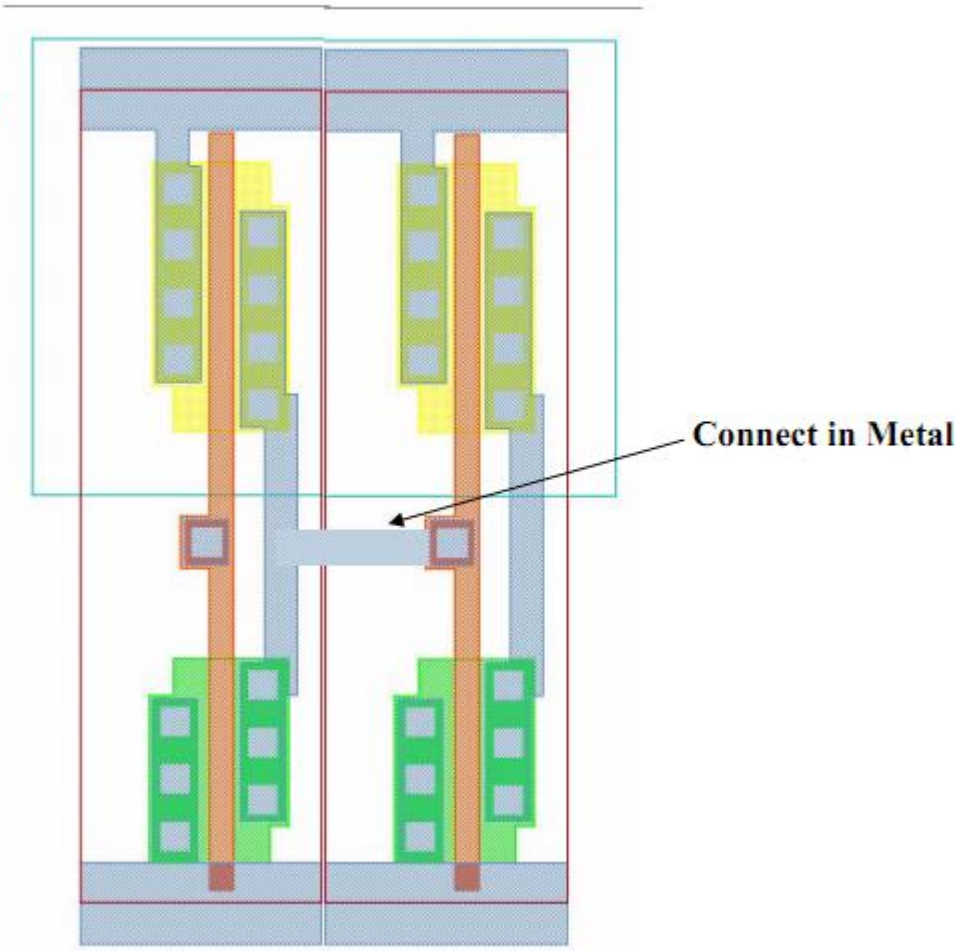



# Two Inverters

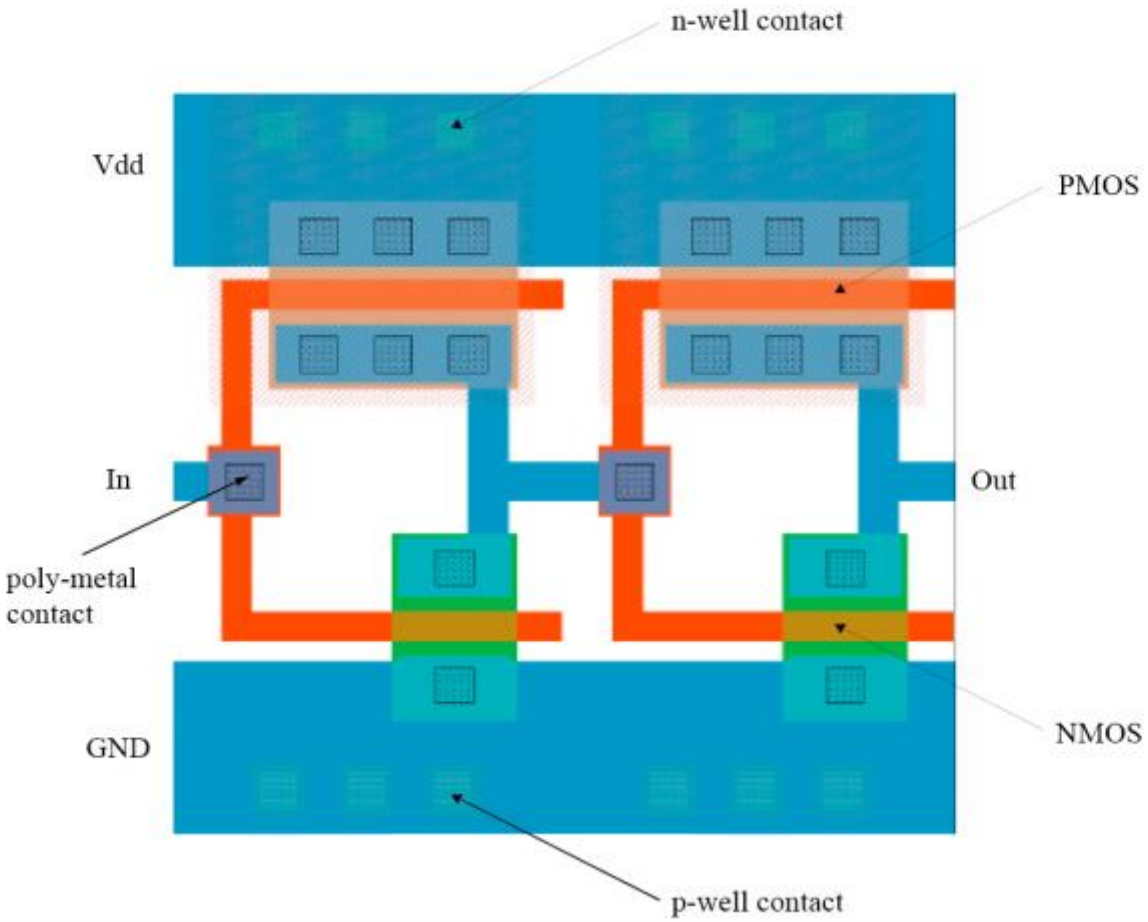
Share power and ground

Abut cells



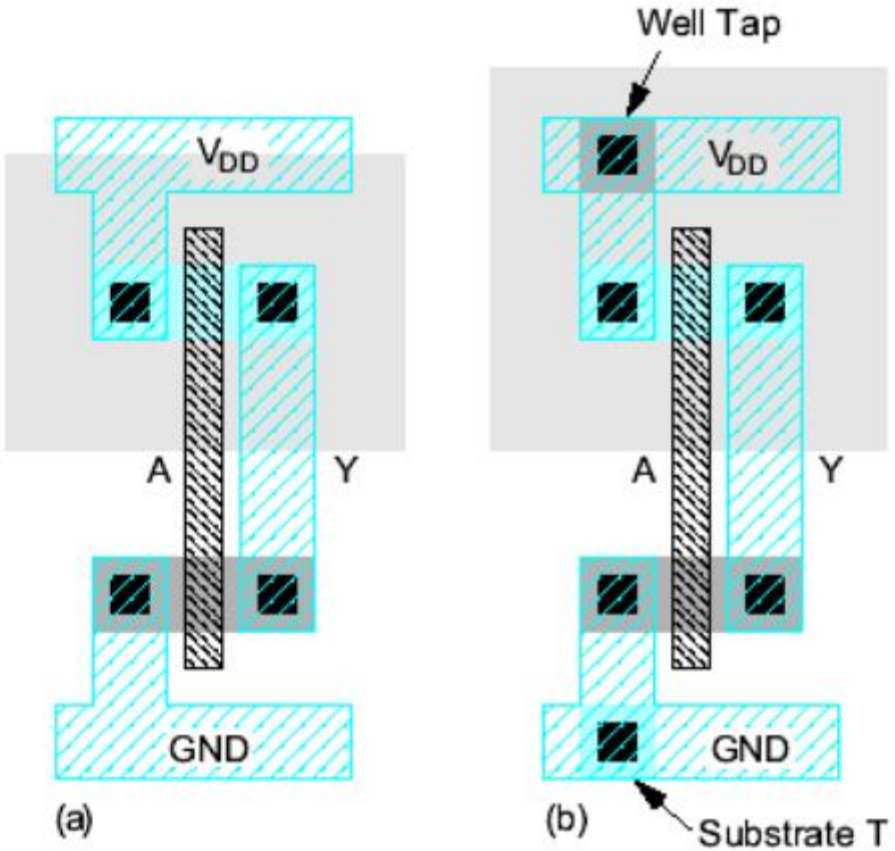
# CMOS Inverter Layout



# Gate Layout

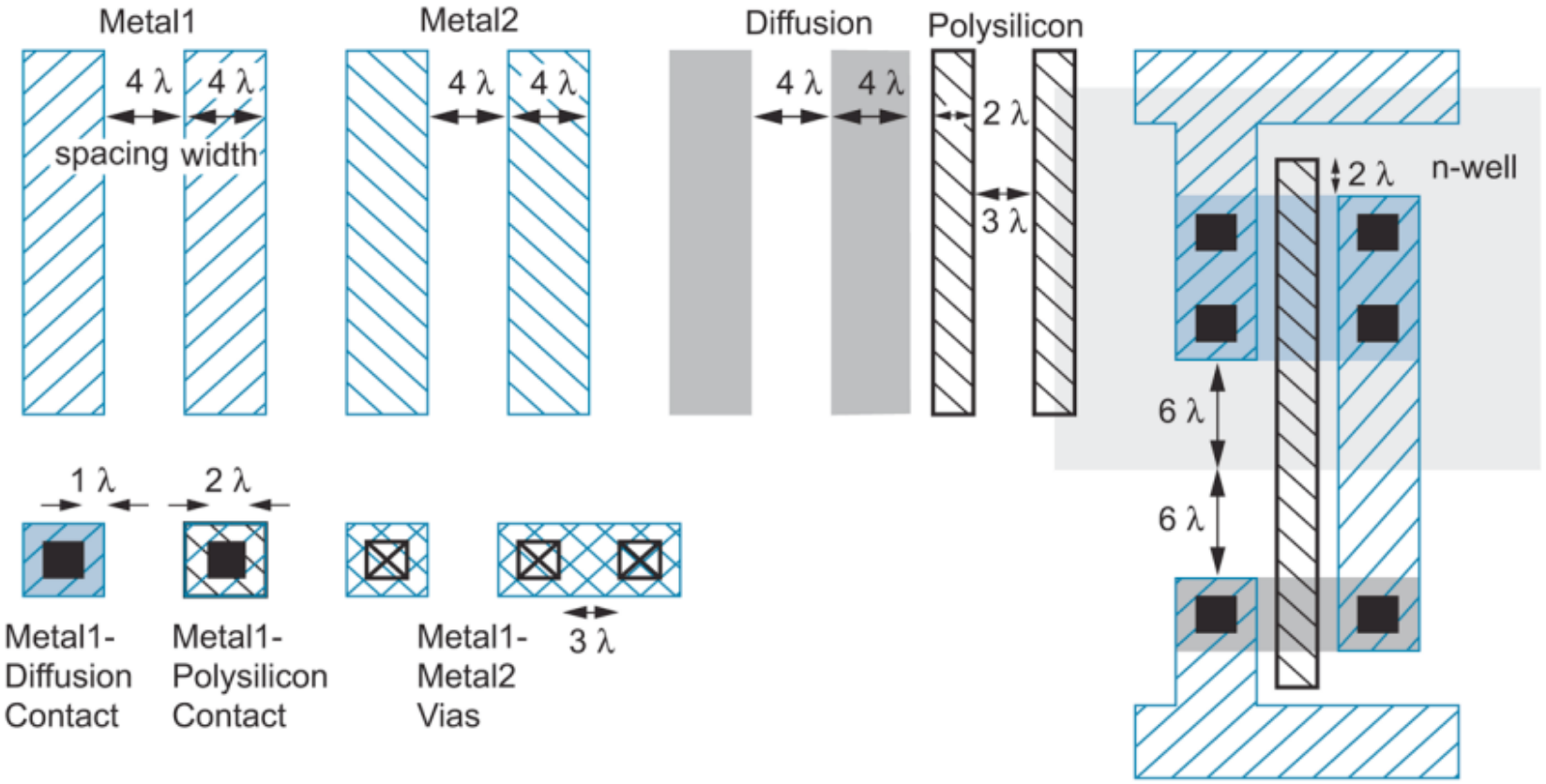
- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - $V_{DD}$ and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

# Example: Inverter



# Layout Design Rules

*Conservative rules to get started !*

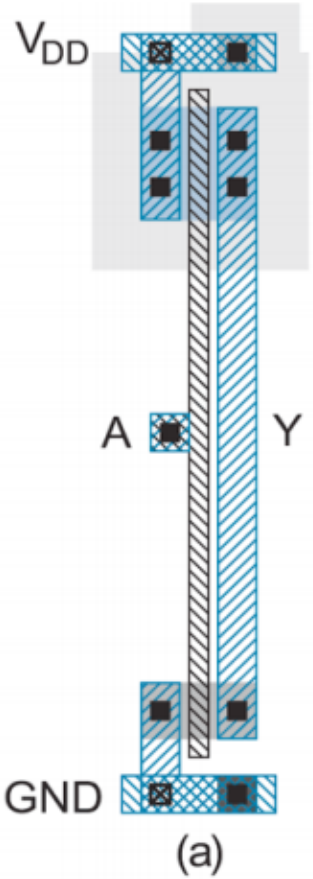


# Design Rules Summary

- Metal and diffusion have minimum width and spacing of 4λ
- Contacts are 2λ x 2λ and must be surrounded by 1λ on the layers above and below
- Polysilicon uses a width of 2λ
- Polysilicon overlaps diffusions by 2λ where a transistor is desired and has spacing or 1λ away where no transistor is desired
- Polysilicon and contacts have a spacing of 3λ from other polysilicon or contacts
- N-well surrounds pMOS transistors by 6λ and avoid nMOS transistors by 6λ

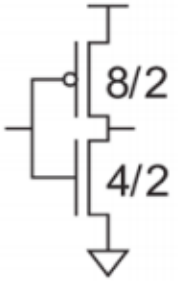
The power and ground lines are called supply rails

# Inverter Layout

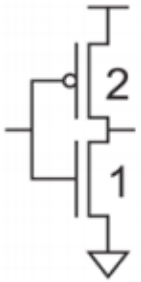


(a)

- Transistor dimensions specified as W / L ratio
- Minimum size is 4λ / 2λ, sometimes called 1 unit



(b)



(c)

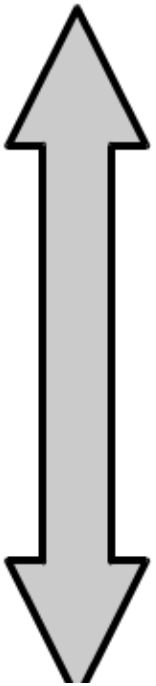
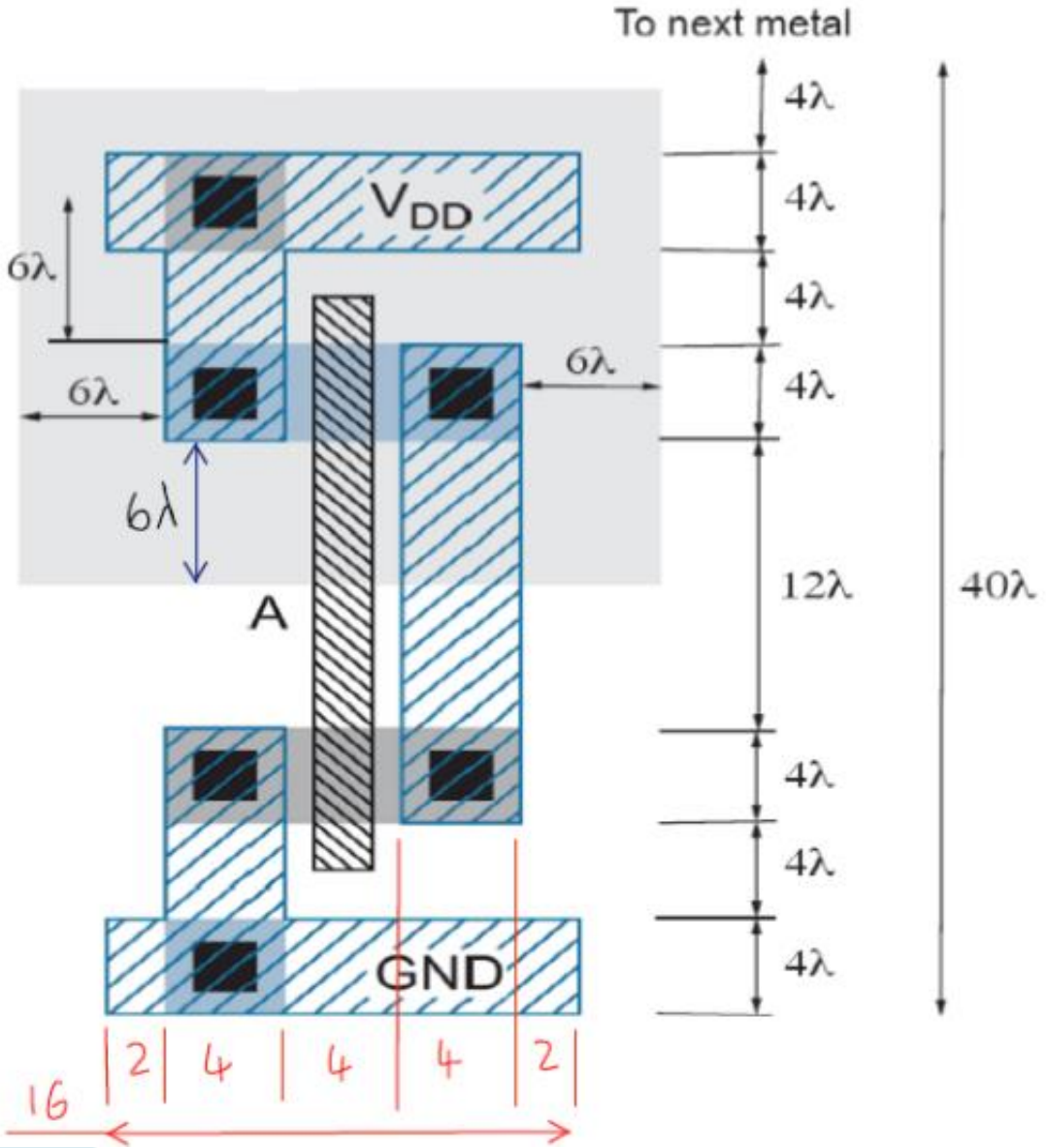
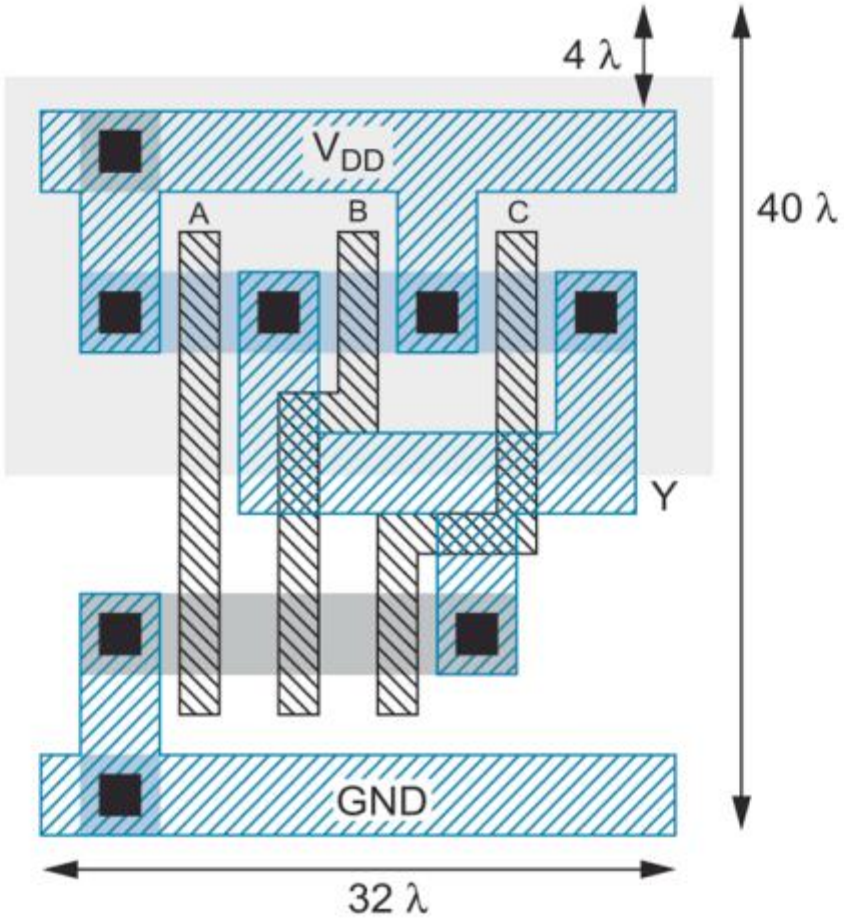


**FIG 1.40** Inverter with dimensions labeled

# Inverter Standard Cell Area (1/2

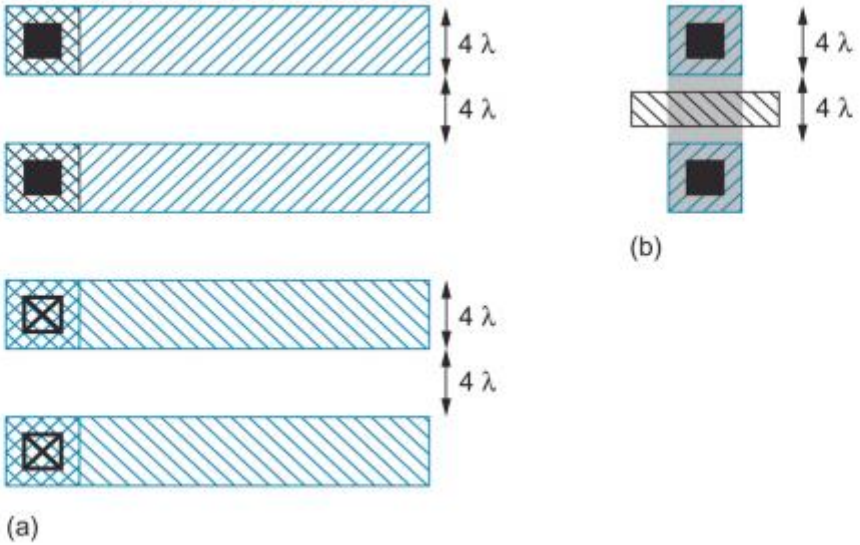


# 3-input Standard Cell NAND



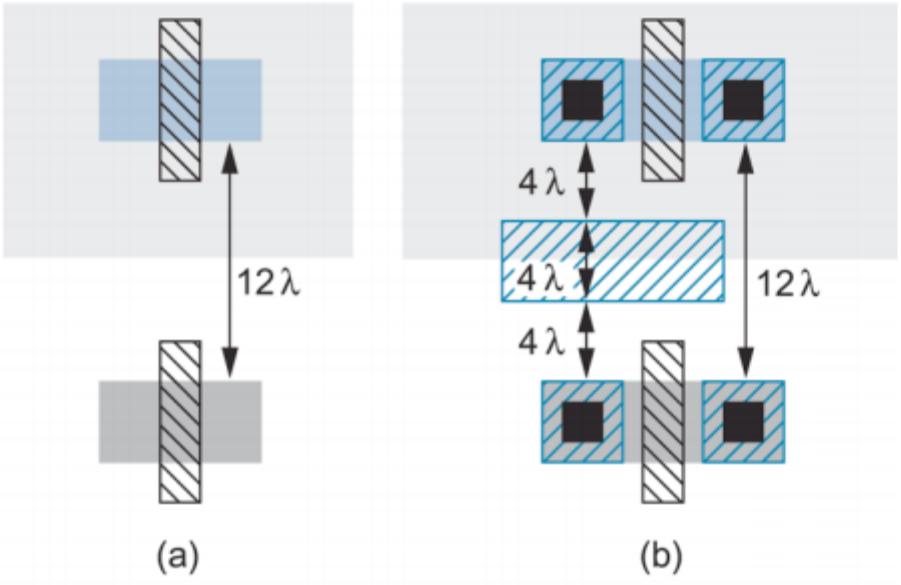
# Wiring Tracks

- A **wiring track** is the space required for a wire
  - 4λ width, 4λ spacing from neighbor = 8λ pitch
  - Transistors also consume one wiring track



# Well Spacing

- Wells must surround transistors by 6λ
  - Implies 12λ between opposite transistor flavors
  - Leaves room for one wire track

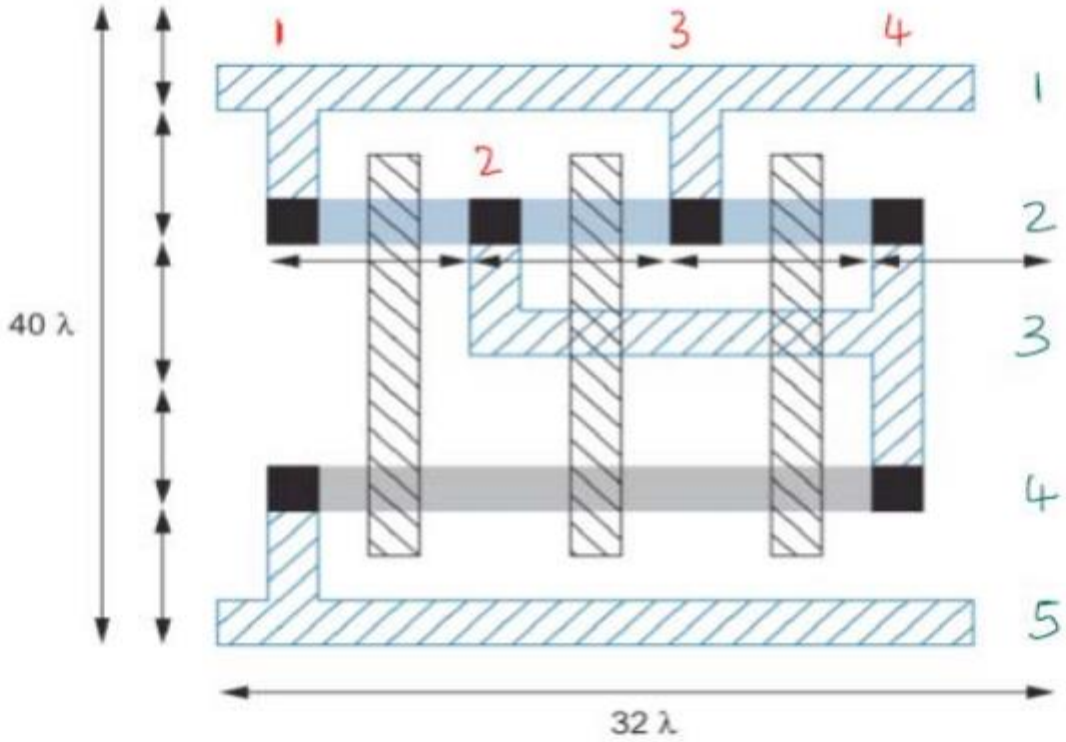


# Area Estimation

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in λ

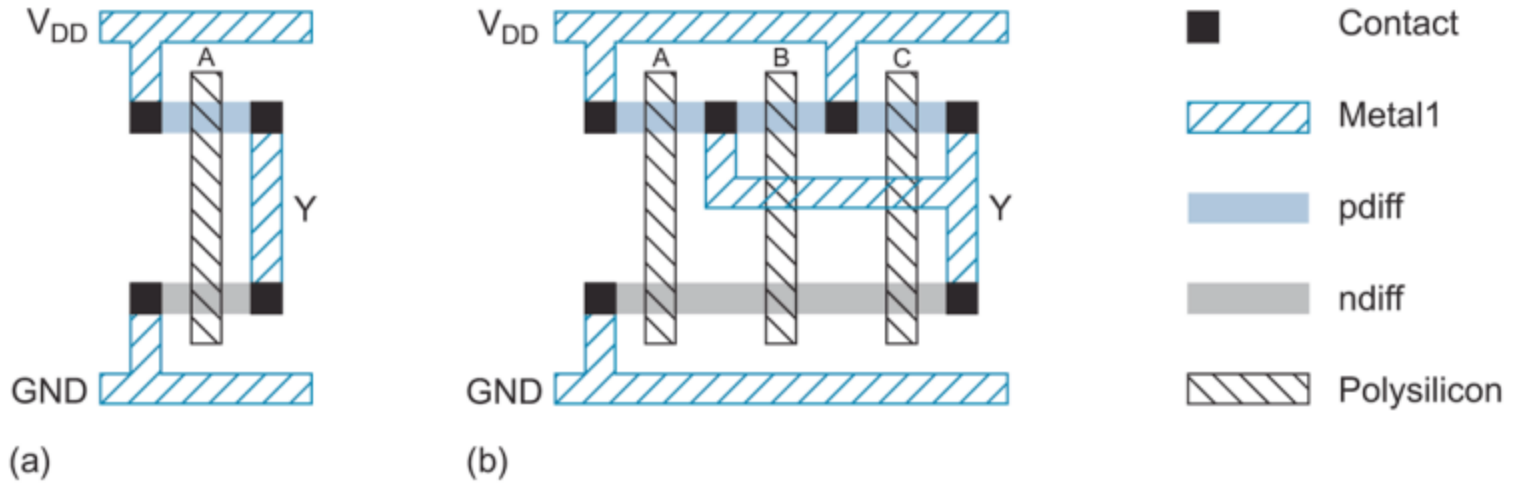
Horizontal
4 × 8 = 32

Vertical
5 × 8 = 40



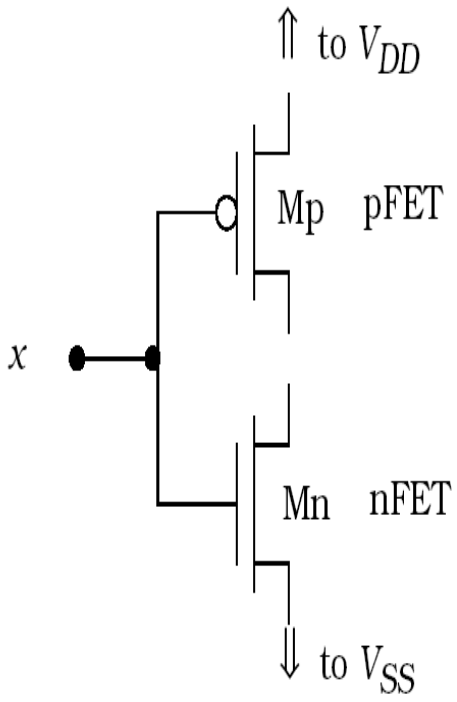
# Stick Diagrams

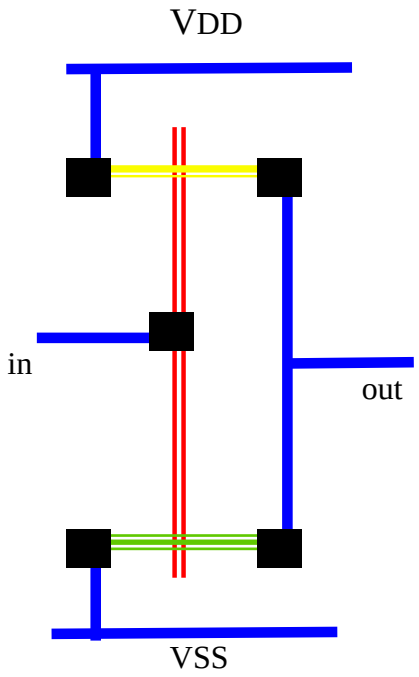
- **Stick diagrams** help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers

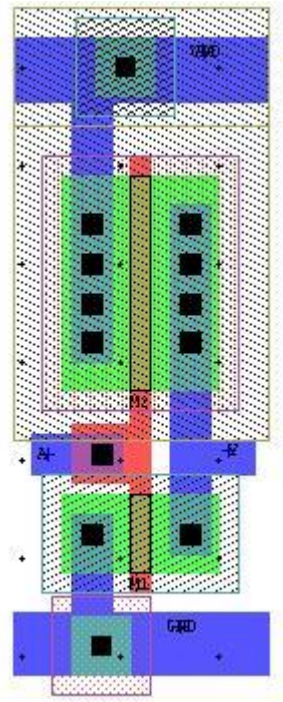


# CMOS Inverter Stick Diagrams

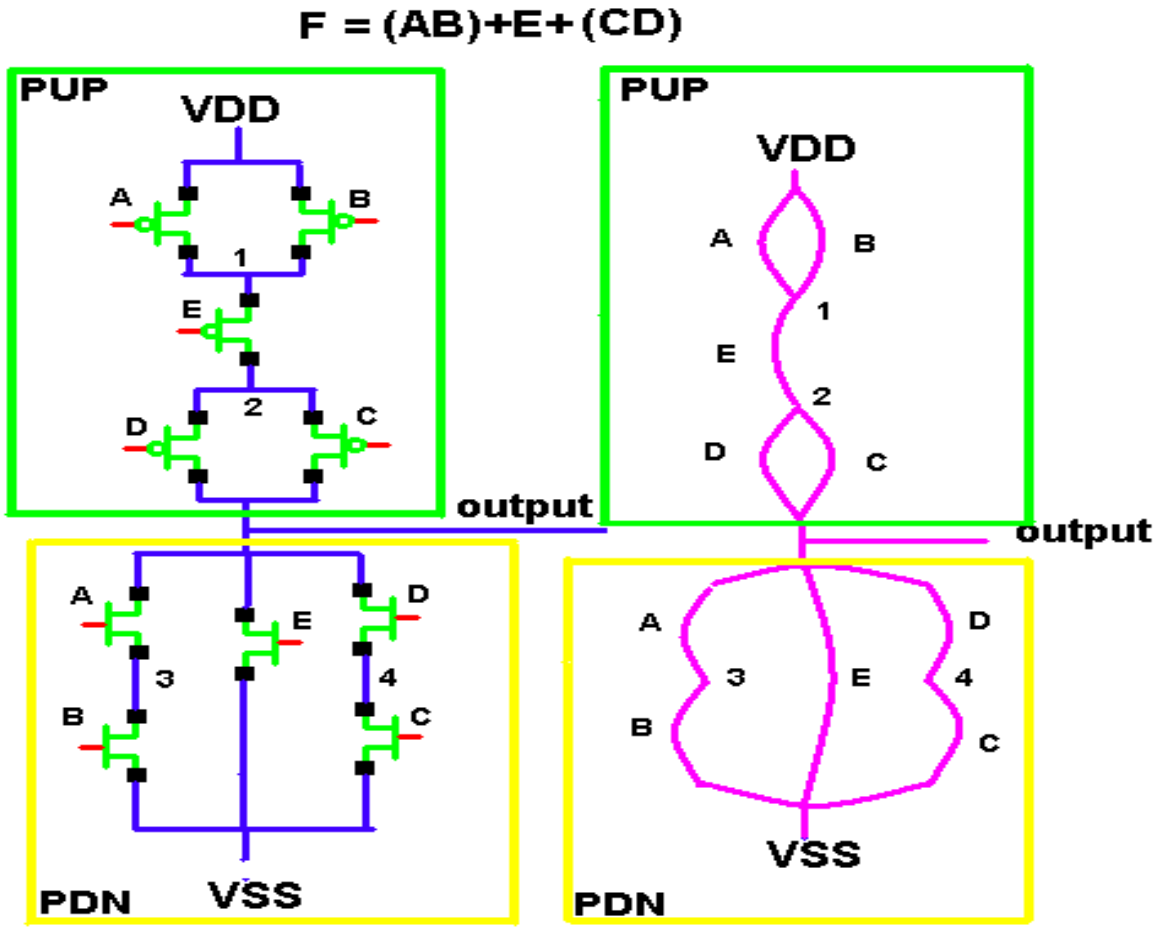
- **CMOS inverter described in other way.**



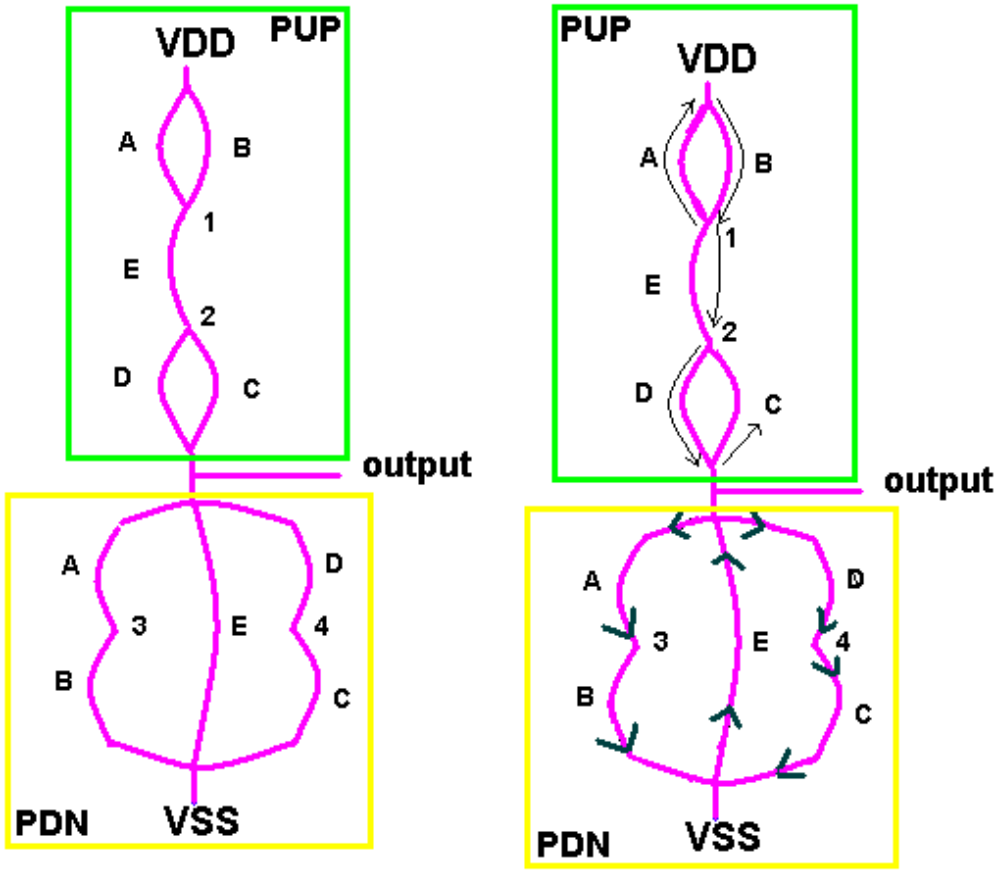
# Stick Diagram




Identify each transistor and construct a logic graph
connection to the transistor
a unique name

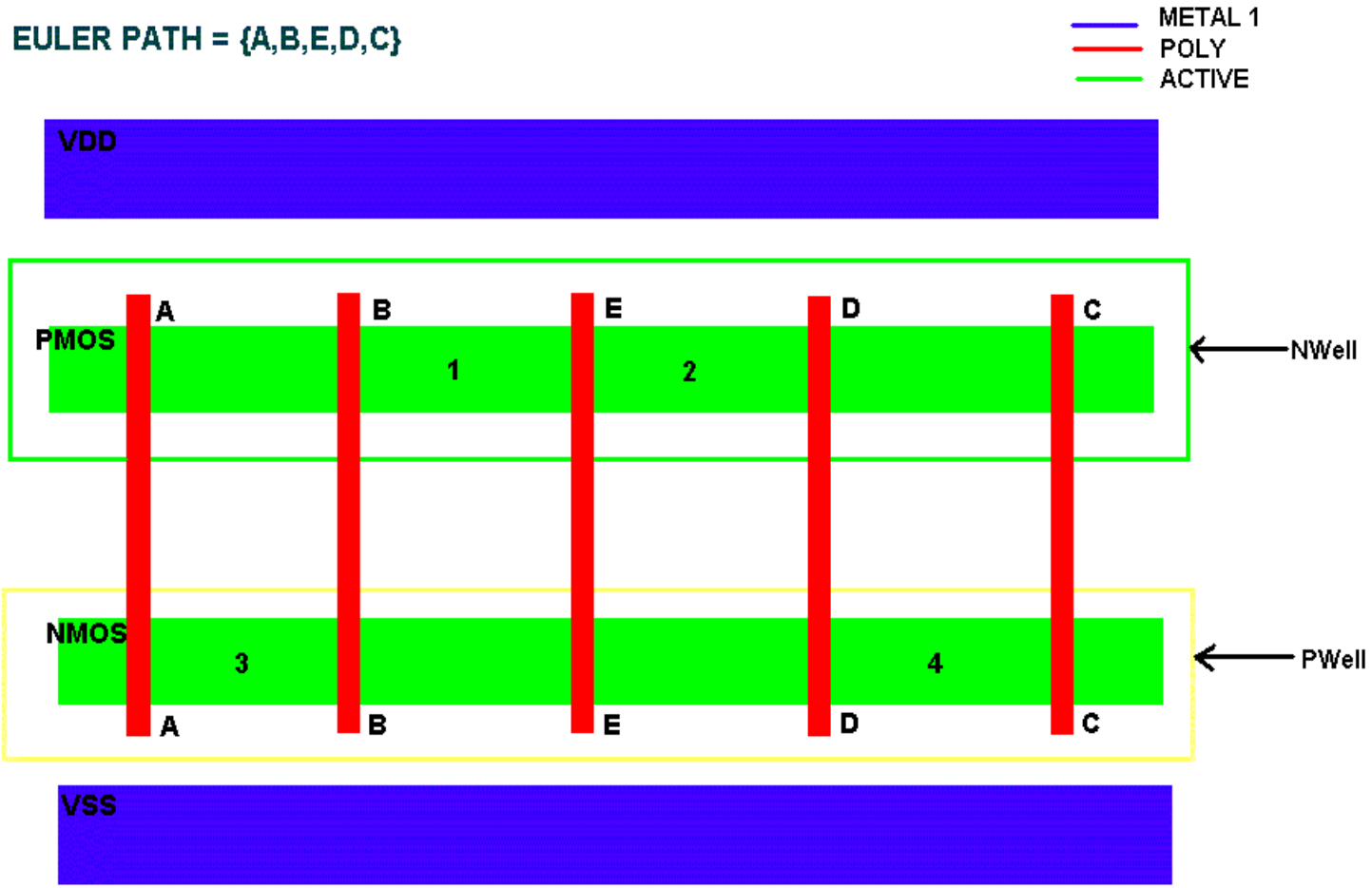
F = (AB)+E+(CD)

See the tutorial for further details.




EULER PATH = {A,B,E,D,C}

- construct one Euler path for both the Pull up and Pull down network



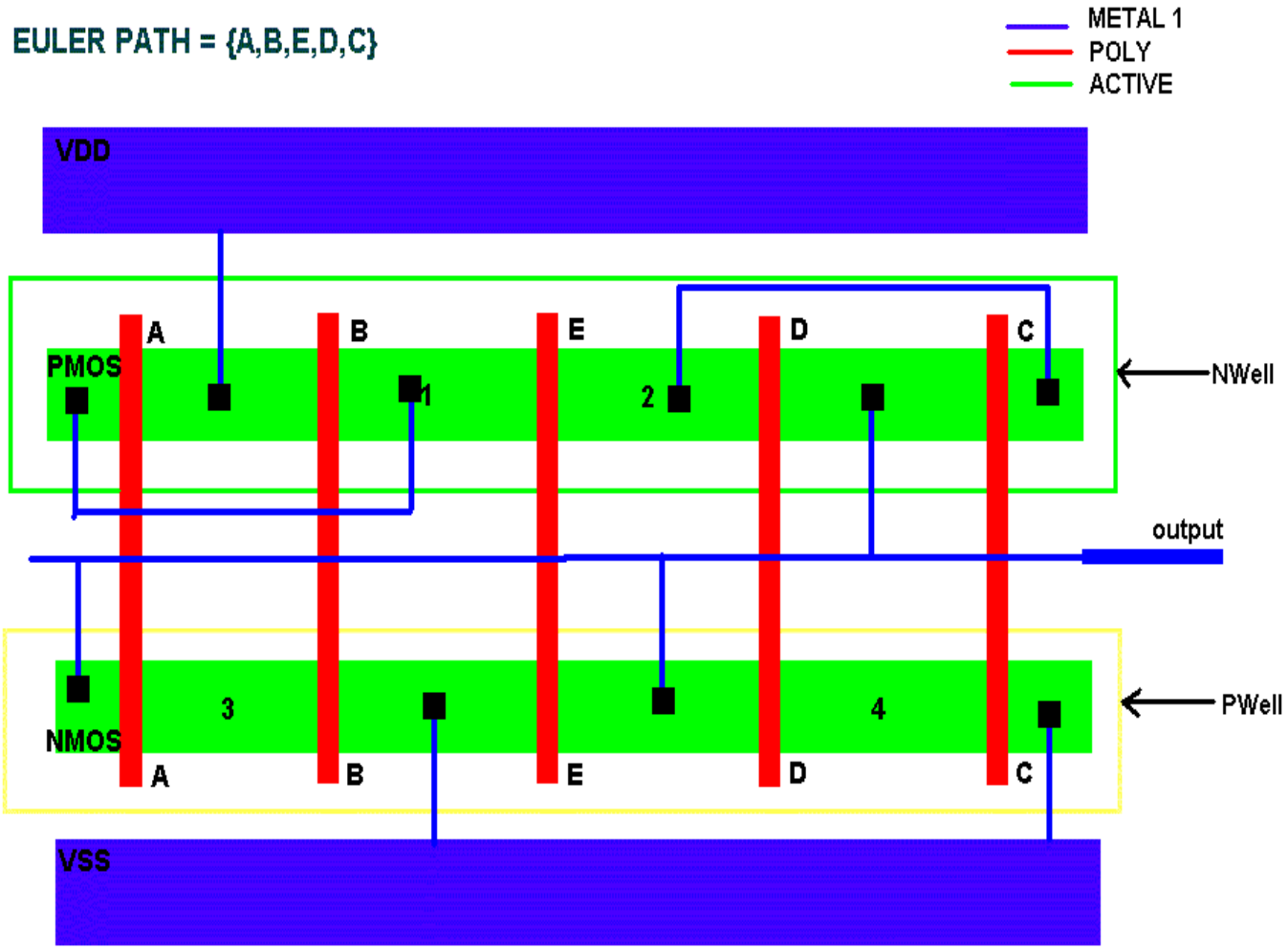

-Trace two green lines horizontally to represent the NMOS and PMOS devices and surround them by n and p-wells

-Trace the number of inputs (5 in this example) vertically across each green strip and label them in order.

-Trace blue lines to represent VDD and VSS

-Place the connection labels upon the NMOS and PMOS devices

# Layout




-Place the VDD, VSS and all output names upon the NMOS and PMOS devices

-interconnect the devices based on Euler path.