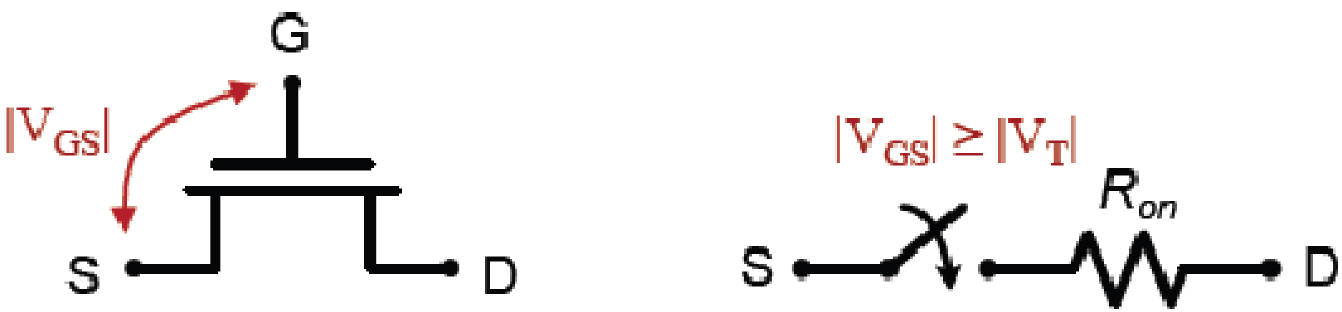
Design Metrics

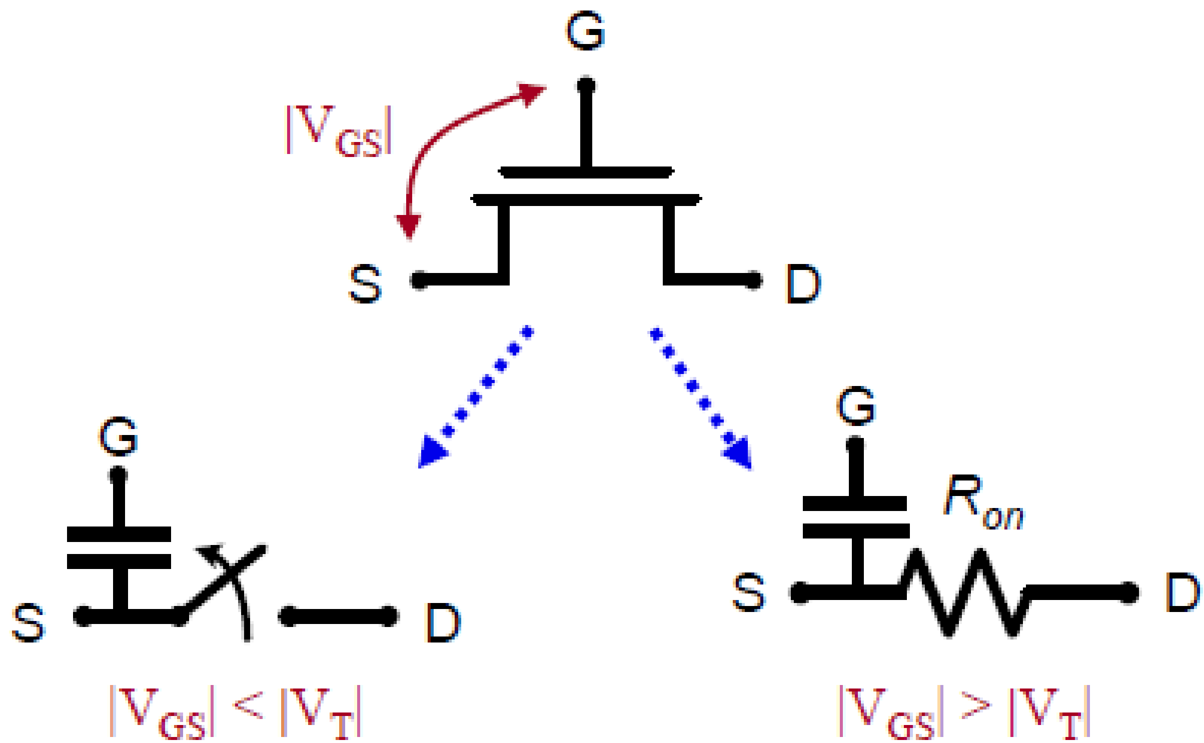
Textbook:

What is a Transistor?

An MOS Transistor ⟷ A Switch!



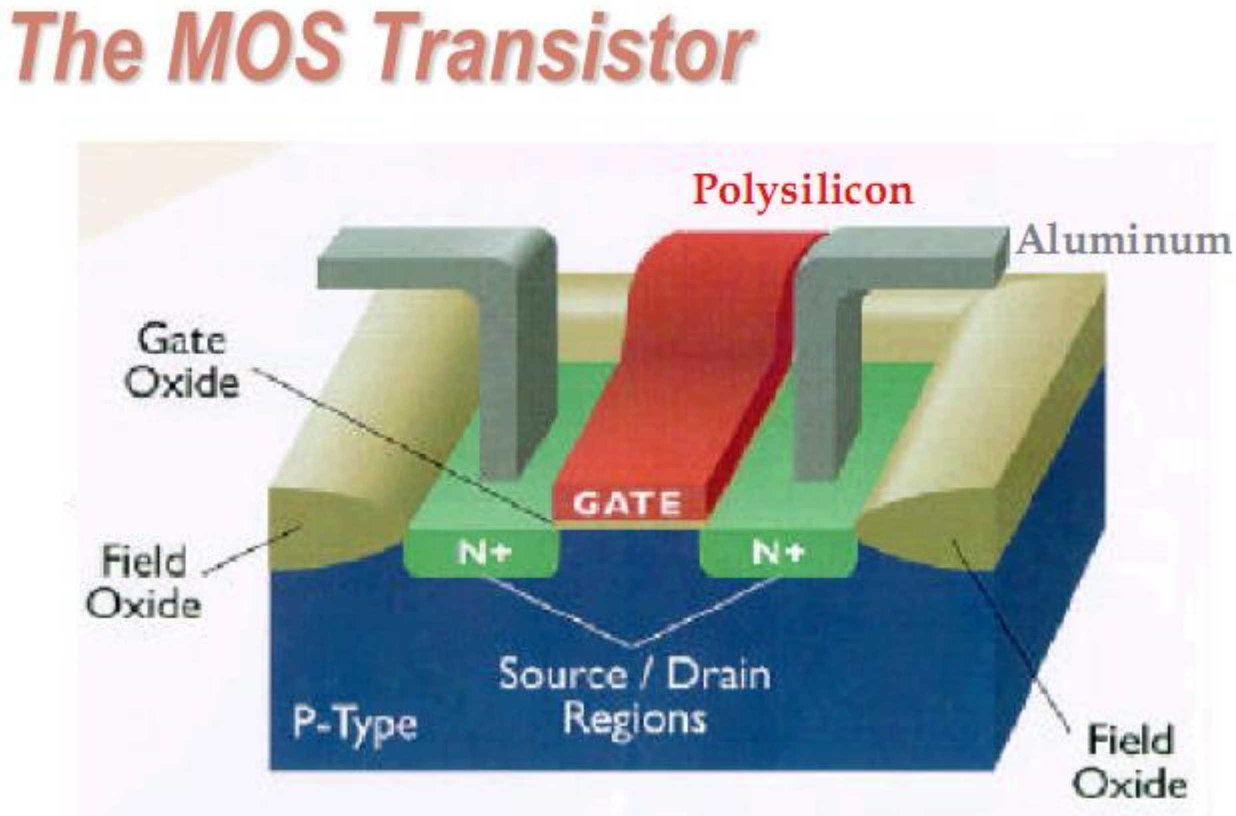
Switch Model of MOS Transistor



Design Metrics

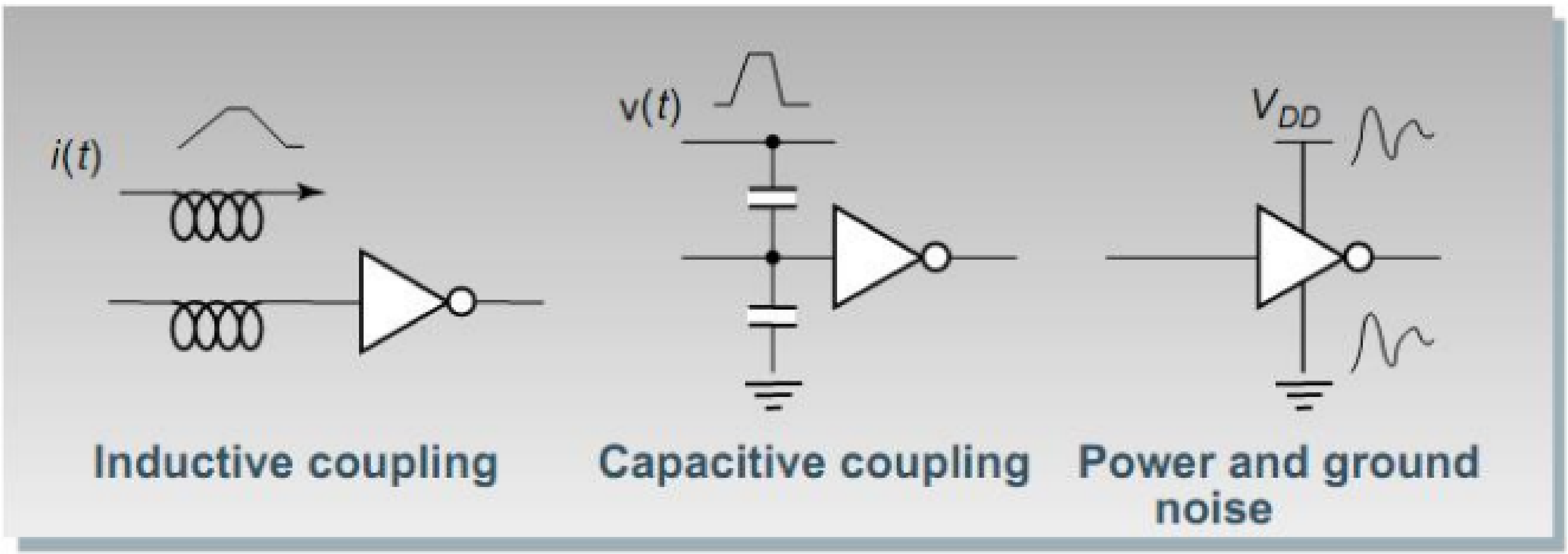
- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Speed/Performance (delay, frequency)
  - Power

Introduction to IC CMOS Manufacturing



Reliability

- The real world is analog
  - All physical quantities you deal with as a circuit designer are actually continuous
  - Thus, even a "digital" signal can be noisy:

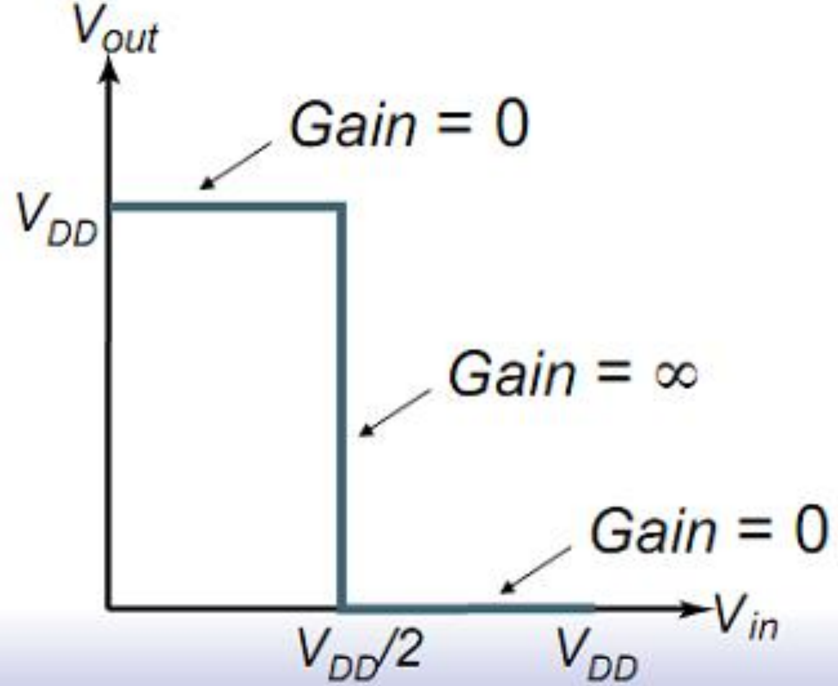


Noise and Digital Systems

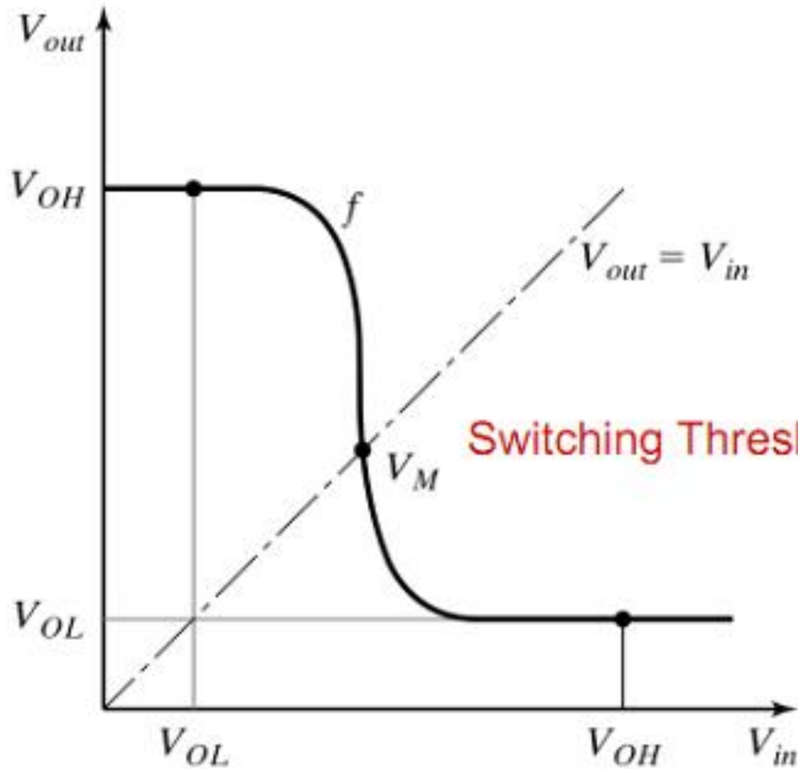
- Circuit needs to works despite “analog” noise
  - Digital gates can reject noise
  - This is actually how digital systems are defined
- Digital system is one where:
- Discrete values mapped to analog levels and back
- All the elements (gates) can reject noise
  - For “small” amounts of noise, output noise is less than input noise
- Thus, for sufficiently “small” noise, the system acts as if it was **noiseless**

Noise Rejection

- To see if a gate rejects noise
  - Look at its DC voltage transfer characteristic (VTC)
  - See what happens when input is not exactly 1 or 0
- Ideal digital gate:
  - Noise needs to be larger than $V_{DD}/2$ to have any effect on gate output



More Realistic VTC

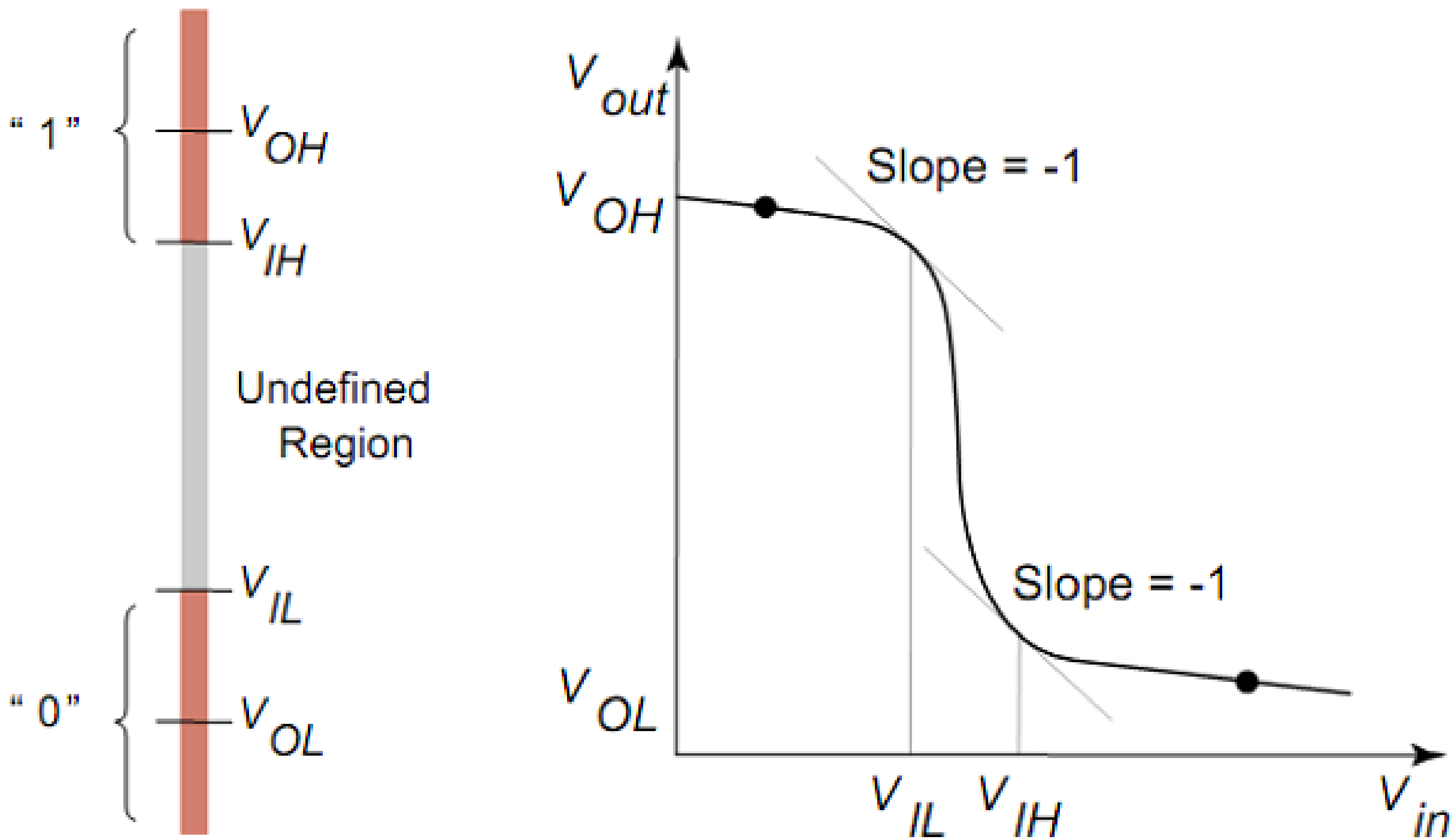


Switching Threshold

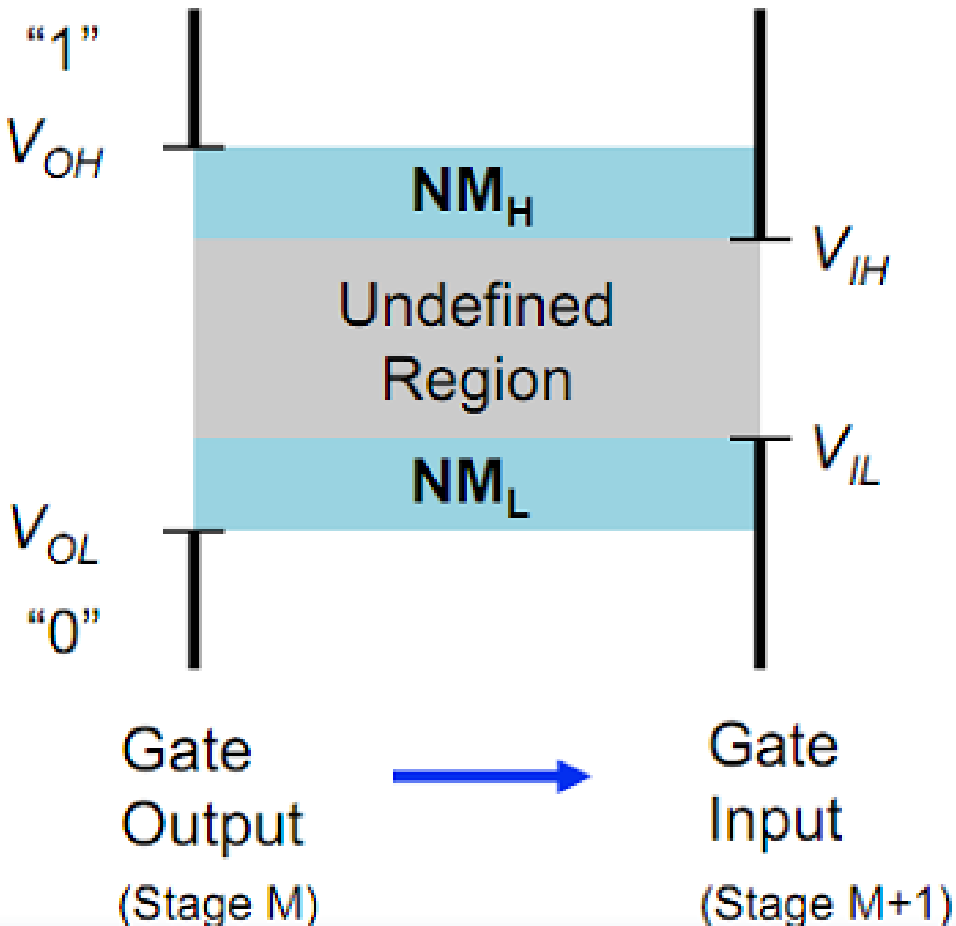
VOH = *f*(VOL)
VOL = *f*(VOH)
VM = *f*(VM)

Nominal Voltage Levels

Voltage Mapping



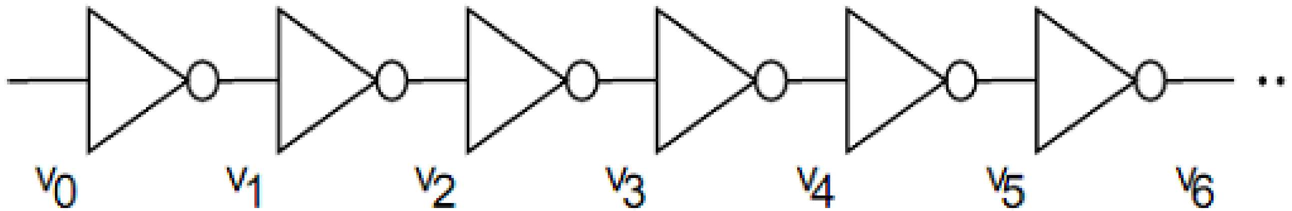
Definitions of Noise Margins



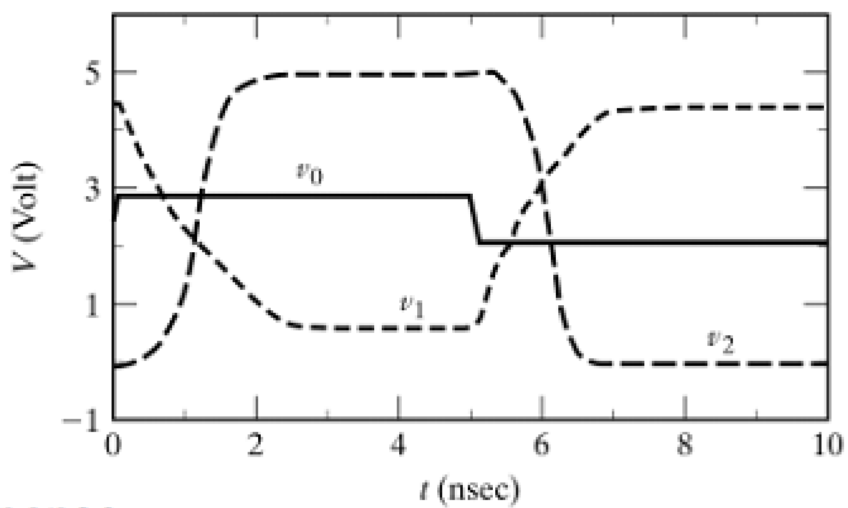
Noise margin high:
$NM_H = V_{OH} - V_{IH}$

Noise margin low:
$NM_L = V_{IL} - V_{OL}$

Digital Noise Reduction: Regenerative Property

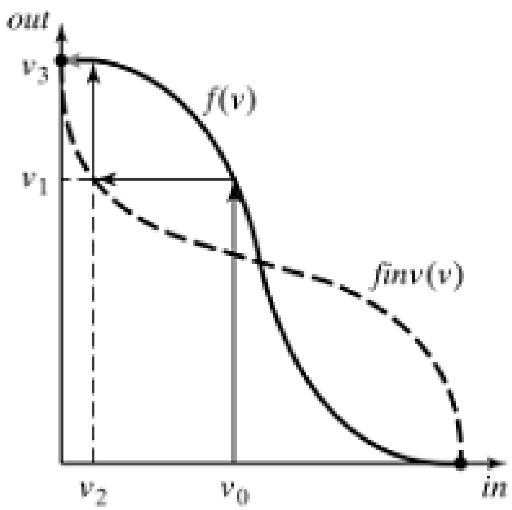


A chain of inverters

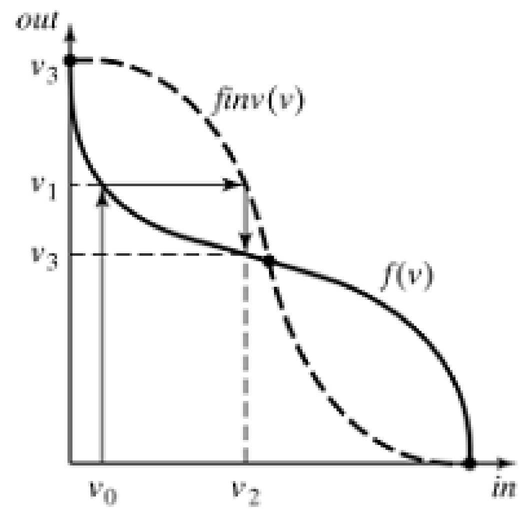


Simulated response

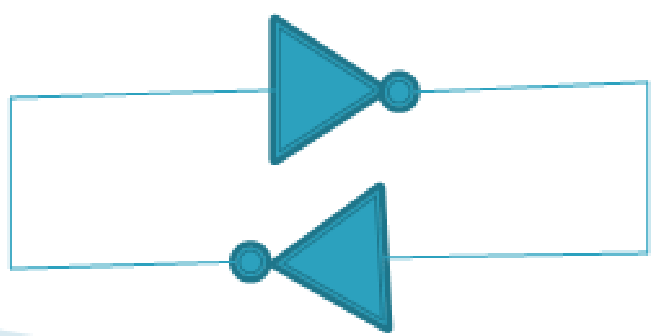
Regenerative Property



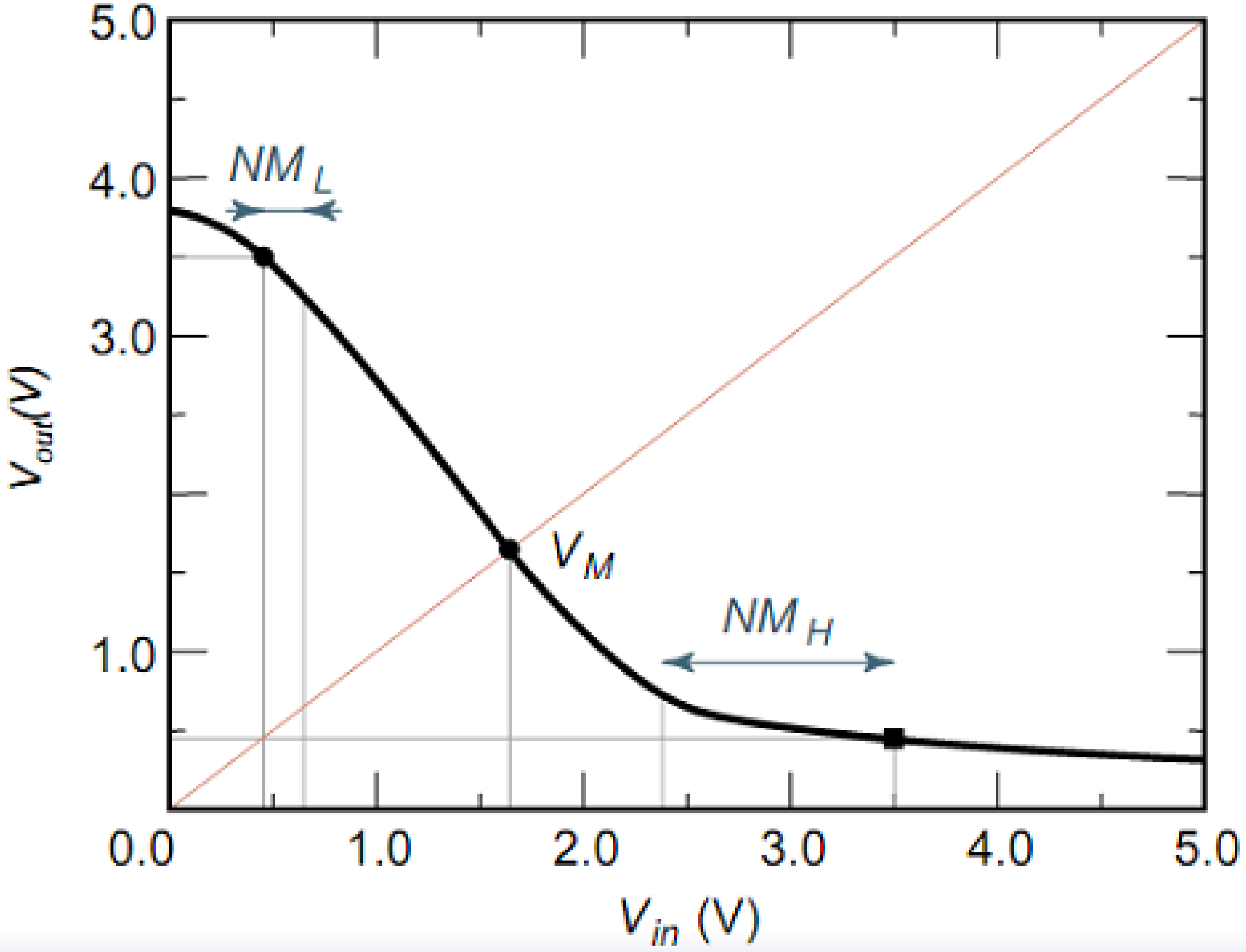
Regenerative



Non-Regenerative



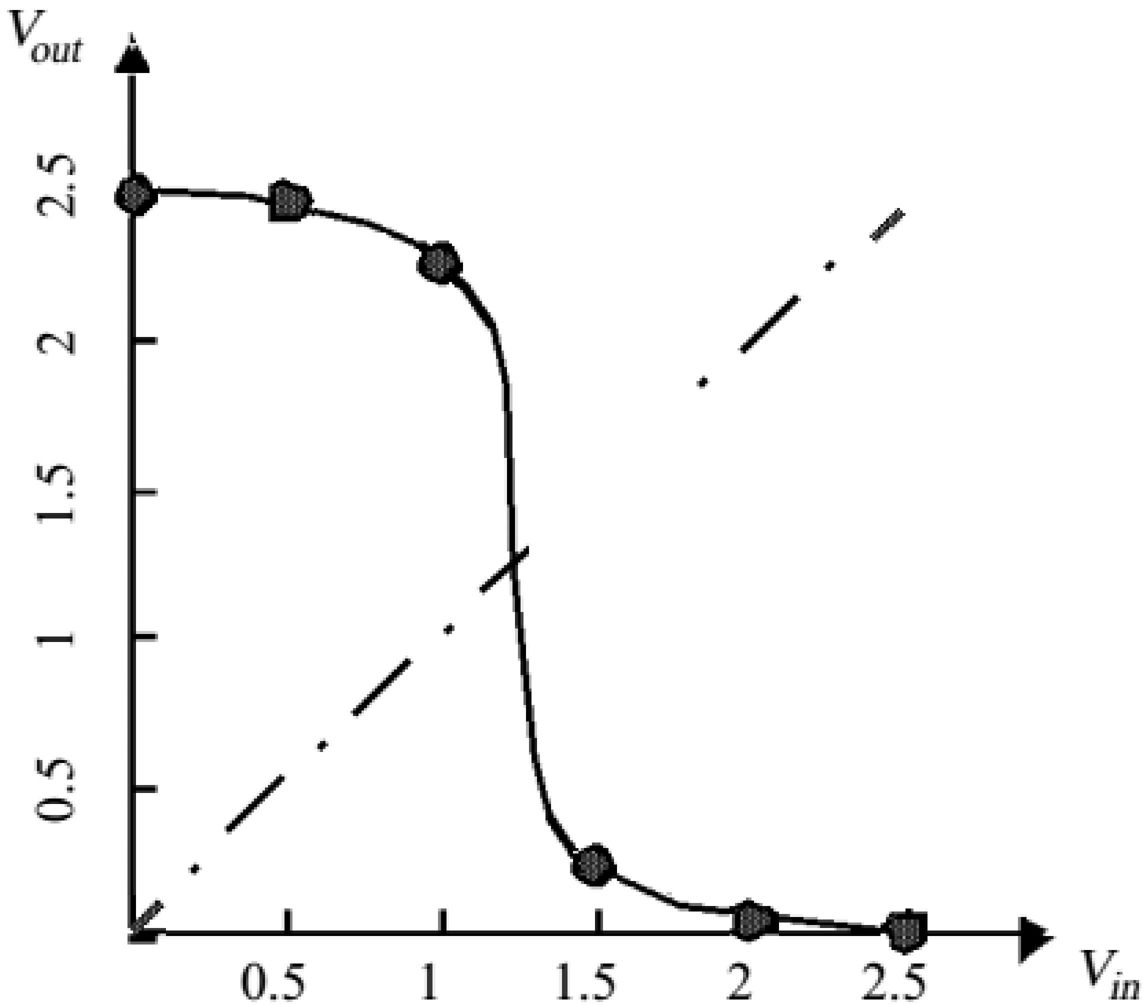
Example NMOS Inverter of 1970



Example

- $V_{OH} = 3.6V$
- $V_{OL} = 0.4V$
- $V_{IL} = 0.6V$
- $V_{IH} = 2.3V$
- $NM_H = V_{OH} - V_{IH} = 1.3V$
- $NM_L = V_{IL} - V_{OL} = 0.2V$

CMOS Inverter VTC



Summery

- Understanding the design metrics that govern digital design is crucial
  - We discussed cost and reliability so far

- Key design messages so far:
  - Keep chip area as small as possible
  - Pick design styles and parameters so that noise margins are reasonable

- Summary of some key reliability metrics:
  - Noise transfer functions & margin (ideal: gain = ∞, margin = $V_{dd}/2$)
  - Output impedance (ideal: $R_o = 0$)
  - Input impedance (ideal: $R_i = \infty$)

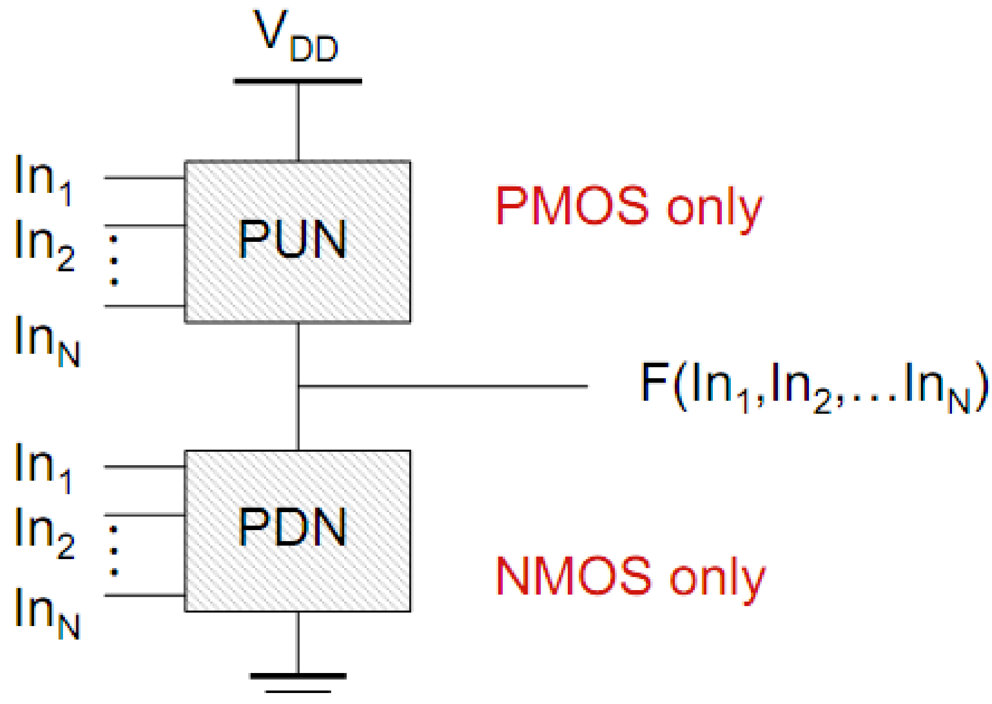
Static Logic Gates

At every point in time (except during the switching transients) each gate output is connected to either V_{DD} or V_{SS} via a low resistive path.

The outputs of the gates assume at all times the valu of the Boolean function implemented by the circuit (ignoring, once again, the transient effects during switching periods).

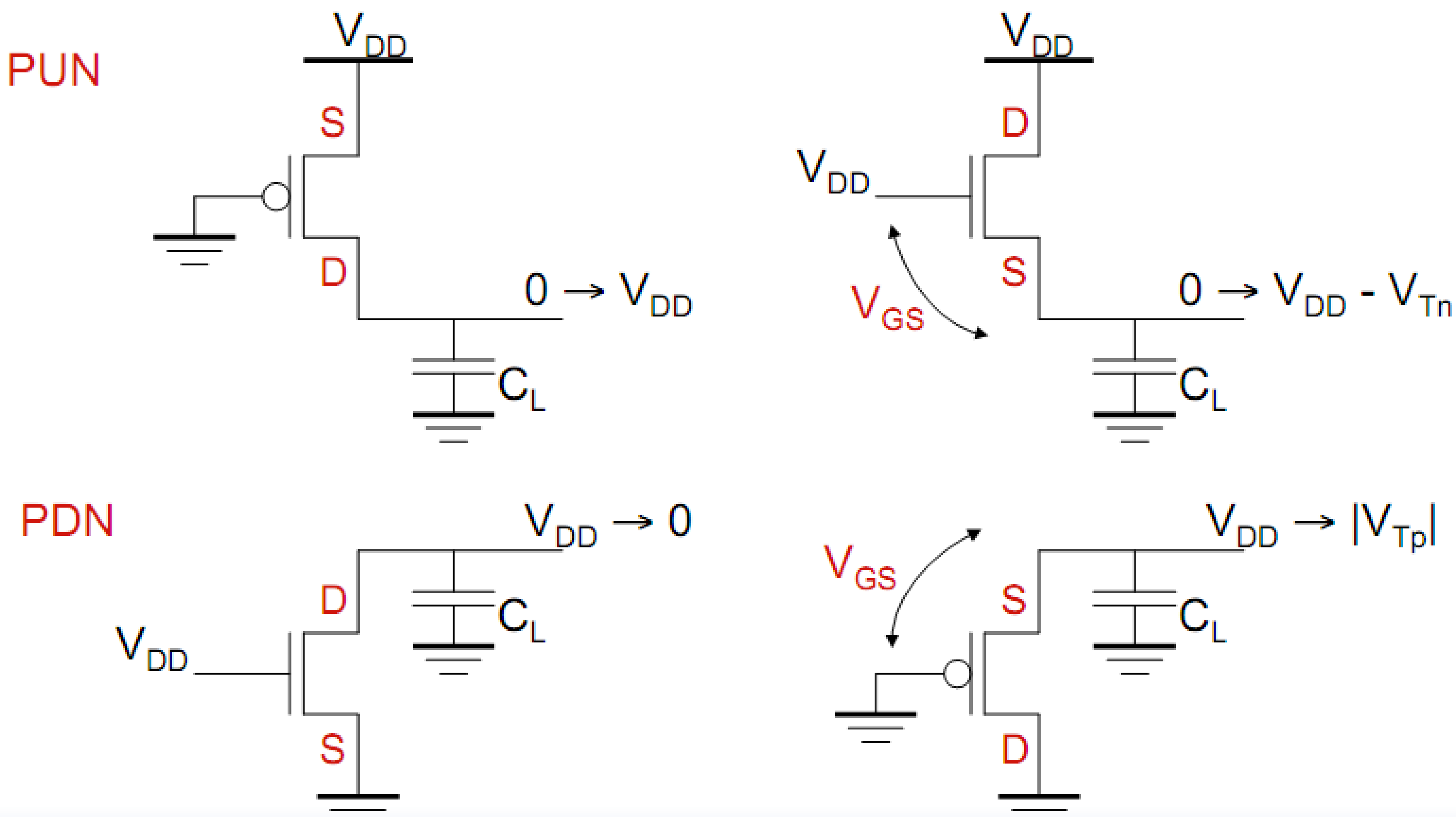
(Will contrast this later to dynamic circuit style.)

Static Complementary CMOS



PUN and PDN are dual logic networks
PUN and PDN functions are complementary

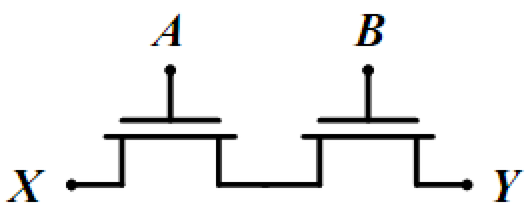
REMEMBER ….


PUN
VDD
S
D
0 → VDD
CL
VDD
D
VDD
S
VGS
0 → VDD - VTn
CL
PDN
VDD → 0
D
VDD
S
CL
VGS
VDD → |VTp|
S
D
CL

NMOS Transistors in Series/Parallel Connection

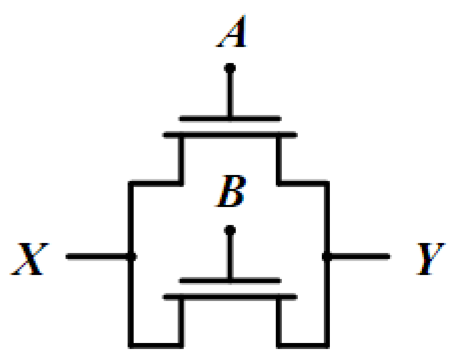
- Transistor ↔ switch controlled by its gate signal
  - NMOS switch closes when switch control input is high

AND



$Y = X$ if A AND B

OR



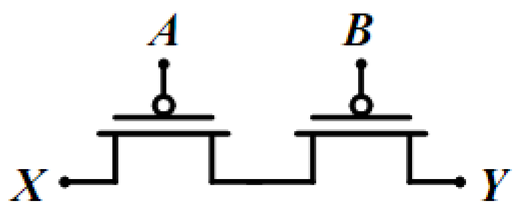
$Y = X$ if A OR B

- NMOS transistors pass a “strong” 0 but a “weak” 1

PMOS Transistors
in Series/Parallel Connection

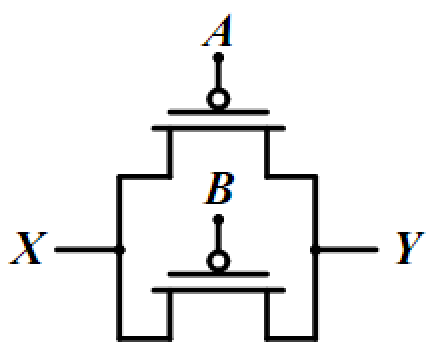
- PMOS switch closes when switch control is low

NOR



$$Y = X \text{ if } \overline{A} \text{ AND } \overline{B} = \overline{A + B}$$

NAND



$$Y = X \text{ if } \overline{A} \text{ OR } \overline{B} = \overline{AB}$$

- PMOS transistors pass a “strong” 1 but a “weak” 0

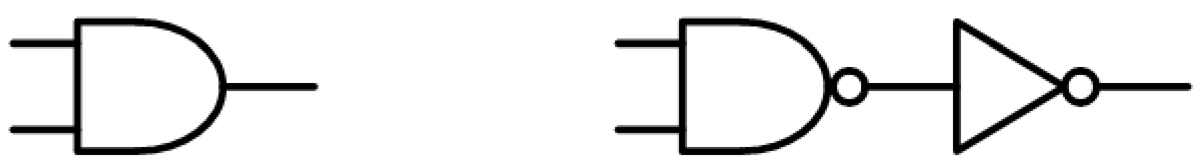
Complementary CMOS Logic Style

- PUP is the **dual** to PDN
  (can be shown using DeMorgan's Theorems)

$$\overline{A+B} = \bar{A}\bar{B}$$

$$\overline{AB} = \bar{A} + \bar{B}$$

- Static CMOS gates are always inverting

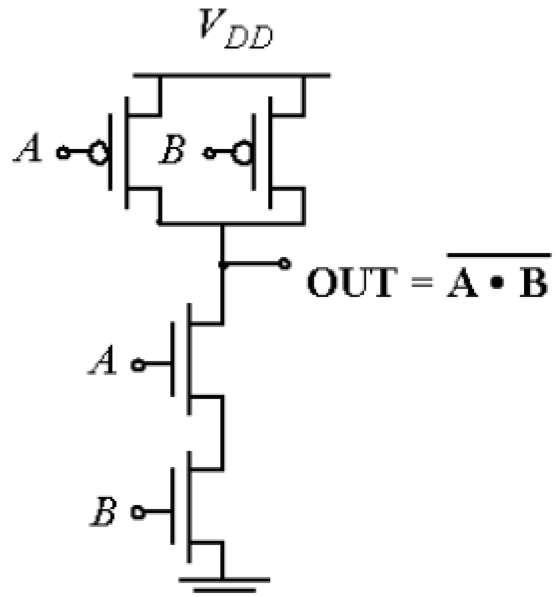


AND = NAND + INV

Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate

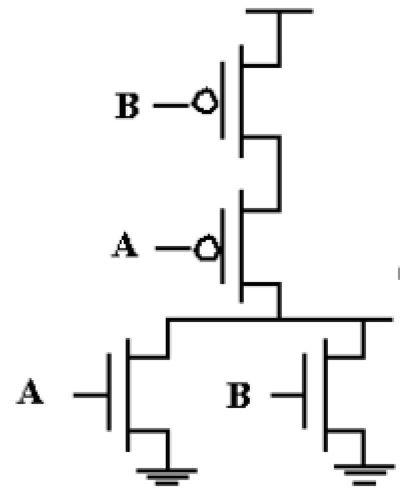


- PDN: G = AB ⇒ Conduction to GND
- PUN: F = $\bar{A} + \bar{B} = \overline{AB}$ ⇒ Conduction to V_{DD}
- $\overline{G(In_1,In_2,In_3,\ldots)} \equiv F(\overline{In_1},\overline{In_2},\overline{In_3},\ldots)$

Example Gate: NOR

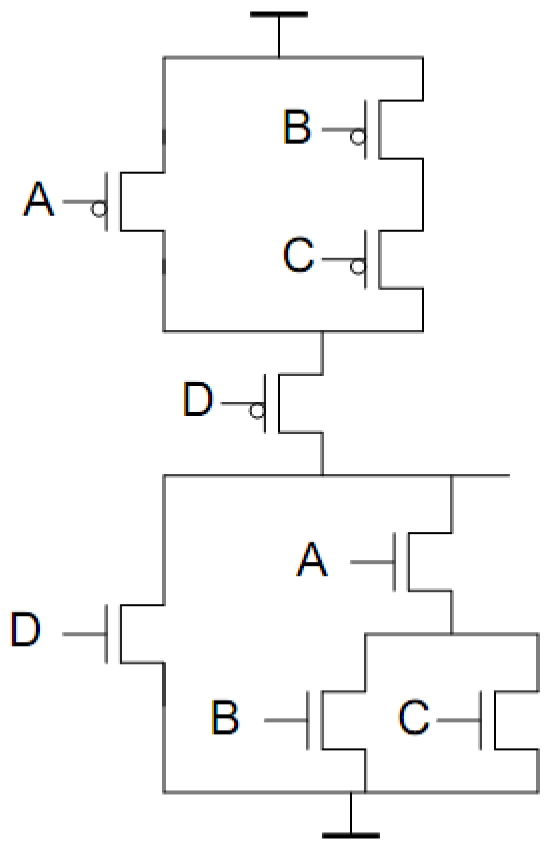
A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate



$$OUT = \overline{A + B}$$

Complex CMOS Gate

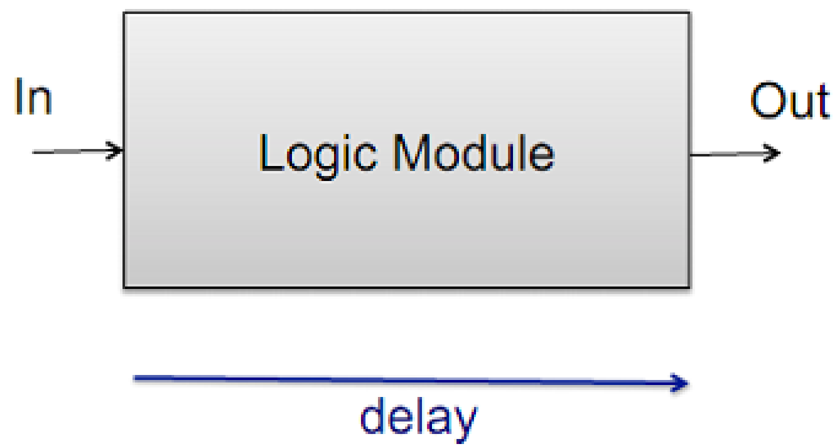


$OUT = \overline{D + A \cdot (B + C)}$

CMOS Properties

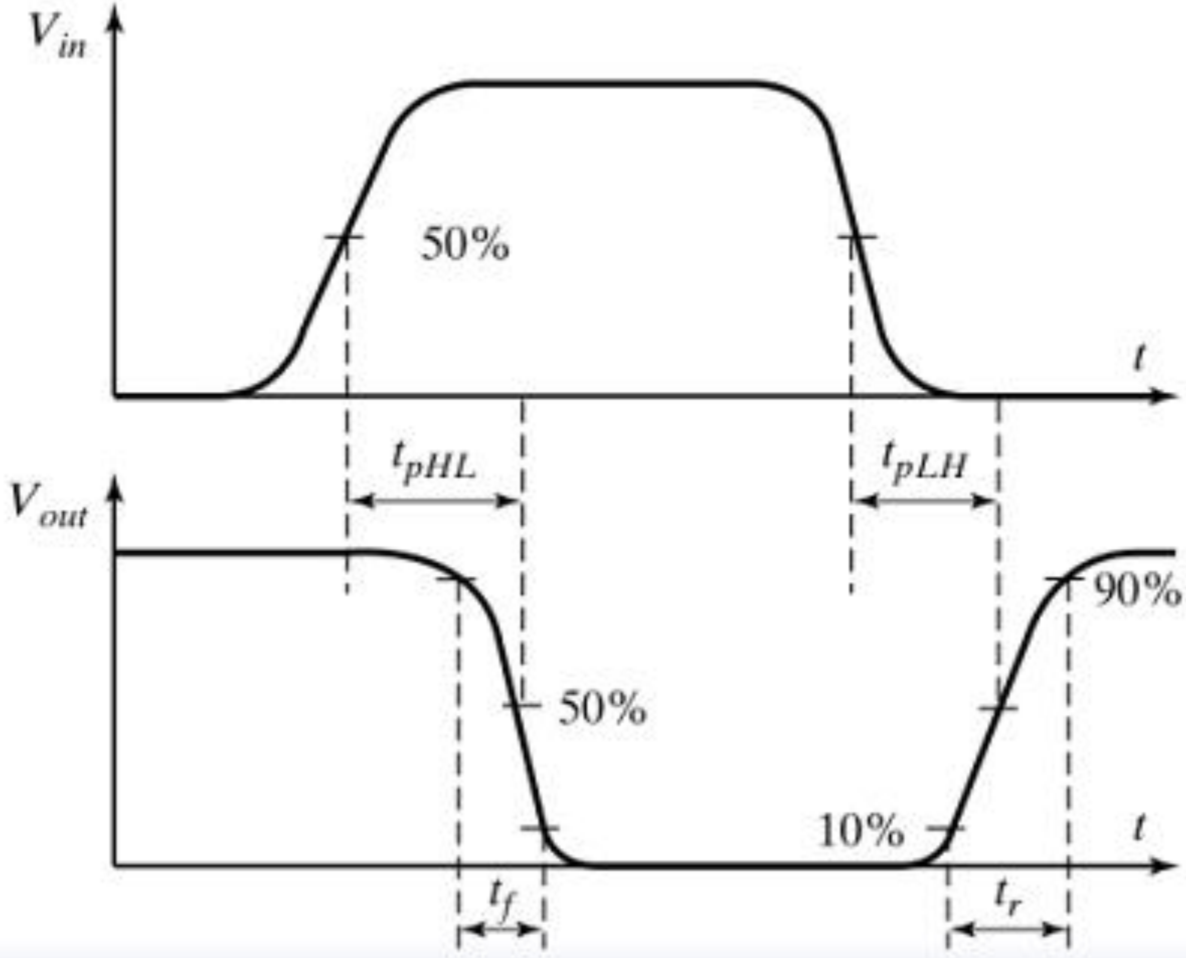
- Full rail-to-rail swing
- Symmetrical VTC
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation
- Direct path current during switching

Primary Performance Metric: Delay

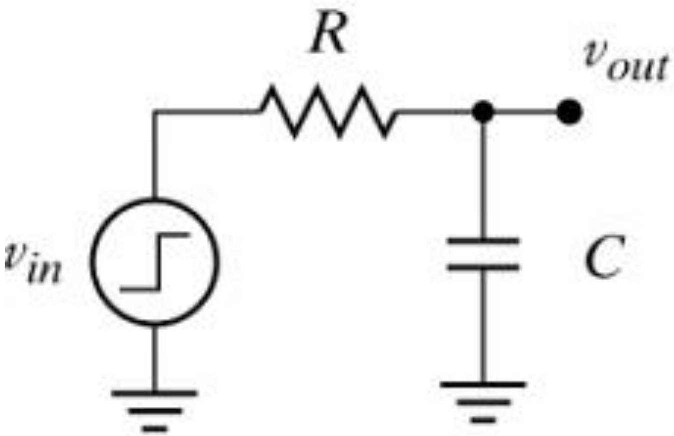


How to define delay in a universal way?

Delay Definitions



A First-Order RC Network



$$v_{out}(t) = (1 - e^{-t/\tau})\, V$$

↓

$$t_p = \ln(2)\,\tau = 0.69\, RC$$

Important model – matches delay of an inverter

Power Dissipation

Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply}i(t)$$

Peak power:

$$P_{peak} = V_{supply}i_{peak}$$

Average power:

$$P_{ave} = \frac{1}{T}\int_{t}^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_{t}^{t+T} i_{supply}(t)dt$$

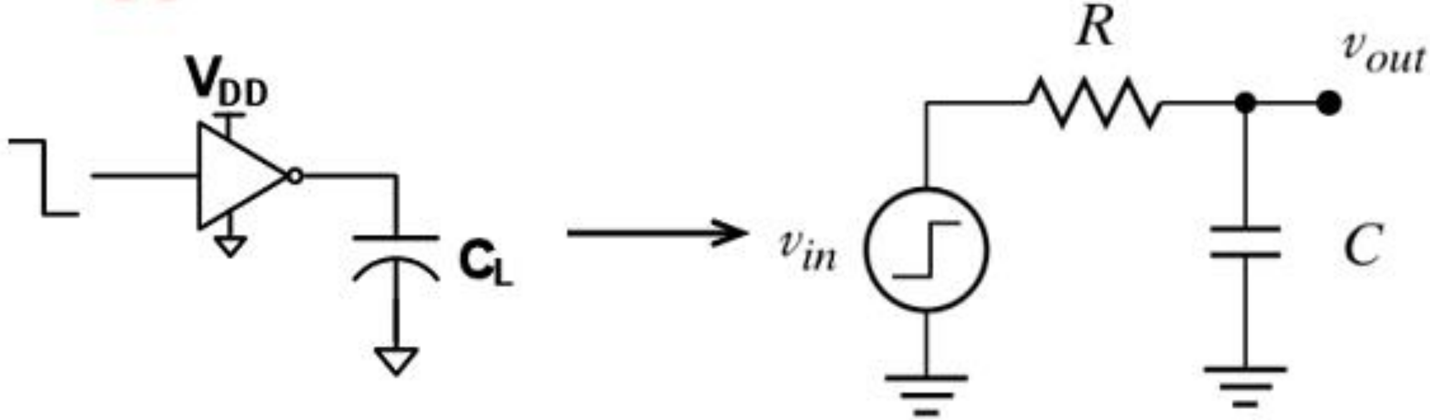
"Power-Delay" and Energy-Delay

- Want low power and low delay, so how about optimizing the product of the two?
  - So-called "Power-Delay Product"

- Power·Delay is by definition Energy
  - Optimizing this pushes you to go as slow as possible

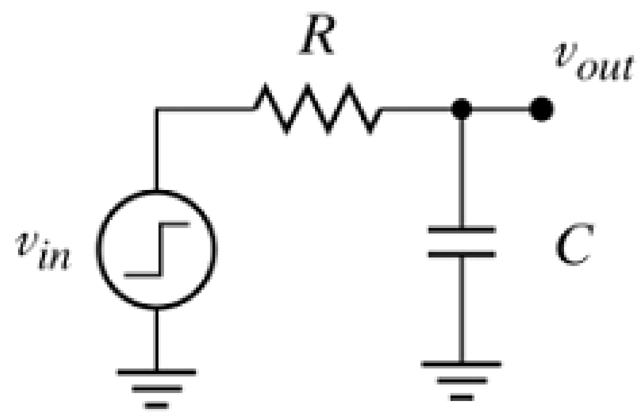
- Alternative gate metric: Energy-Delay Product
  - $EDP = (P_{av} \cdot t_p) \cdot t_p = E \cdot t_p$

Energy in CMOS



- The voltage on C_L eventually settles to V_{DD}
- Thus, charge stored on the capacitor is $C_L V_{DD}$
  - This charge has to flow out of the power supply
- So, energy is just $Q \cdot V_{DD} = (C_L V_{DD}) \cdot V_{DD}$

Energy



$$E_{0\to 1} = \int_0^T P_{DD}(t)dt = V_{DD}\int_0^T i_{DD}(t)dt = V_{DD}\int_0^{V_{DD}} C_L dv_{out} = C_L V_{DD}^2$$

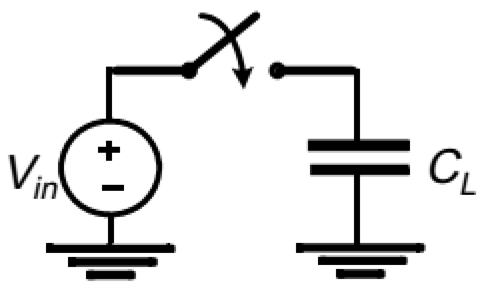
$$E_C = \int_0^T P_C(t)dt = \int_0^T v_{out} i_L(t)dt = \int_0^{V_{DD}} C_L v_{out} dv_{out} = \frac{1}{2} C_L V_{DD}^2$$

Energy Thought Experiment (1)

- Why doesn't R matter?

Energy Thought Experiment (2)

- Where did the energy go?



$$E_{Vin} = C_L V_{in}^2$$

$$E_{CL} = (1/2) C_L V_{in}^2$$