University of California
College of Engineering
Department of Electrical Engineering
and Computer Sciences

D. Markovic

TuTh 11-12:30

Thursday, December 15, 5:00-8:00pm

EECS 141: FALL 2005—FINAL

NAME	SOLUTION Last First

SID	

Problem 1 (7): 7

Problem 2 (9): 9

Problem 3 (15): 15

Problem 4 (11): 11

Problem 5 (10): 10

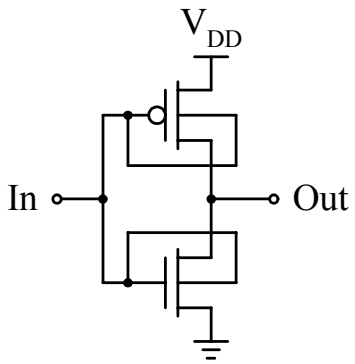
Problem 6 (8): 8

Problem 7 (15): 15

Total (75)	75

PROBLEM 1: Devices (7 pts)

Consider the inverter shown below.



Compared to an inverter of the same size with the bulk connections at GND (for the NMOS) and V_{DD} (for the PMOS), and connecting the gates to the bulk, how will the following parameters change? For each of the parameters place an "X" in the appropriate column of the table.

Parameter	Increase	Decrease	Stays the same	Cannot be determined
Input capacitance	X			
Intrinsic cap			X	(X)
Intrinsic delay		X		(X)
Inverter V_M			X	
Drive current	X			
Leakage current	X		(X)	
Switching energy	(X)		X	

Input cap increases due to added well-to-substrate cap needed to be driven by the input.

Intrinsic cap stays the same since the source/drain cap to bulk are not changed. (also accepted cannot be determined)

Intrinsic delay decreases since more drive current is available to drive the intrinsic load cap. (also accepted cannot be determined)

Inverter V_M stays the same since PMOS and NMOS current increase by the same amount.

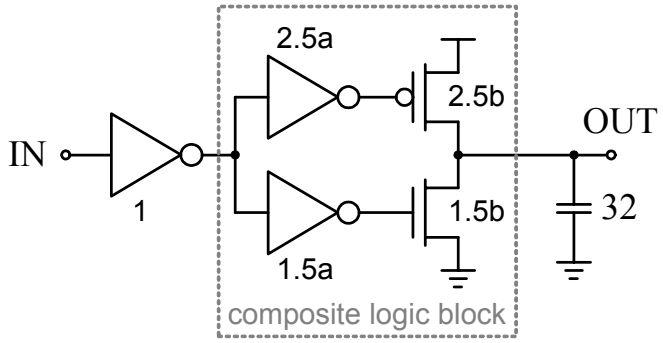
Inverter drive current increases due to the reduction in threshold voltage by forward body bias.

Inverter leakage current increases due to smaller effective threshold. (we also accept if you considered only off current and answered stays the same)

Switching energy stays the same since the intrinsic load cap is not changed. (also OK if you considered gate cap and answered increase)

PROBLEM 2: Logic (9 pts)

a. Find the logical effort of the composite logic block below. **(4 pts)**
Hint: consider path logical effort.



Parameters *a* and *b* don't affect LE.

Consider path effort to obtain LE.

H→L transition (OUT pull-down):
First stage LE = 1*(1+2.5/1.5) = 2.67
Second stage LE = 1/3
Total LE (H→L) = LE_1*LE_2 = 0.89

L→H transition (OUT pull-up):
First stage LE = 1*(1+1.5/2.5) = 1.6
Second stage LE = 2/3
Total LE (L→H) = LE_1*LE_2 = 1.07

We also accepted if you did not consider branching at first stage.
LE (H→L) = 1/3
LE (L→H) = 2/3

LE (H→L) = 0.89 (also accepted 1/3)
LE (L→H) = 1.07 (also accepted 2/3)

b. This logic block is placed in a circuit shown above. Write an expression for the propagation delay from input to output (the delay is normalized to t_{p0}). Assume $\gamma = 1$. **(3 pts)**

Use stage-based delay calculation approach.
Main point to realize is that parasitic cap of the second stage is different for L→H and H→L:
For L→H, we compare total output W to 2/1 inverter (2.5b/1.25b inverter for simpler calculation).
We get P (L→H) = 4b/3.75b = 16/15.
For H→L, we compare total output W to 2/1 inverter (3b/1.5b) and obtain P (H→L) = 4b/4. 5b = 8/9.

D (L→H) = (1+4a) + (1 + b/a) + (16/15 + 2/3*32/2.5b)
D (H→L) = (1+4a) + (1 + b/a) + (8/9 + 1/3*32/1.5b)

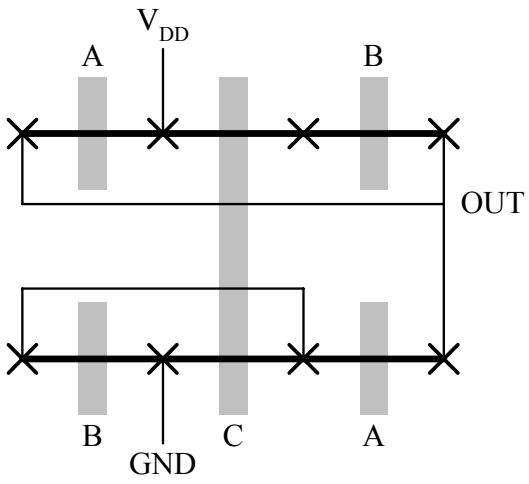
c. Find *a* and *b* for optimum t_{pLH}. **(2 pts)**

Take partial derivative of D(L→H) w.r.t. *a* and *b*.
$a = (8/15)^{1/3} = 0.81$, $b = 4a^2 = 2.62$
Observe that 1.5a > 1 (assuming min transistor size is 1)

a (L→H) = 0.81	b (L→H) = 2.62

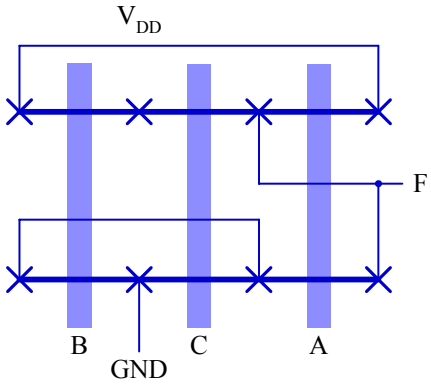
PROBLEM 3: Layout techniques (15 pts)

a. Write out the truth table that corresponds to the following stick diagram. **(2 pts)**



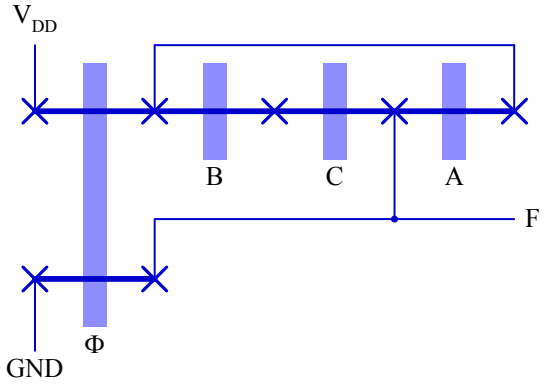
A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

b. Implement $F = \overline{AB+AC}$ in one diffusion region using stick diagram. Each gate must be used for both PMOS and NMOS. Use static CMOS. Clearly denote if crossing wires are connected or not. Use the fewest number of transistors possible. **(4 pts)**

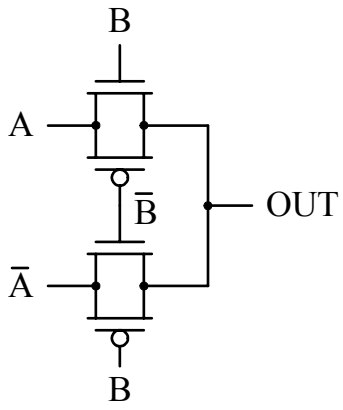


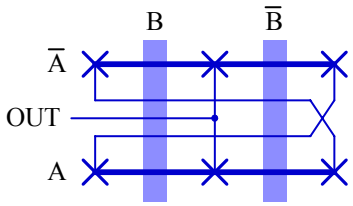
$F = \overline{A(B+C)}$

c. Repeat part (b) for dynamic CMOS using a PUN. All PMOS transistors must share one diffusion. **(3 pts)**



d. Implement the following circuit in stick diagram. Assume all inputs are given and do not break the diffusion. **(2 pts)**



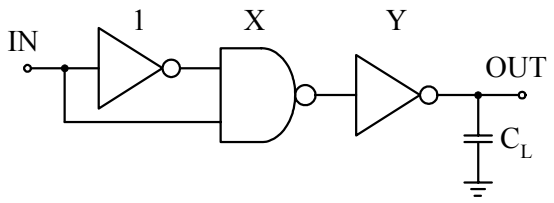


e. Fill out the table using only one word per entry. **(4 pts)**

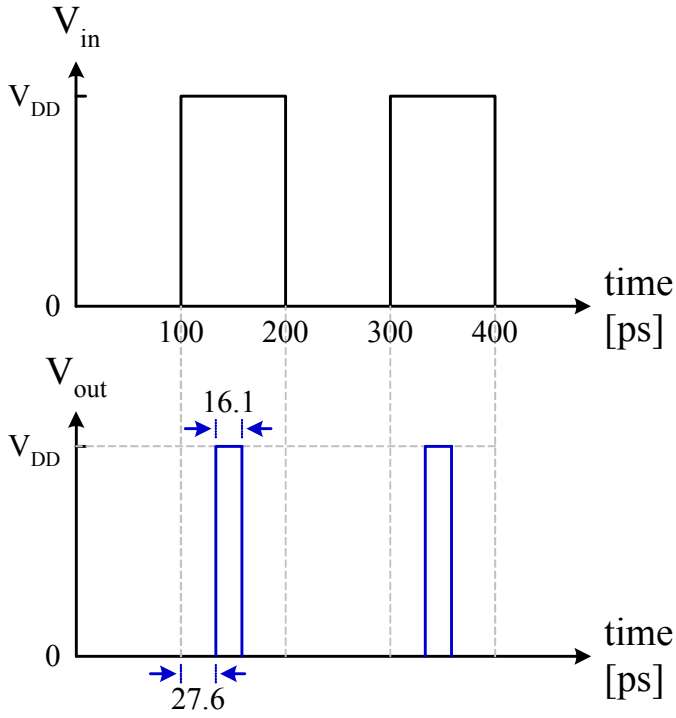
Logic Family	Advantage	Disadvantage
Standard CMOS	Robust	Area
Dynamic	Delay	Power
PTL	Area	Swing
RTL	Area	Power

PROBLEM 4: Sequential circuits and their building blocks (11 pts)

X and Y are the sizing factors. For the unit sized inverter assume $\gamma = 1$, $C_{in} = 2$ fF, $R_{eq} = 5$ KΩ.



a. Assume $C_L = 0$ and IN is a perfect 5 GHz clock with 50% duty cycle. Graph OUT and label important points on the x-axis. Do not label more than two points. X = Y = 1. **(4 pts)**



$t_{p0} = 0.69RC = 6.9$ps

Critical path delay (normalized to t_{p0}):
(1+4/3) + (2+1) + (0+1) = 6.33
$t_{p1} = 43.7$ps

Other path delay (normalized to t_{p0}):
(2+1) + (0+1) = 4
$t_{p2} = 27.6$ps

The difference determines pulse width: PW = $2.33t_{p0} = 16.1$ps

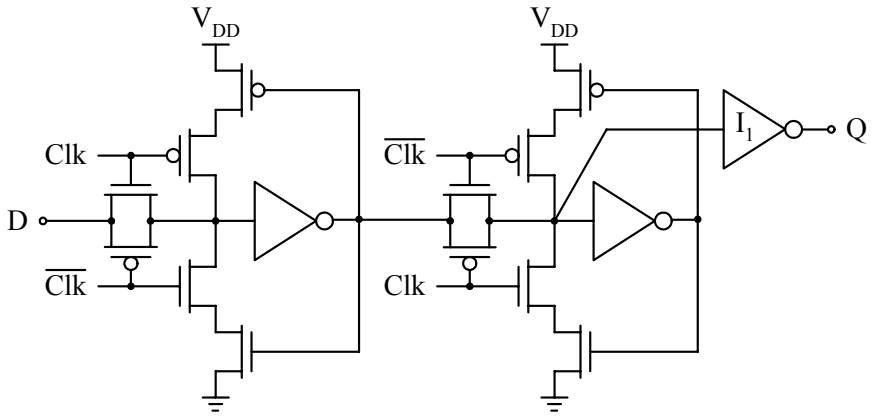
b. Assume C_L = 100 fF. Given IN is a perfect 500 MHz clock signal with 50% duty cycle. Size X and Y such that OUT is a 500 MHz clock signal with 10% duty cycle and minimized propagation delay. **(4 pts)**

Clock is high for 1ns, want 200ps: $t_{p0}*(1+4/3*X) = 200ps \Rightarrow X = 21$

For fixed X, delay is minimized when SE of the last two stages is equal: $SE_2 = Y/X$, $SE_3 = 50/Y$.
$Y = (21*50)^{1/2} = 32.4$

X = 21	Y = 32.4

c. What is the functionality of the circuit below? Why is it advantageous to implement its functionality in this manner? **(3 pts)**



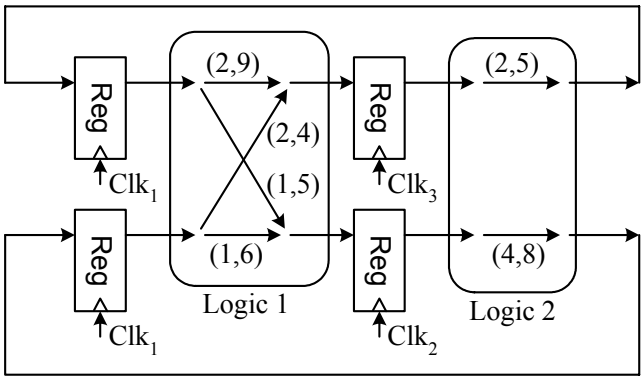
Functionality: flip-flop

Why is this circuit good: $C^2MOS \Rightarrow$ no skew

Main reason to use inverter I_1: buffer (avoid loading of state node)

PROBLEM 5: Timing (10 pts)

The notation for each path is (min-Delay, max-Delay).



The above is a register based system. The registers have following characteristics: (min-t_{CQ}, max-t_{CQ}) = (0.5, 2), t_{setup} = 1, t_{hold} = 1.

a. Assuming Clk_{1-3} have the same exact frequency and phase, determine the minimum T_{cycle} for this system. **(2 pts)**

T_{min} > max-CQ + max-Logic + max-t_{setup} = 2 +9 +1
T_{min} > 12

Min T_{cycle} = 12

b. If we use an arbitrary larger T_{cycle}, what is the maximum random clock skew ($|t_{skew}|$) between Clk_{1-3} that this system can tolerate? From calculated max($|t_{skew}|$), what is the minimum T_{cycle}? **(3 pts)**

min-Logic > t_{hold} – min-CQ + $|t_{skew}|$
case 1: btw Clk_1 and Clk_2
case 2: btw Clk_1 and Clk_2

2 > 1 – 0.5 + $|t_{skew}|$ ⇒ $|t_{skew}|$ < 1.5 (case 1)
1 > 1 – 0.5 + $|t_{skew}|$ ⇒ $|t_{skew}|$ < 0.5 (case 2) critical case

T_{min} > 12 – 0.5 = 11.5 for t_{skew} >0
T_{min} > 12 + 0.5 = 12.5 for t_{skew} <0

T_{min} > 12.5 to satisfy both inequalities

Max ($|t_{skew}|$) = 0.5	Min T_{cycle} = 12.5

c. Assuming no random skew, you are now permitted to adjust the timing of Clk_2 with respect to Clk_1 intentionally. What t_{skew21} would you choose to further reduce T_{cycle} (define t_{skew21} positive when Clk_2 arrives later than Clk_1)? What is the new minimum T_{cycle}? **(5 pts)**

For Logic 1: $t_{hold} + |t_{skew,\ Clk21}| < \text{min-CQ} + \text{min-Logic}$
$|t_{skew,\ Clk21}| < 0.5$

For Logic 2: $t_{hold} + |t_{skew,\ Clk21}| < \text{min-CQ} + \text{min-Logic}$
$|t_{skew,\ Clk21}| < 3.5$

Chose $|t_{skew,\ Clk21}| < 0.5$, to satisfy hold time constraints

If $t_{skew,\ Clk21} = 0.5$
For Logic 1: $T_{min} > 2 + 6 + 1 - 0.5 = 8.5$
For Logic 2: $T_{min} > 2 + 8 + 1 + 0.5 = 11.5$

If $t_{skew,\ ck21} = -0.5$
For Logic 1: $T_{min} > 2 + 6 + 1 + 0.5 = 9.5$
For Logic 2: $T_{min} > 2 + 8 + 1 - 0.5 = 10.5$

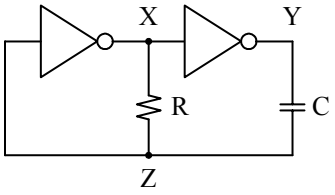
Check for Clk_1 to Clk_3 constraints:
$T_{min} > 2 + 9 + 1 - 0.5$
$T_{min} > 11.5$

Therefore: $T_{min} = 11.5$

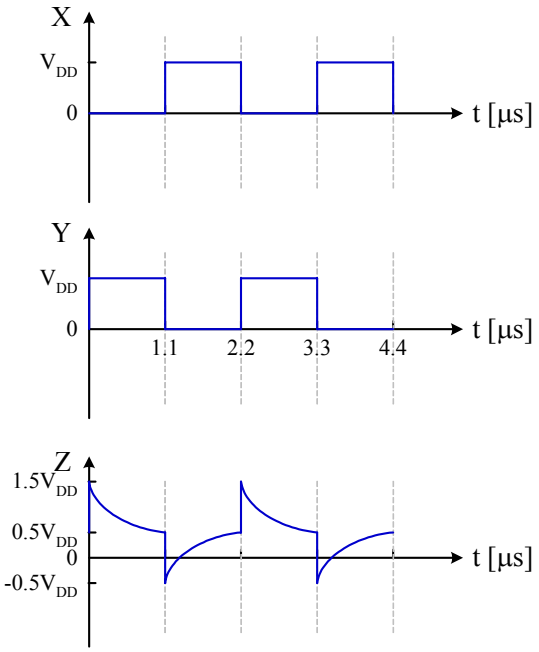
$t_{skew21} = 0.5$	Min $T_{cycle} = 11.5$

PROBLEM 6: Oscillator (8 pts)

Figure below shows a relaxation oscillator. Assume V_{DD} = 2.5V, R = 1kΩ, C = 1nF. Switching threshold of the inverters is $V_M = V_{DD}/2$.



a. Calculate and draw voltage waveforms at nodes X, Y, and Z using diagrams below. Clearly label time and voltage axes. **(6 pts)**



$V_C = V_Y - V_Z$
$\tau = RC = 1\mu s$

For Y = V_{DD}, X = 0:
$V_C(0) = -V_{DD}/2$, $V_C(\infty) = V_{DD}$
Switching point: $V_C(t) = V_{DD}/2$

For Y = 0, X = V_{DD}:
$V_C(0) = V_{DD}/2$, $V_C(\infty) = -V_{DD}$
Switching point: $V_C(t) = -V_{DD}/2$

$V_C(t) = V_C(\infty) + [V_C(0) - V_C(\infty)]*e^{-t/\tau}$

Half-period is given by:
$T_{half} = \tau * \ln 3$

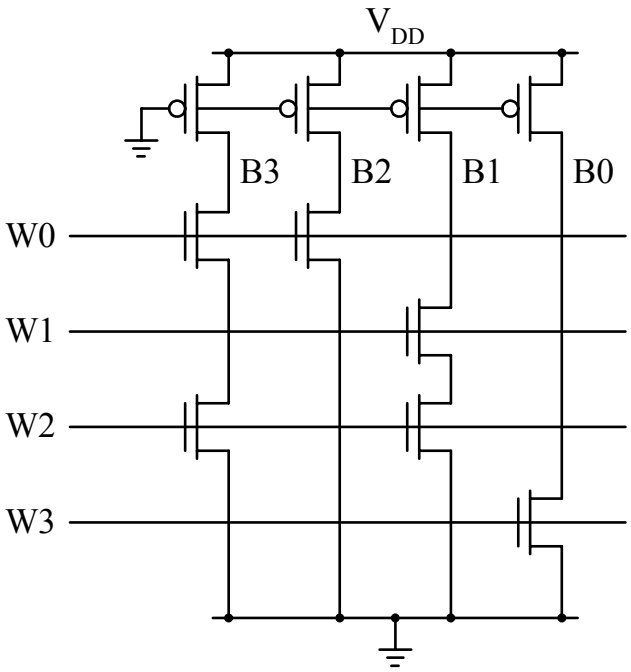
b. What is the oscillation frequency? **(2 pts)**

$1/f_{OSC} = T_{OSC} = 2RC*\ln 3 = 2.2\mu s$

f_{OSC} = 455 kHz

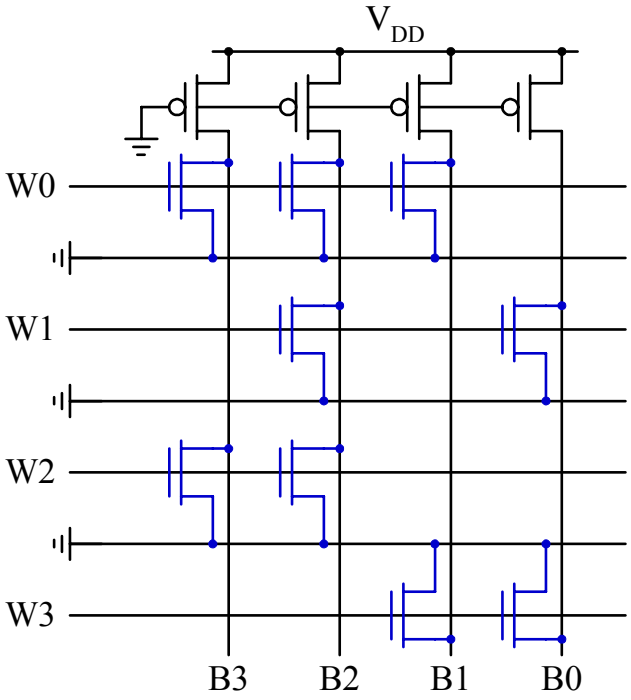
PROBLEM 7: Memory (15 pts)

a. What are the words stored in the NAND memory block. (MSB on the left) **(2 pts)**



W0	1100
W1	0010
W2	1010
W3	0001

b. Program the following NOR block by drawing transistors. (W = {B3, B2, B1, B0}) **(3 pts)**



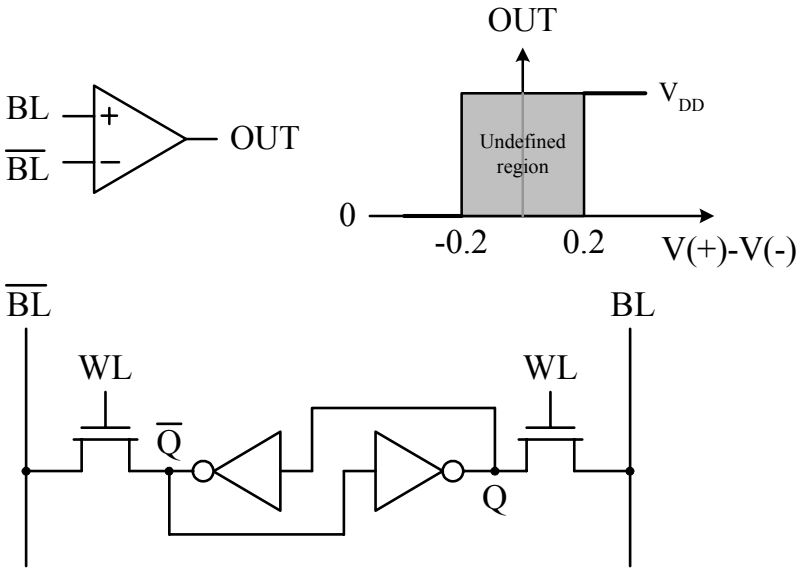
W0	0001
W1	1010
W2	0011
W3	1100

c. The advantage of NOR memory is speed.

The advantage of NAND memory is size. **(2 pts)**

d. The inverters have $W_p/W_n = 3\mu m/1\mu m$ and the other two transistors have width $0.5\mu m$. Assume 1,000 words are attached to each bit line. BL and $\overline{BL}$ are precharged to 0. The VTC for the sense amp is shown. In words, the amp's output become valid if the difference between the two inputs is greater than 0.2 volts. What is the read delay? For simplicity, calculate C_{eq} at the initial stage and assume it stays constant. **(5 pts)**

Refer to Table 3-2 on page 103 of text for MOS parameters. You can ignore bulk capacitance and use $\varepsilon_{ox} = 3.5 \cdot 10^{-11}$ F/m, $t_{ox} = 10$nm, $C_{overlap} = 0.1$ fF/μm, L = 0.25μm.



$C_L = 1{,}000 * [(1/2\mu m * 0.1\ fF/\mu m) + (2/3 * 1/2\mu m * L * E_{ox}/t_{ox})] = 342\ fF$
$V_M = 0.2V$

Smaller transistor is in velocity saturation/saturation the whole time.
$I_{DS}(initial) = 0.254\ mA$
$I_{DS}(final) = 0.225\ mA$
$R_{eq} = ½ * (2.5/0.254mA + 2.3/0.225mA) = 10k\Omega$
$T_{read} = - RC \ln (2.3/2.5) = 2.85 * 10^{-10} \sim 285\ ps$

$T_{read} = 285\ ps$

e. Repeat part d but BL and $\overline{BL}$ are precharged to $V_{DD}/2$. **(3 pts)**

NMOS is pulling down while PMOS is pulling up. Assume each node change by 0.1V. This is a conservative estimate.

For pull-up:
C_L = 1,000 * (0.5μm * 0.1 fF/μm) = 50 pF
NMOS in velocity saturation the whole time.
I_{DS}(initial) =70 μA
I_{DS}(final) = 48 μA
R_{eq} = 20.7 kΩ
T_{read} = RC ln (1.25/1.15) = 86.3 ps

For pull-down:
No C_{gd}
C_L = 1,000 * (0.5μm * 0.1 fF/μm) = 50 pF
NMOS in velocity saturation the whole time.
I_{DS}(initial) = 285 μA
I_{DS}(final) = 285 μA
R_{eq} = 4.2 kΩ
T_{read} = RC ln (1.25/1.15) = 17.5 ps

T_{read} = 51.9 ps