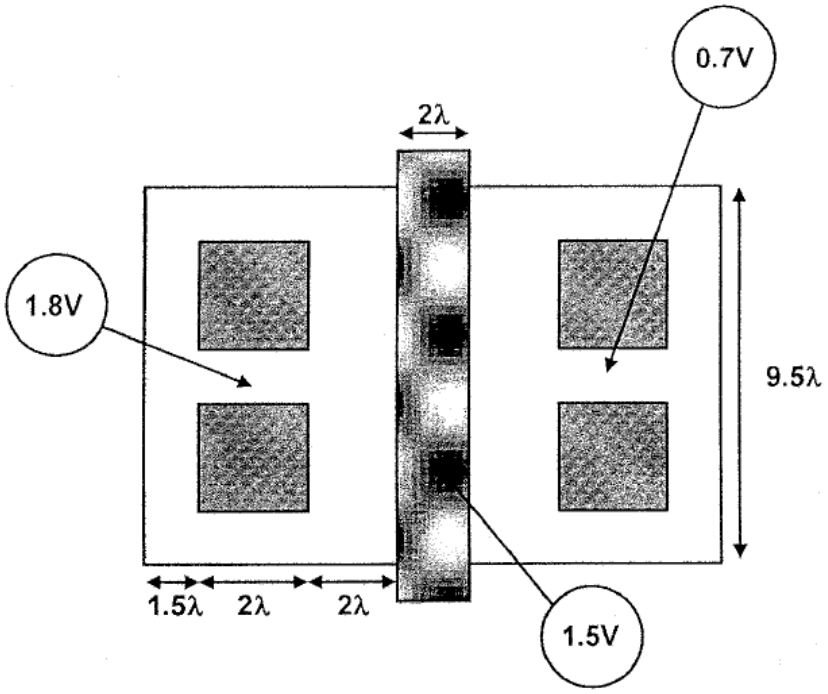
Problem 1 Consider the NMOS transistor layout and voltage biases shown in Figure 1. Suppose we know that for the NMOS under bias, $V_{T0,n} = 0.3\text{V}$, minimum feature size $2\lambda = 2 \times 90\text{nm}$, $\gamma = 0.27\text{V}^{1/2}$, channel length modulation factor $\lambda = 0\ \text{V}^{-1}$, $\mu C_{ox} = 299\ \mu\text{A/V}^2$, and $-2\Phi_F = 0.6\ \text{V}$. Assume the bulk node of the transistor is at 0V. Find the drain-source current I_{DS}.

Hint: Need threshold $V_{Tn} = V_{Tn\phi} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$



Sol:

$V_G = 1.5\text{V}$ $V_D = 1.8\text{V}$ $V_S = 0.7\text{V}$ $V_B = 0\text{V}$

D 1.8V, I_{DS}, 1.5V G, B, S 0.7V (2pt.)

$V_{Tn} = V_{Tn\phi} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$ $V_{SB} = 0.7\text{V}$ (1pt.)

$= 0.3\text{V} + (0.27\text{V}^{1/2})\left(\sqrt{|0.6\text{V} + 0.7\text{V}|} - \sqrt{0.6\text{V}}\right)$ (1pt.)

$= 0.3987\ \text{V} \approx 0.4\text{V}$ (1pt.)

$V_{GS} = 0.8\text{V} > V_{Tn} = 0.4\text{V}$ (1pt.)

$V_{DS} = 1.8\text{V} - 0.7\text{V} = 1.1\text{V} > V_{GS} - V_{Tn} = 0.4\text{V}$

sat (1pt.)

$I_{DS,n} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{Tn})^2(1 + \lambda V_{DS})$ (2pt.)

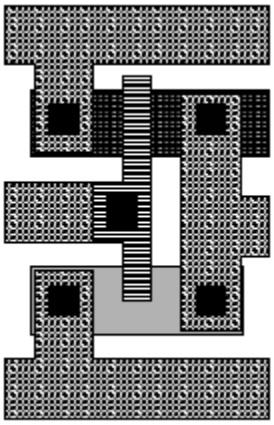
$= \frac{299\ \mu\text{A/V}^2}{2}\left(\frac{9.5}{2}\right)(0.8\text{V} - 0.4\text{V})^2$ (1pt.)

$= 114.4\ \mu\text{A}$

$= \boxed{114\ \mu\text{A}}$ (1pt.)

Problem 2

What type of logic function does this layout implement? Point out the three largest problems with this layout. For each explain the impact on gate behavior.



Inverter

The bottom half of the NMOSFET gate is missing.

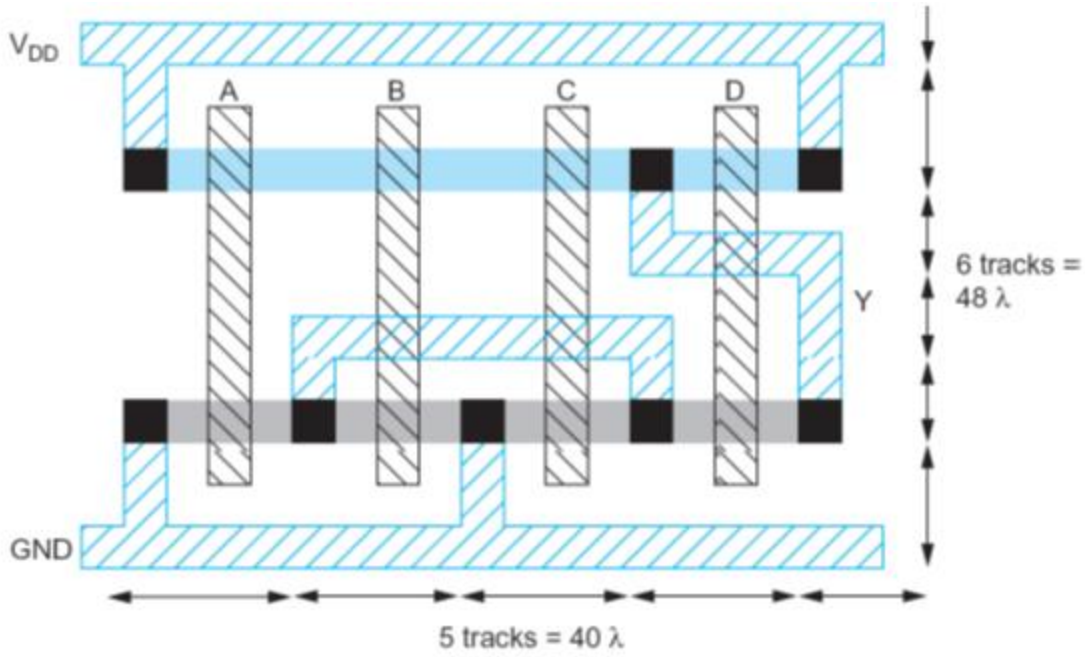
ii. The PMOSFET drain is bigger than it needs to be, increasing capacitance without bene_t.

iii. The NMOSFET and PMOSFET active regions are the same width, which would result in asymmetric pull-up and pull-down resistances if the gates were designed correctly.

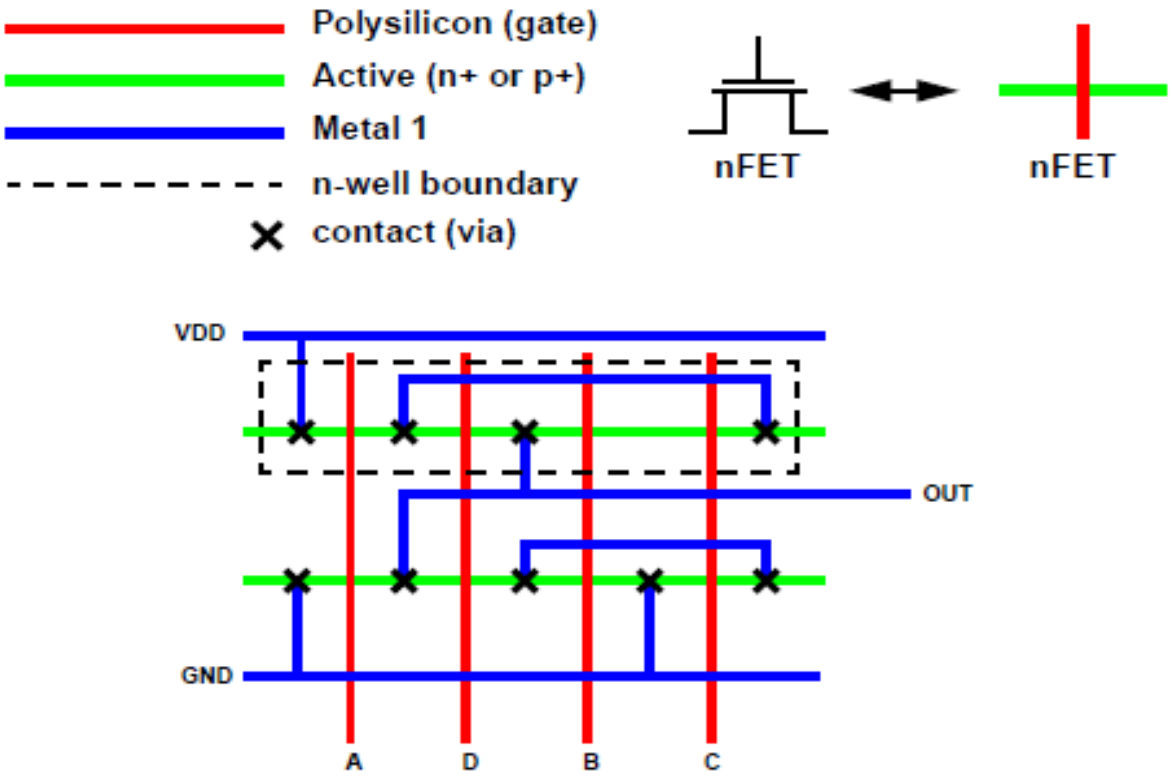
Problem 3:
What function does this layout represent?
How many Metal 1 track in horizontal and vertical direction we have ?

CMOS compound gate for function $Y = \overline{(A + B + C) \bullet D}$

5 vertical and 6 horizontal



Problem 4:
Given the following stick diagram, what is the function ?
Or I could give you the function and ask about the stick diagram
Or I could give you schematic and ask for stick diagram



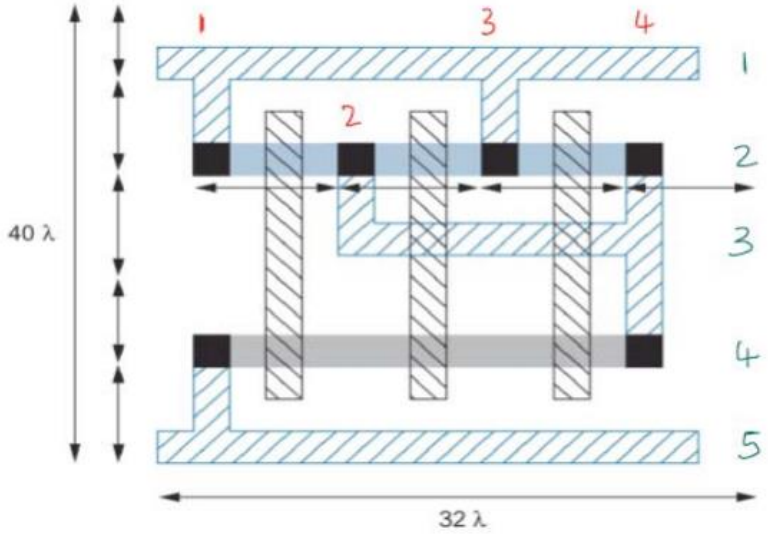
Proplem 6:
What is a design rule ? is it the same for all process /technology ?
Who generate the design rules ? is it the circuit designer or process engineer ?

Problem 7:
Draw detail inverter layout and mark/name all metal1, contact, pdif, ….a as in lect6

Problem 8:
How do you estimate size of cell like

Area Estimation

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in λ



Horizontal
4×8 = 32

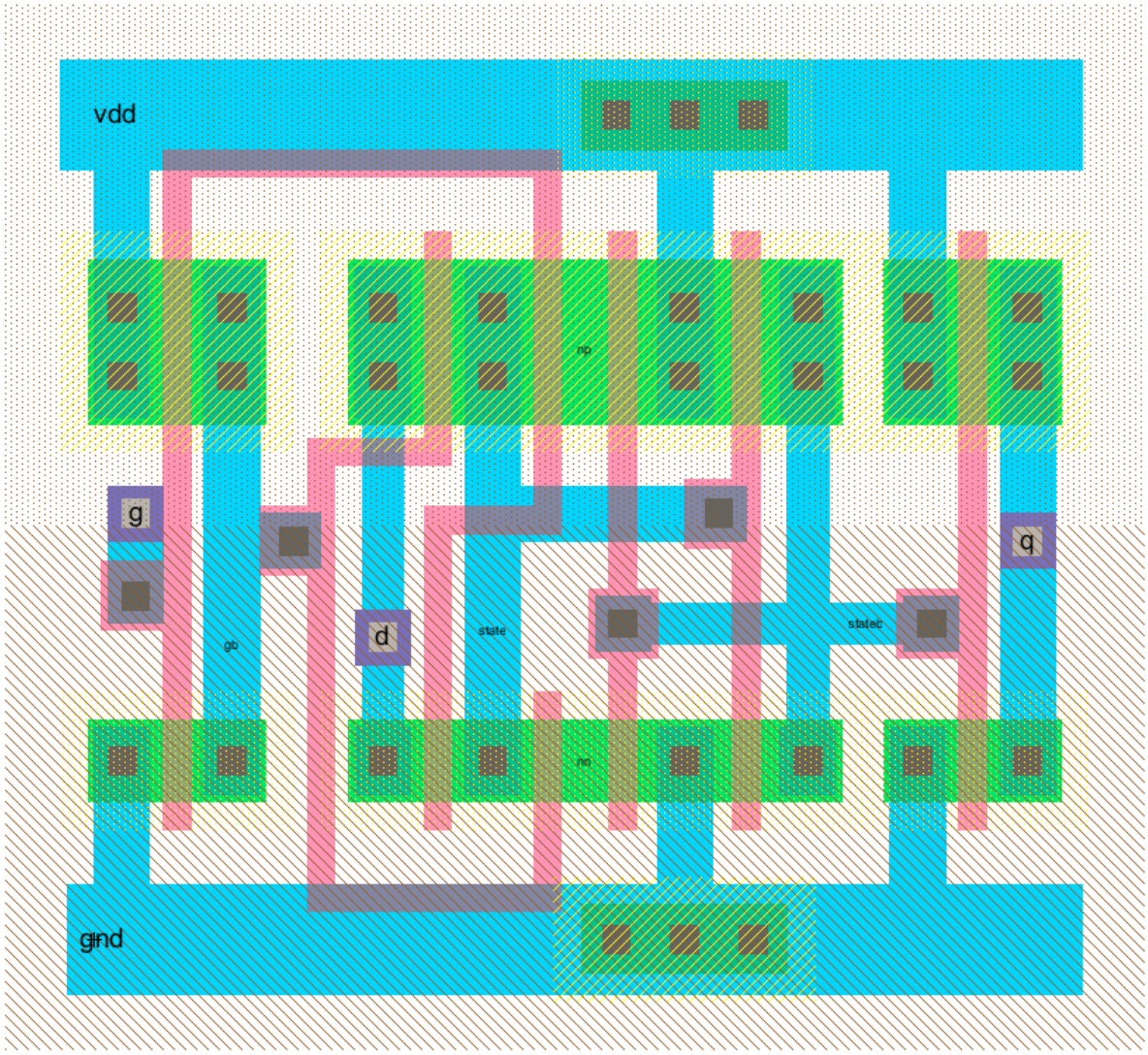
Vertical
5×8 = 40

Problem 9:

As in slides, Draw stick diagram for this cell /function

Proplem 10

Sketch the corresponding schematic for the following layout. Make sure the body connections of the MOSFETs are clearly seen in your schematic.


vdd
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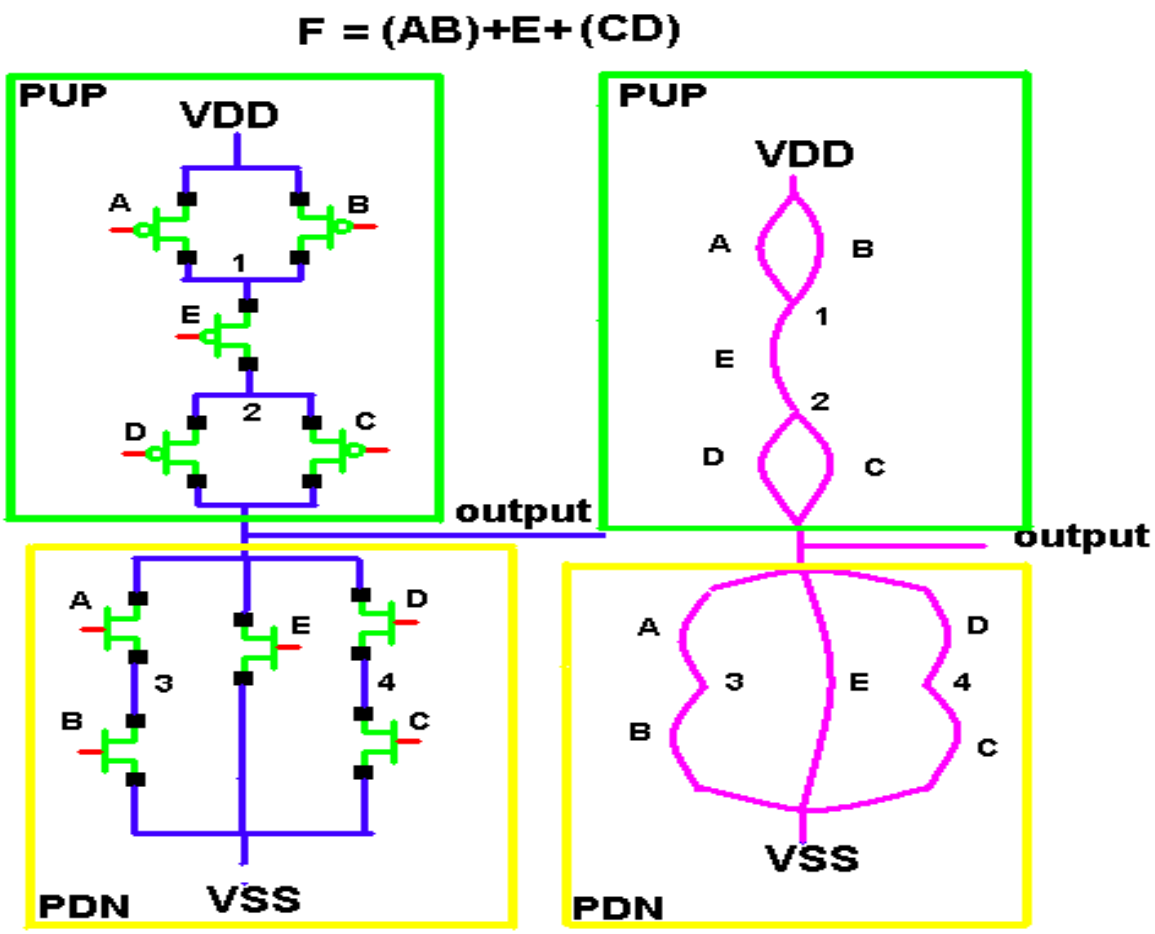

Problem 10

1. Why NMOS technology is preferred more than PMOS technology?

N- channel transistors has greater switching speed when compared tp PMOS transistors.

2.What is Stick Diagram?

It is used to convey information through the use of color code. Also it is the cartoon of a chip layout.

27.What are the uses of Stick diagram?

_ It can be drawn much easier and faster than a complex layout.

_ These are especially important tools for layout built from large cells.

28.Give the various color coding used in stick diagram?

_ Green – n-diffusion

_ Red- polysilicon

_ Blue –metal

_ Yellow- implant

_ Black-contact areas.