**ENCS333**

**Homework 1**

**Due October 31ST**

1. Please watch below videos and answer What is a CMOS? [NMOS, PMOS]

Watch this vedio :

Ref1: <https://www.youtube.com/watch?v=docgmTprR5o>

Ref2: https://www.youtube.com/watch?v=\_SwY-WfWTQo

1. Please watch below videos and search about CMOS IC fabrication and then list the basic steps for CMOS IC fabrication?

* Ref 1: <https://www.edgefx.in/understanding-cmos-fabrication-technology/>
* Ref2: <https://www.youtube.com/watch?v=tggM3tZYRAA>

1. Step One:
   * Wafer Production
   * **Epitaxial growth**
2. **Step Two:**

**Masking: To protect other parts of wafers when working on specific place or area of the wafer**

1. Etching
   * It removes material selectively from the surface of wafer to create patterns. The pattern is defined by etching mask. The parts of material are protected by this etching mask
2. Step 4:

* Doping:

To alter the electrical character of silicon, atom with one less electron than silicon such as boron and atom with one electron greater then silicon such as phosphorous are introduced into the area.

* **Atomic diffusion**

In this method p and n regions are created by adding dopants into the wafer. The wafers are placed in an oven which is made up of quartz and it is surrounded with heating elements.

* **Ion implantation**

This is also a method used for adding dopants. In this method, dopant gas such as phosphine or boron trichloride will be ionized first. Then it provides a beam of high energy dopant ions to the specified regions of wafer

1. Step 5

* Metalization

It is used to create contact with silicon and to make interconnections on chip. A thin layer of aluminum is deposited over the whole wafer. Aluminium is selected because it is a good conductor, has good mechanical bond with silicon, forms low resistance contact and it can be applied and patterned with single deposition and etching process.

* **Assembly and packaging**

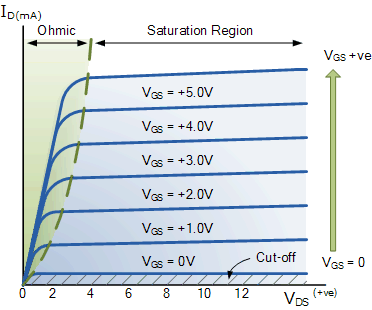
Each of the wafers contains hundreds of chips. These chips are separated and packaged by a method called scribing and cleaving. The wafer is similar to a piece of glass.

1. There are two types Types of transistor : P channel and N channel semiconductor devices OR PMOS or NMOS, Explain the Working Region of both devices

NMOS is layed on p-type substrate while PMOS is layed on N-type substrate, PMOS majority carriers are holes, NMOS majority carries are electrons, and NMOS is faster but, not immune to NOISE as PMOS.

Working Region of PMOS is the same as NMOS, but with negative VGS

Working Region of NMOS:



NMOS Works when a voltage is applied to the gate corresponds to the following

NMOS:

Vgs < Vt                                     OFF

Vds < Vgs  -Vt                         LINEAR

Vds > Vgs – Vt                        SATURATION

PMOS Works when a voltage is applied to the gate corresponds to the following

PMOS

Vsg < |Vt|                                 OFF

Vsd < Vsg – |Vt|                    LINEAR

Vsd > Vsg – |Vt|                    SATURATION

1. What are the main IC parasitic? What are the main IC Characteristics?

And how does the parasitic affect the characteristics

1. Inductance 2. Capacitance 3. Resistance

**Power , Area, speed, timing**

1. Explain What do we mean by process node? And how does that affect IC characteristics
   * The technology node (also process node, process technology or simply node) refers to a specific [semiconductor manufacturing process](https://en.wikichip.org/w/index.php?title=semiconductor_manufacturing_process&action=edit&redlink=1) and its design rules.
   * Different nodes often imply different circuit generations and architectures. Generally, the smaller the technology node means the smaller the feature size, producing smaller transistors which are both faster and more power-efficient. Historically, the process node name refered to a number of different features of a transistor including the [gate length](https://en.wikichip.org/w/index.php?title=gate_length&action=edit&redlink=1) as well as M1 half-pitch
2. Ic flow

