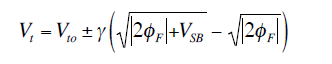
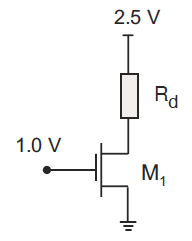


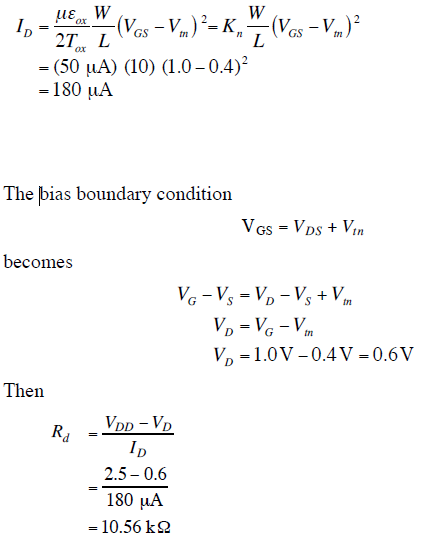
Kn as a current drive symbol for nMOS transistors



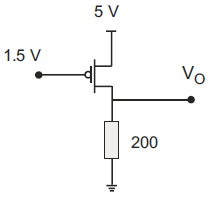
Q1: What value of *Rd* will drive transistor M1 just at non-saturation if *Kn* = 50 μA/V2, *Vtn* =

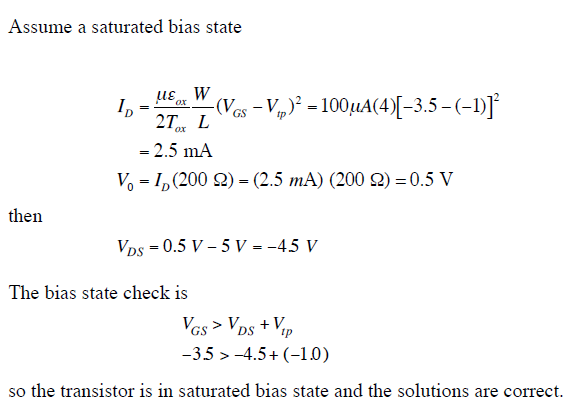
0.4 V, and *W/L* = 10?



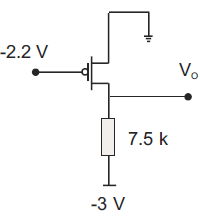


Q2: Calculate *ID* and *VDS* for *Vtp* = –1.0 V, *Kp* = 100 μA/ V2, and *W/L* = 4.



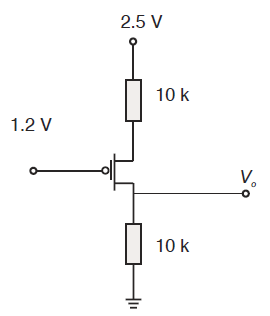


Q3: Find ID and VO for Vtp = –0.6 V, Kp = 20 μA/V2 , and W/L = 3



*Answer*: *ID* = 153.6 μA, *VO* = -1.848 V

Q4: Calculate ID, VDS , and verify the assumed bias state of transistor M1 for Vtp = –0.4 V, Kp = 60 μA/V2, and W/*L =2*



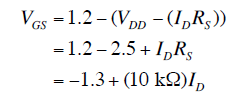
Assume a saturated bias state and



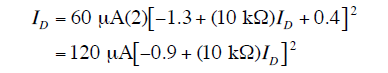
Since *VGS* is not known, we must search for another expression to supplement this

equation.

We can use the KVL statement

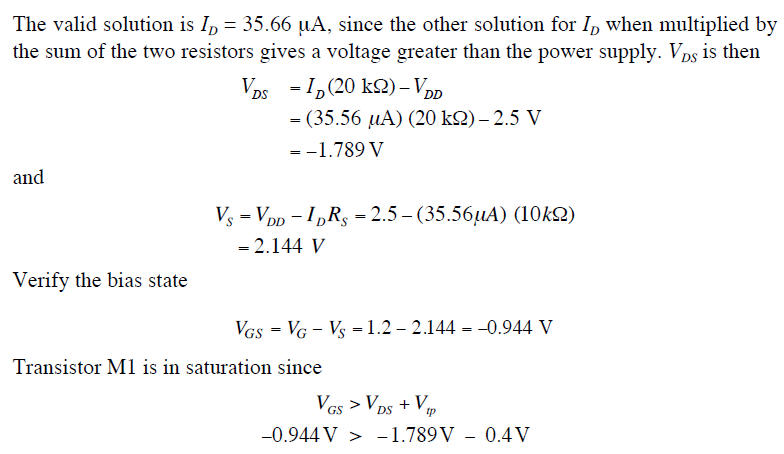


We substitute this into the saturated current expression to get



This quadratic equation in *ID* gives solutions





Q5: which region of the iv curve determine delay?

Linear

Q6:How can that match with RC ?

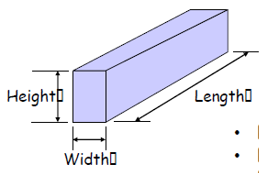
As ron larger , slow , more delay

Q7: answer the following question:

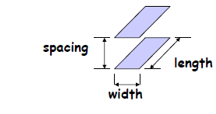
1. Describe the basic components of a CMOS transistor?

Drain/source/gate/sio2 …

1. Draw a CMOS invertor and regions of operation
   1. See notes
2. why do VLSI chips have multiple metal layers? What are these used for? Why so many?
   1. To make connections between devices
3. What is drive strength?
   1. Driver has raise/fall time proportional to the load
4. Are N and P devices sized the same? Why ?
   1. No, p twice N
5. How do you measure wire delay ? SLOPES?
   1. 50% OF THE SIGNAL
6. Effect of wires dimensions on cap and resistance?
   1. SEE NOTES
7. Current flow in CMOS? From where to where?
   1. Nmos d🡪s
8. What is delay of logic cell? Where the delay of net comes from?
   1. Parasatics R/C
9. If you have wire as in the figure below, How do you calculate its resistance?

* 
  + SEE NOTES

1. If we have 2 wires (plates as in figure beow, how do you calculate the capacitance between them ?

* 

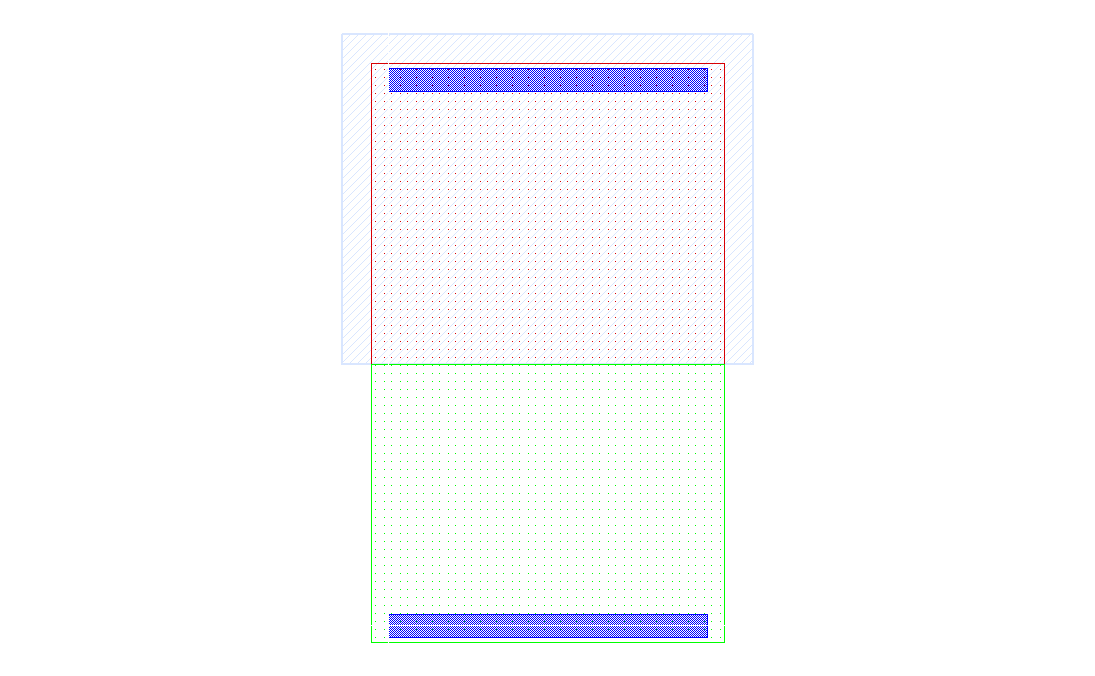
SEE NOTES

**Laboratory tasks**

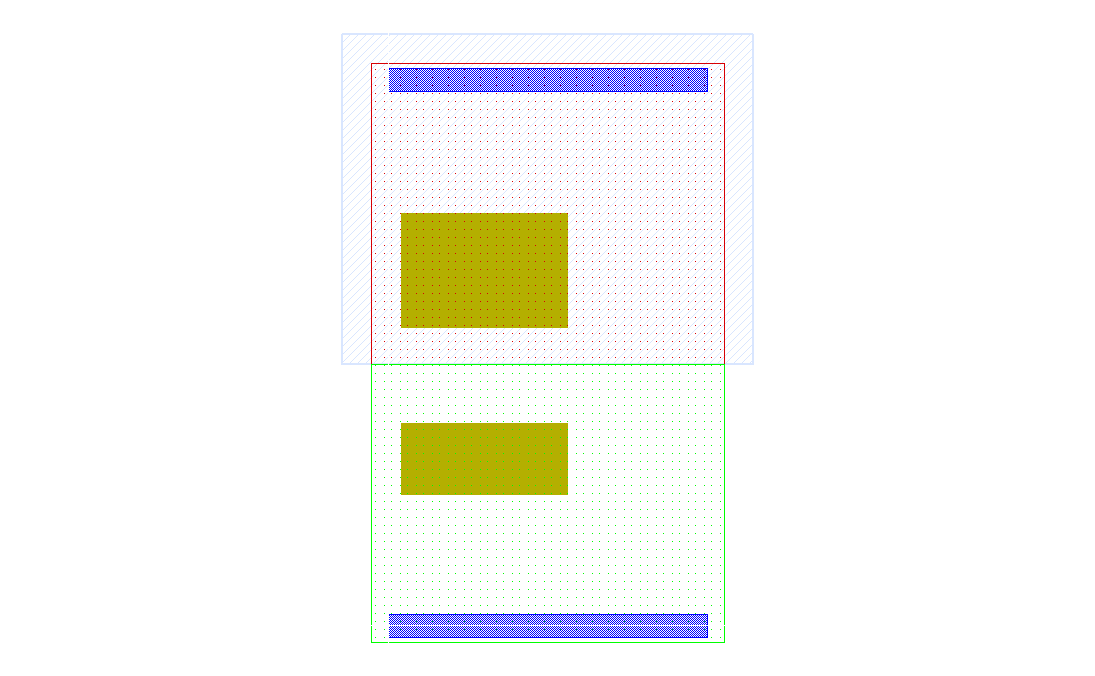
**What you need to turn in with the HW**

1. Layout screenshot
2. Power
3. Area of the cell
4. Create layout CellView for Cell Nand .

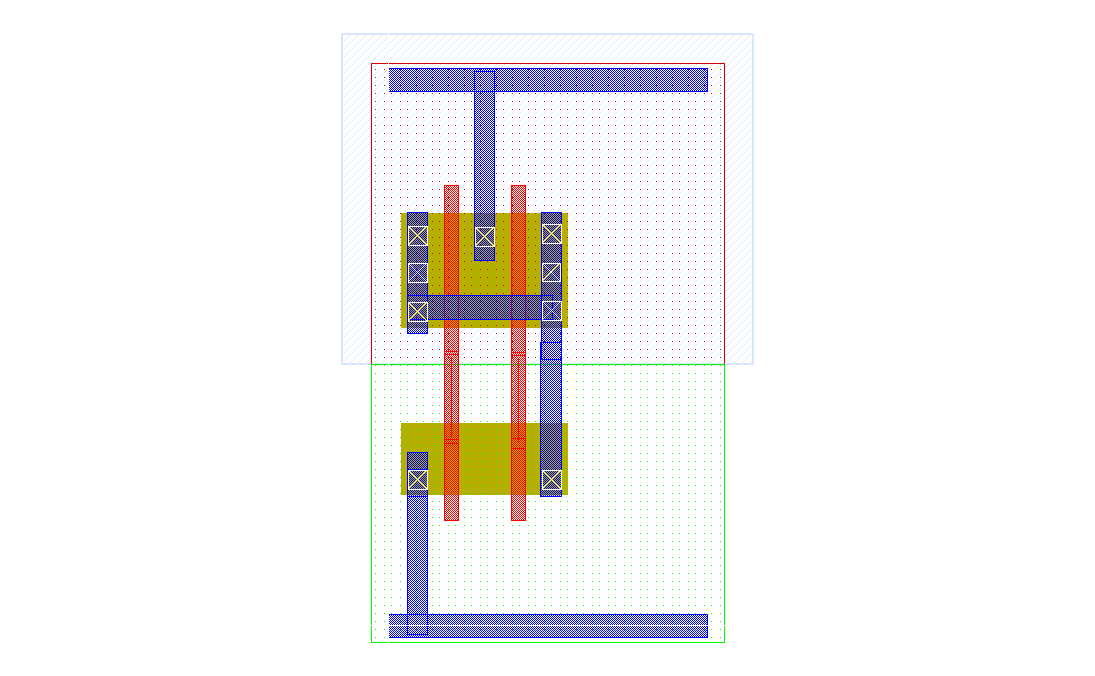
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Fig. 2.1. A fragment from Nand circuit layout

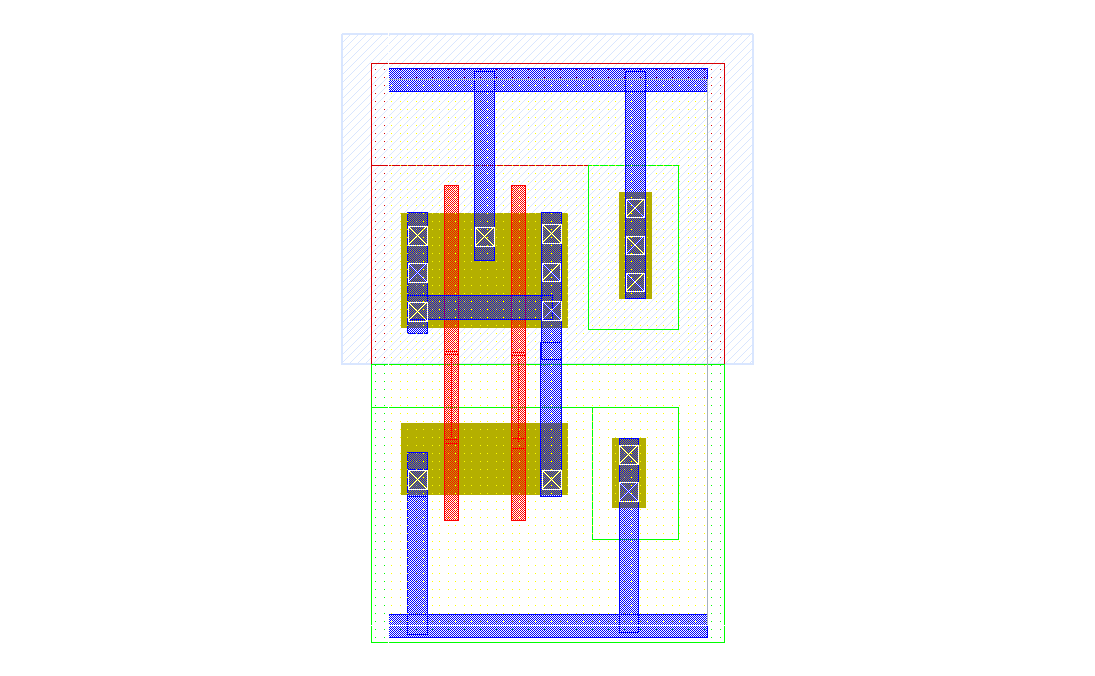
Choose layer DIFF and draw rectangles sized and place it

Fig. 2.2. A fragment from Nand circuit layout

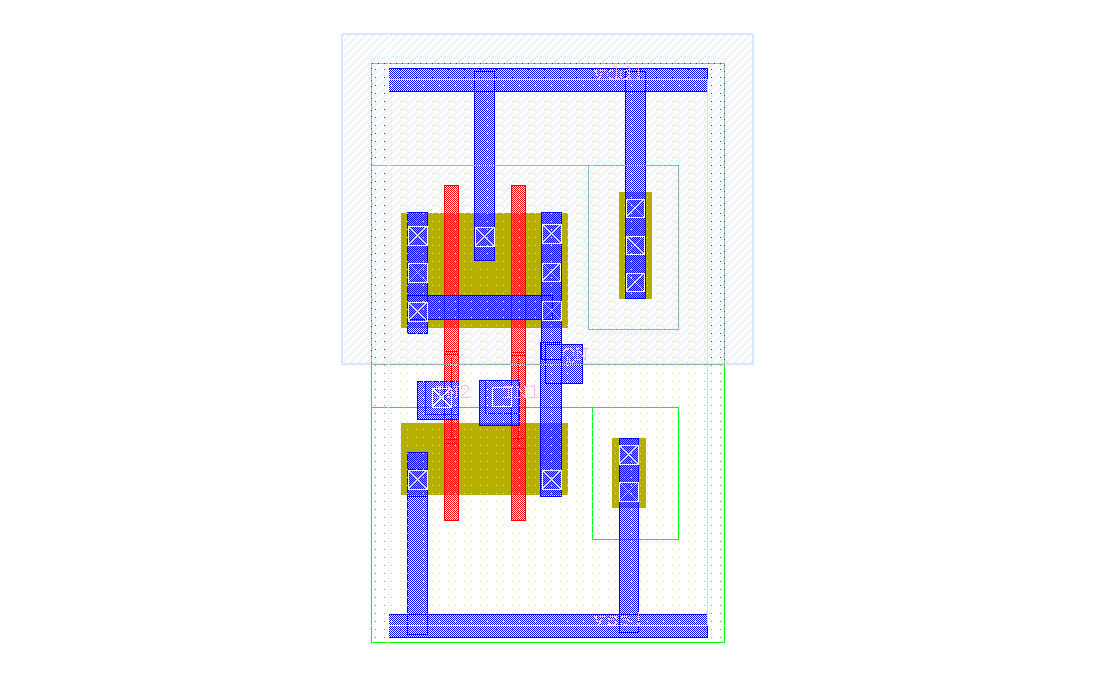
After creating contacts with the layer CO create paths with the M1 layer using Complete part of the circuit Nand layout as shown in Fig. 2.3.

 Fig. 2.3. A fragment from Nand circuit layout

Create polycontact layout looks like Fig. 2.4.

Fig. 2.4. A fragment from Nand circuit layout

Create pins Nand circuit layout is shown in Fig. 5.

Fig. 2.5. Final layout view of Nand circuit

Save the cell.

* 1. Physical Verification Invoke the DRC setup window and make sure no errors