



Faculty Of Information Technology
Electrical and Computer Engineering Department
DIGITAL INTEGRATED CIRCUITS (ENCS333)
Homework#1

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Section 2

Due to:19-2-2019

Question #1:

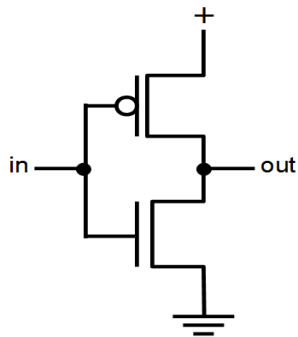
CMOS: is a complementary metal oxide semiconductor. used to perform logical functions. Consist of two types of MOSFET transistors: PMOS, NOMS.

It works as Inverter:

Input: 0 >> Output: 1.

Input: 1 >> Output: 0.

Symbol:

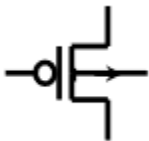


PMOS: P-channel MOS is played on N-type substrate, PMOS majority carriers are holes.

Input: Low >> Output: High.

Input: High >> Output: Low.

Symbol:

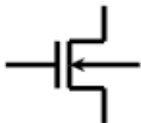


NMOS: N-channel MOS is played on P-type substrate, NMOS majority carries are electrons.

Input: Low >> Output: Low.

Input: High >> Output: High.

Symbol:



Question #2:

IC fabrication steps:

1. Wafer production.
2. Masking.
3. Etching.
4. Doping.
5. Metallization.
6. Assembly and packaging.

Question #3:

Working Region of PMOS is the same as NMOS, but with negative V_{gs} .

NMOS:

When ($V_{gs} < V_t$) \gg Off.

When ($V_{ds} < V_{gs} - V_t$) \gg Linear.

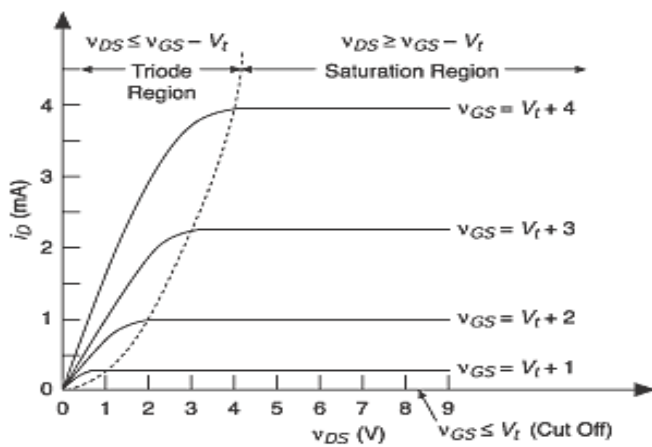
When ($V_{ds} > V_{gs} - V_t$) \gg Saturation.

PMOS

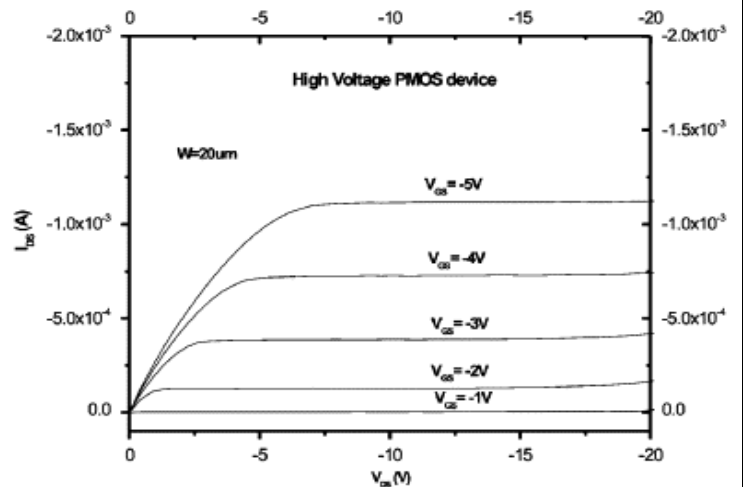
When ($V_{sg} < |V_t|$) \gg Off.

When ($V_{sd} < V_{sg} - |V_t|$) \gg Linear.

When ($V_{sd} > V_{sg} - |V_t|$) \gg Saturation.



‘NMOS’



‘PMOS’

Question #4:

The main IC parasitic: Resistance, Inductance, Capacitance.

The main IC Characteristics: Power, Area, speed, timing.

How does the parasitic affect the characteristics?

The answer is:

At first, there is a relation between frequency and (L, C). since, in high frequencies, Capacitance parasitic appears clearly the same with Inductance. Now, the relation between the length of device's channel and the resistance is opposite. When the length is large then the resistance will be smaller and this length or process can effect on power, area and speed. For example: when we choose L (process) smaller then we get >> less area, speed faster, cost less bur the complexity will increase. R and C affect the timing analysis since the constant time (τ) = RC and the power (P) = $I^2 \cdot R$.

Question #5:

The process node: is a standardized process used across a wide range of products. Standardizing the process for multiple products makes yield and process improvement much easier, since the same resources can solve complex problems.

Technology scaling: The scaling theory developed by Mead and Dennard allows a “photocopy reduction” approach to feature size reduction in CMOS technology, and while the dimensions shrink, scaling theory causes the field strengths in the MOS transistor to remain the same across different process generations.

Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months. 1 He made a prediction that semiconductor technology will double its effectiveness every 18 months.

Technology Scaling Models: - Full Scaling (Constant Electrical Field) -Fixed Voltage Scaling - General Scaling ideal model.

Question #6:

