* Lab1\_Solution:

1. Design 2 input NAND gate using transistors:

* Schematic:

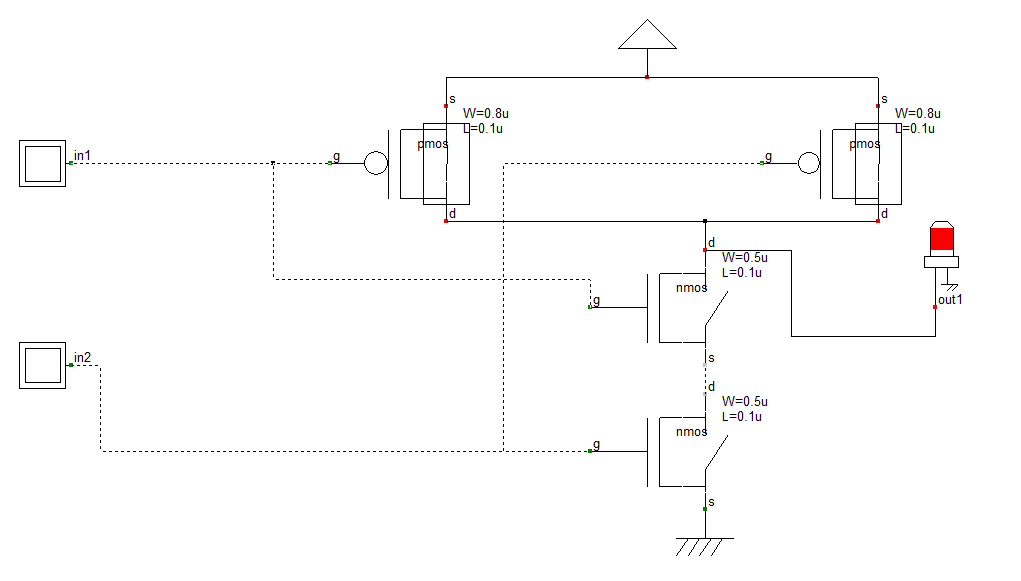


Fig 1.1

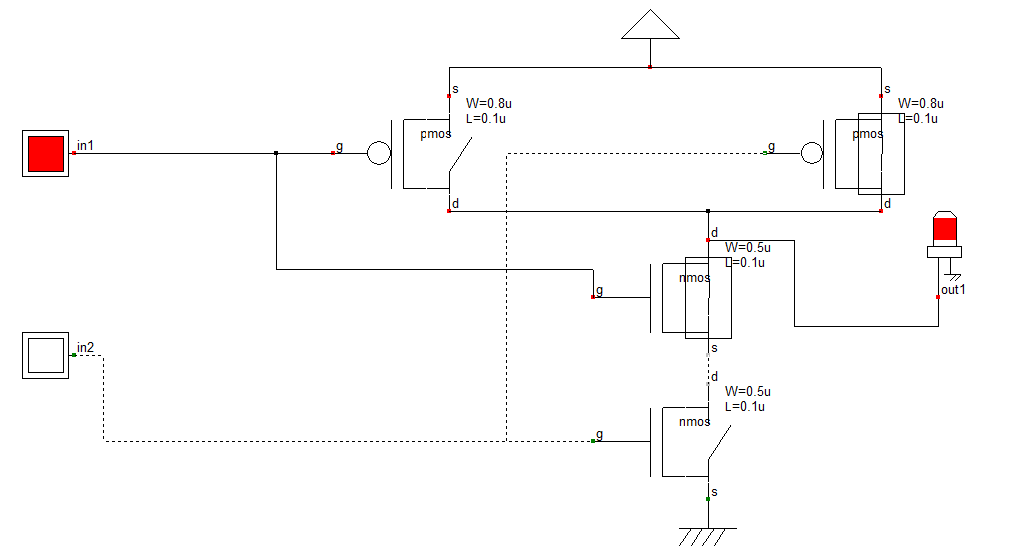


Fig 1.2

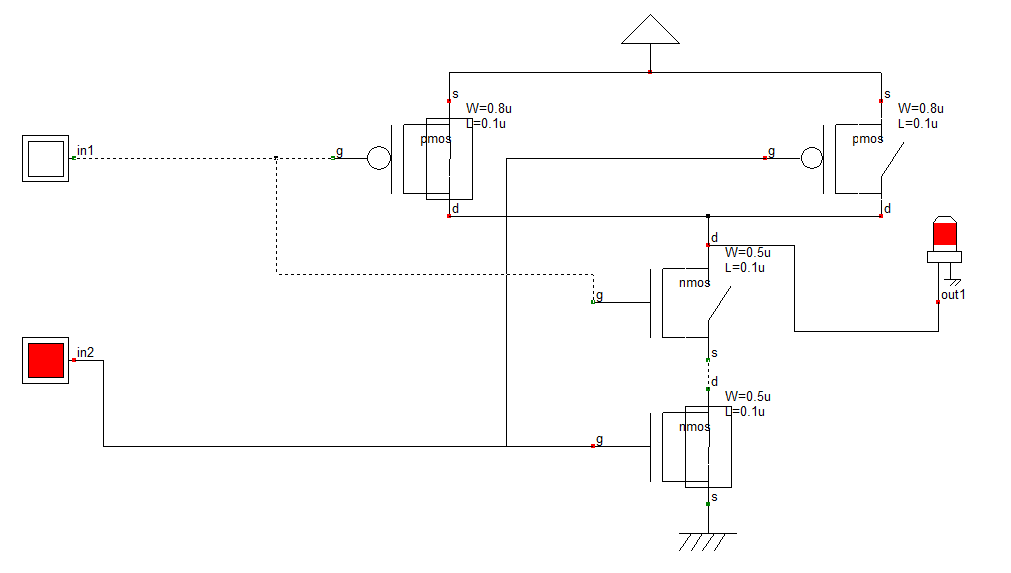


Fig 1.3

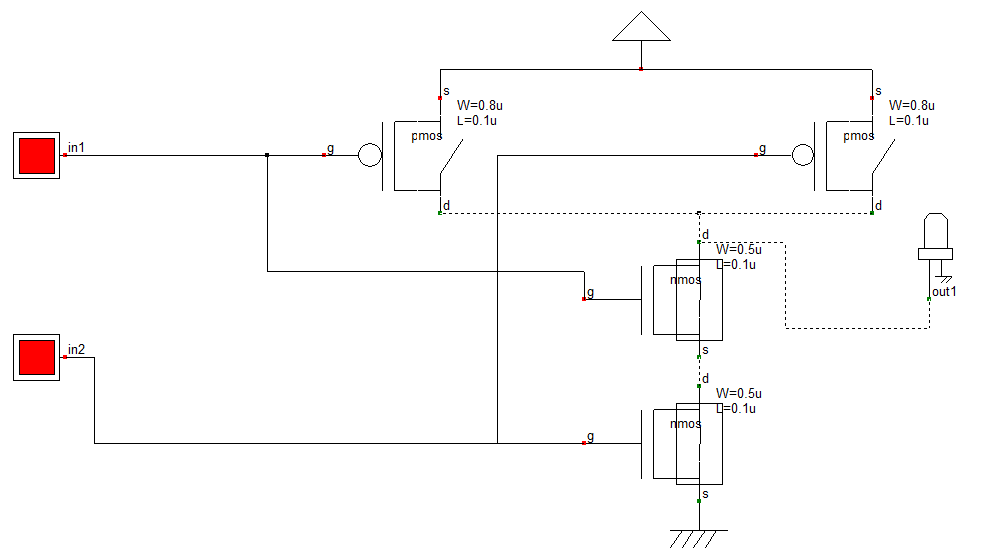


Fig 1.4

As we note in the above figures the result of NAND gate. In **Fig 1.1**, in1 =’0’, in2=’0’ then the output turned ON (out1 =’1’). In **Fig 1.2**, in1 =’1’, in2=’0’ then the output turned ON (out1 =’1’). In **Fig 1.3**, in1 =’0’, in2=’1’ then the output still turned ON (out1 =’1’). But in **Fig 1.1**, we turned ON the two inputs (in1 =’1’, in2=’1’), then the output turned OFF (out1 =’0’). And this is the work of NAND gate.

* Timing Diagram:

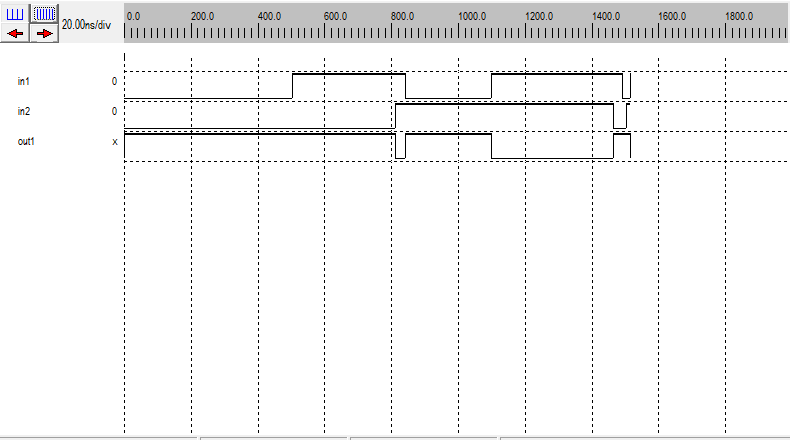
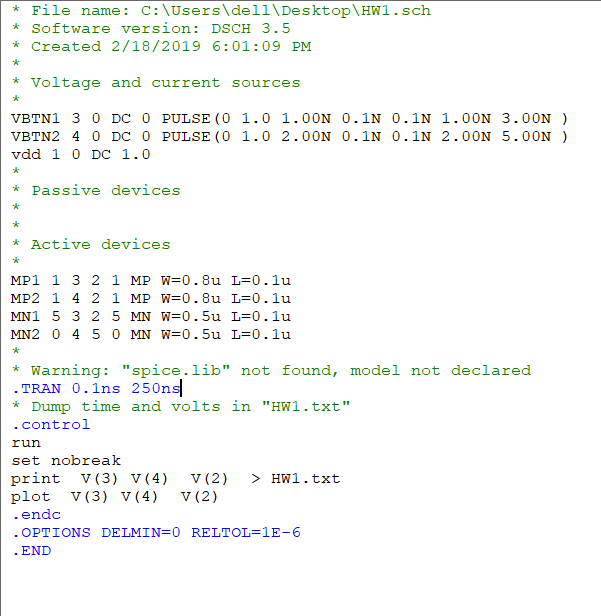


Fig 1.5

As we see in the timing diagram, the implementation of NAND gate.

* SPICE Netlist:



1. The symbol view of NAND cell:

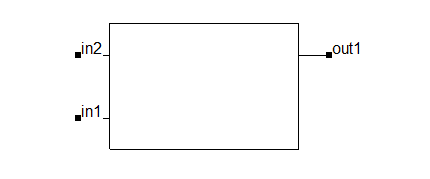


Fig 2: Cell View

1. Nand\_TB circuit with its testbench:

* Schematic:

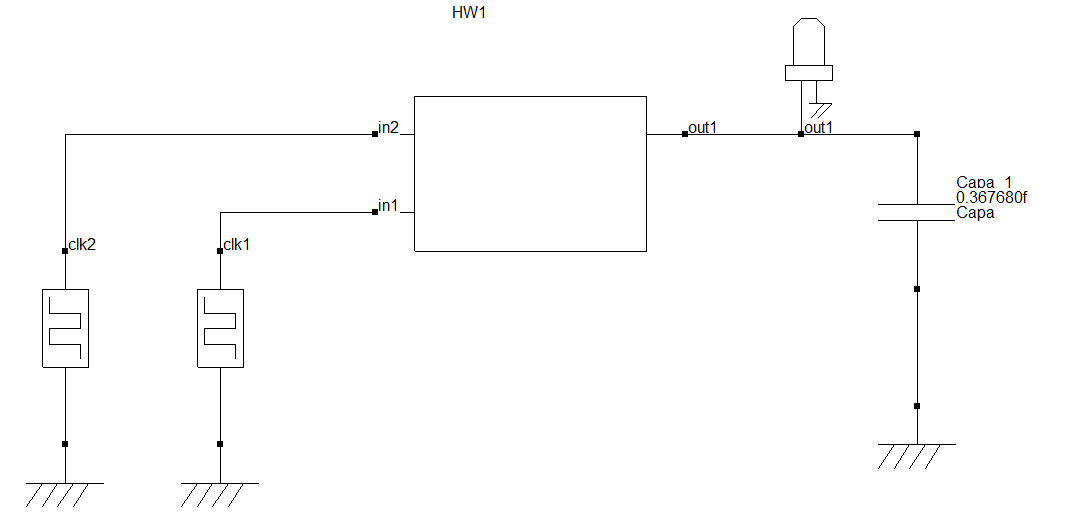


Fig 3.1

In **Fig 3.1** is the schematic of NAND gate’s block or symbol that we make it in part two using clk inputs.

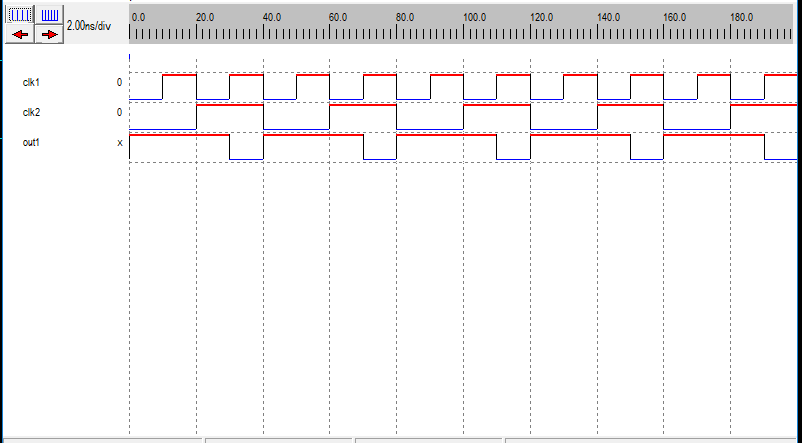
* Simulation (Timing diagram):

Fig 3.2

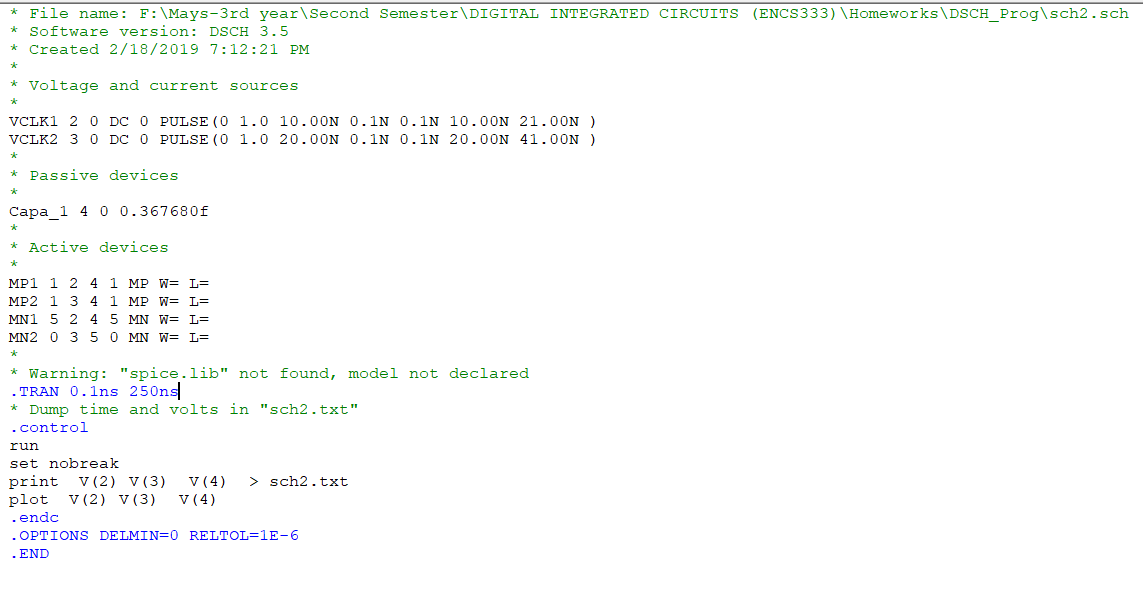
* SPICE Netlist:

Fig 3.3