➢ Lab1_Solution:

1. Design 2 input NAND gate using transistors:
   - Schematic:

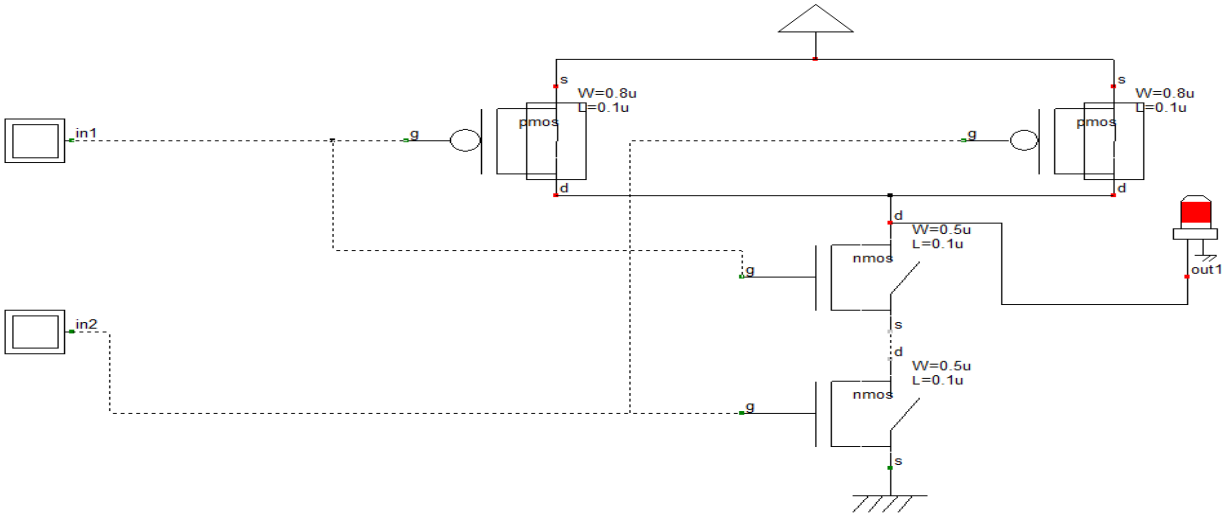

Fig 1.1

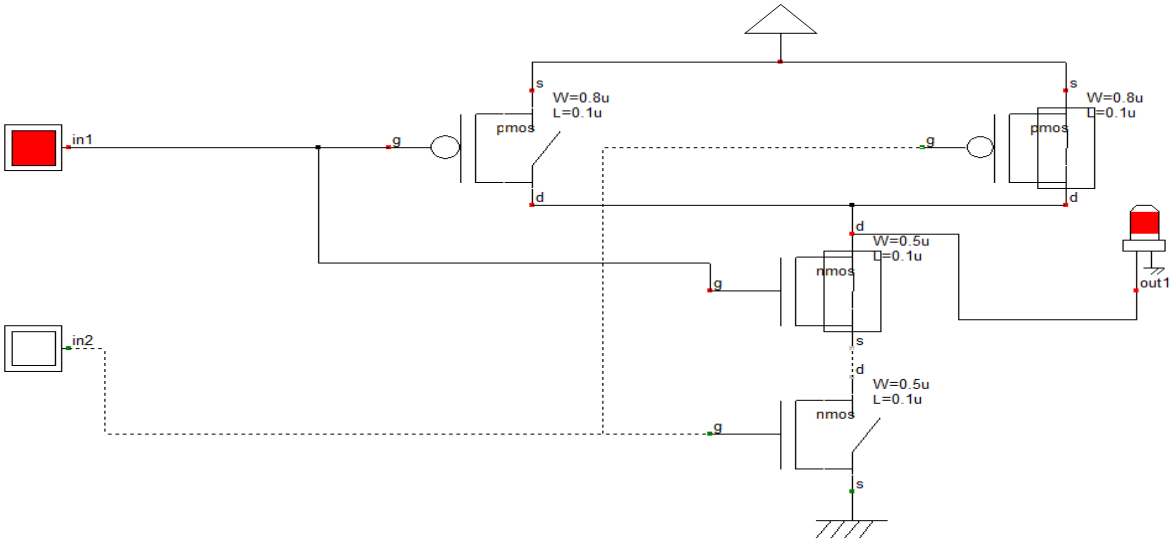

Fig 1.2

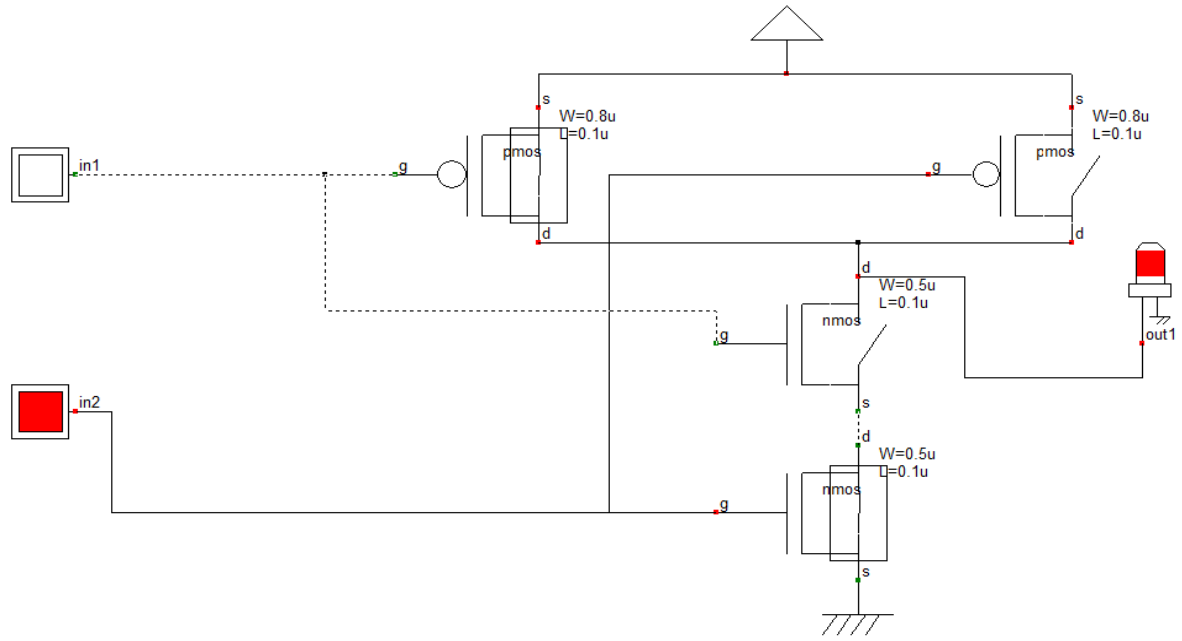
in1
in2
out1
pmos
nmos
W=0.8u
L=0.1u
W=0.5u
L=0.1u
s
g
d

Fig 1.3

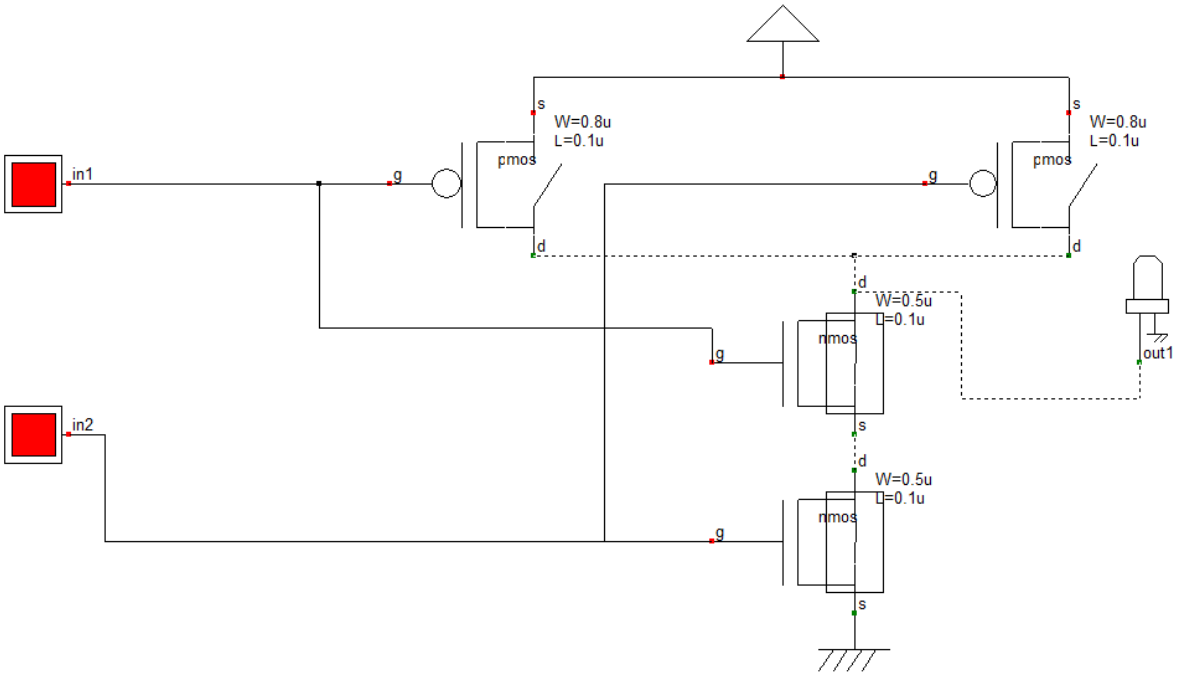
in1
in2
out1
pmos
nmos
W=0.8u
L=0.1u
W=0.5u
L=0.1u
s
g
d

Fig 1.4

As we note in the above figures the result of NAND gate. In **Fig 1.1**, in1 =’0’, in2=’0’ then the output turned ON (out1 =’1’). In **Fig 1.2**, in1 =’1’, in2=’0’ then the output turned ON (out1 =’1’). In **Fig 1.3**, in1 =’0’, in2=’1’ then the output still turned ON (out1 =’1’). But in **Fig 1.1**, we turned ON the two inputs (in1 =’1’, in2=’1’), then the output turned OFF (out1 =’0’). And this is the work of NAND gate.

- Timing Diagram:

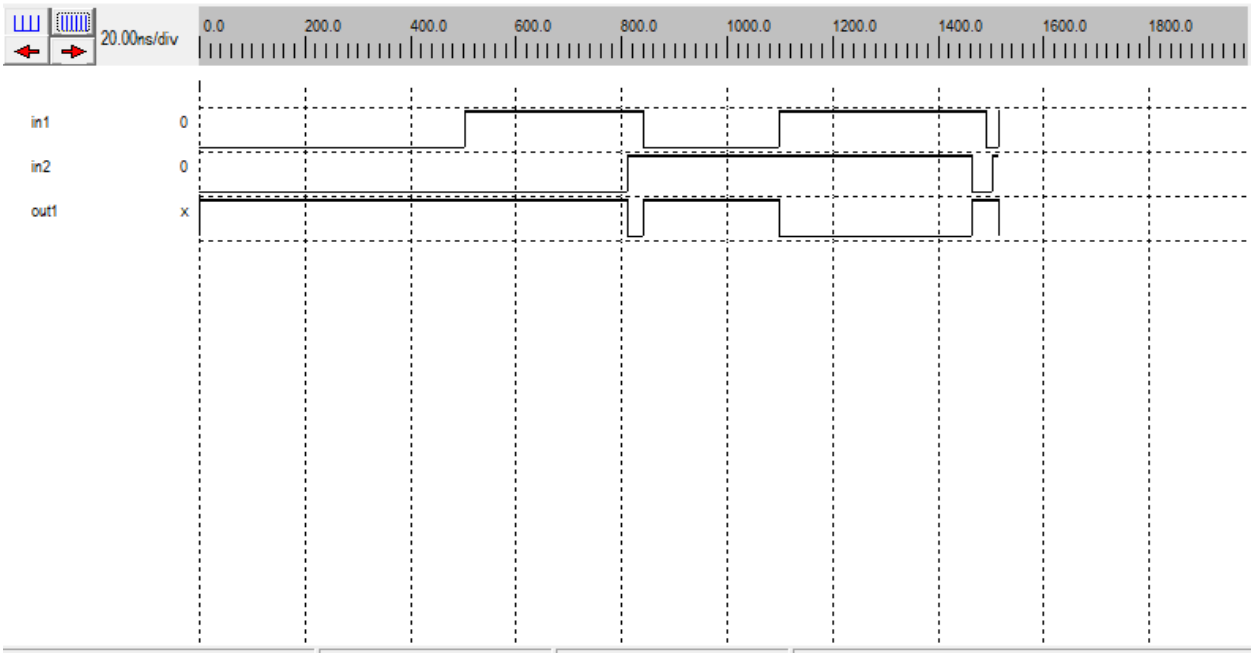

Fig 1.5

As we see in the timing diagram, the implementation of NAND gate.

- SPICE Netlist:

```
* File name: C:\Users\dell\Desktop\HW1.sch
* Software version: DSCH 3.5
* Created 2/18/2019 6:01:09 PM
*
* Voltage and current sources
*
VBTN1 3 0 DC 0 PULSE(0 1.0 1.00N 0.1N 0.1N 1.00N 3.00N )
VBTN2 4 0 DC 0 PULSE(0 1.0 2.00N 0.1N 0.1N 2.00N 5.00N )
vdd 1 0 DC 1.0
*
* Passive devices
*
*
* Active devices
*
MP1 1 3 2 1 MP W=0.8u L=0.1u
MP2 1 4 2 1 MP W=0.8u L=0.1u
MN1 5 3 2 5 MN W=0.5u L=0.1u
MN2 0 4 5 0 MN W=0.5u L=0.1u
*
* Warning: "spice.lib" not found, model not declared
.TRAN 0.1ns 250ns
* Dump time and volts in "HW1.txt"
.control
run
set nobreak
print  V(3) V(4)  V(2)  > HW1.txt
plot  V(3) V(4)  V(2)
.endc
.OPTIONS DELMIN=0 RELTOL=1E-6
.END
```

2. The symbol view of NAND cell:

Fig 2: Cell View

3. Nand_TB circuit with its testbench:
   - Schematic:

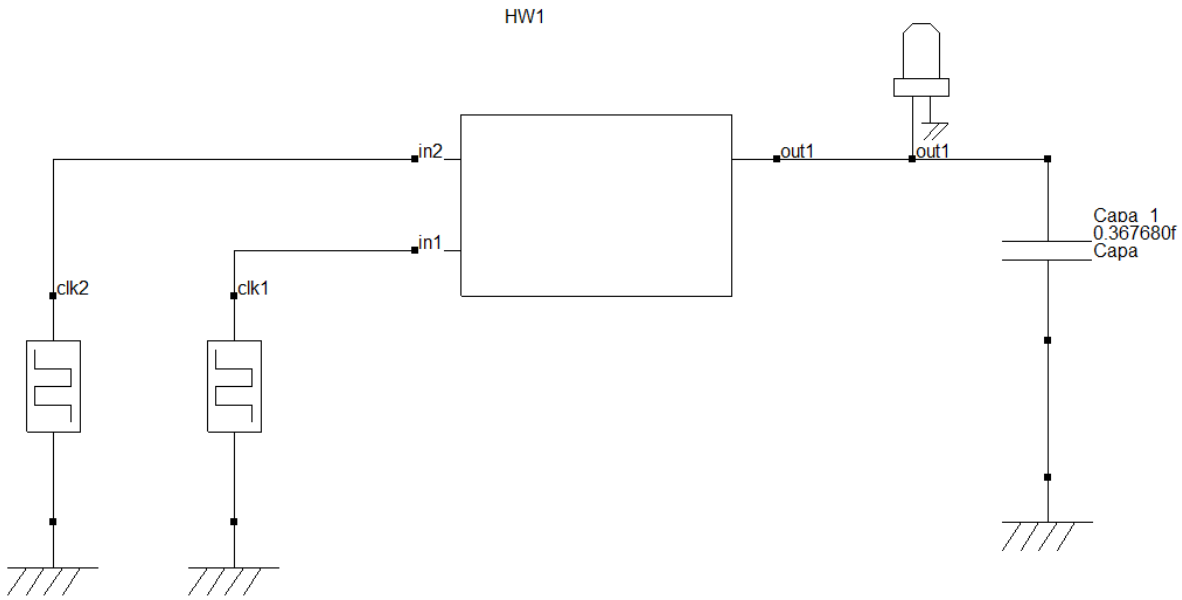

Fig 3.1

In **Fig 3.1** is the schematic of NAND gate's block or symbol that we make it in part two using clk inputs.

   - Simulation (Timing diagram):

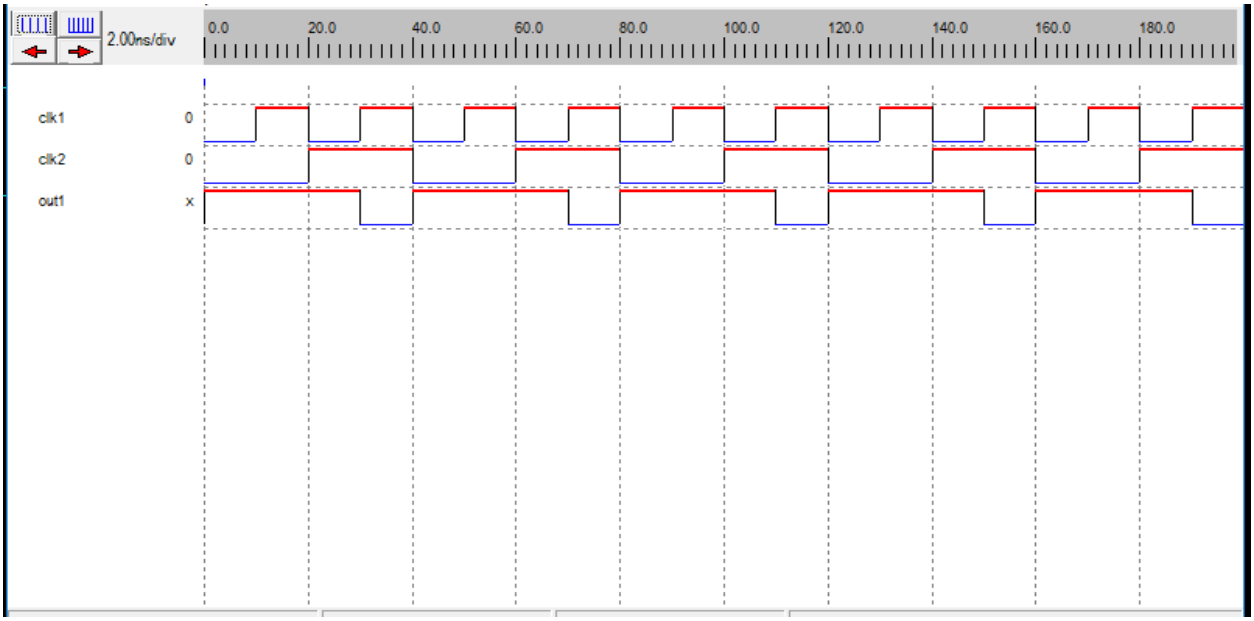

Fig 3.2

- SPICE Netlist:

```
* File name: F:\Mays-3rd year\Second Semester\DIGITAL INTEGRATED CIRCUITS (ENCS333)\Homeworks\DSCH_Prog\sch2.sch
* Software version: DSCH 3.5
* Created 2/18/2019 7:12:21 PM
*
* Voltage and current sources
*
VCLK1 2 0 DC 0 PULSE(0 1.0 10.00N 0.1N 0.1N 10.00N 21.00N )
VCLK2 3 0 DC 0 PULSE(0 1.0 20.00N 0.1N 0.1N 20.00N 41.00N )
*
* Passive devices
*
Capa_1 4 0 0.367680f
*
* Active devices
*
MP1 1 2 4 1 MP W= L=
MP2 1 3 4 1 MP W= L=
MN1 5 2 4 5 MN W= L=
MN2 0 3 5 0 MN W= L=
*
* Warning: "spice.lib" not found, model not declared
.TRAN 0.1ns 250ns
* Dump time and volts in "sch2.txt"
.control
run
set nobreak
print  V(2) V(3)  V(4)  > sch2.txt
plot  V(2) V(3)  V(4)
.endc
.OPTIONS DELMIN=0 RELTOL=1E-6
.END
```

Fig 3.3