

**Faculty of Information Technology**

**Electrical and Computer Engineering Department**

**DIGITAL INTEGRATED CIRCUITS (ENCS333)**

**Homework#2**

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**Section 2**

**Due to:19-3-2019**

**Question #1:**

**What value of Rd will drive transistor M1 just at non-saturation if Kn = 50 μA/V2, Vtn = 0.4 V, and W/L = 10?**





 ID = (50 µA) (10) (1.0−0.4)2 = 180 µA

The bias boundary condition: VGS =VDS +Vtn

Becomes: VG −VS =VD −VS +Vtn

VD =VG −Vtn

VD =1.0V−0.4V = 0.6V. Then,

Rd = $\frac{VDD-VD}{ID}$

 = $\frac{2.5-0.6}{180 µA}= $10.56 kΩ

**Question #2:**

**Calculate *ID* and *VDS* for *Vtp* = –1.0 V, *Kp* = 100 μA/ V2, and *W/L* = 4**.

Assume a saturated bias state:

 ID = (100 µA) (4) (-3.5− -1)2 = 2.5 mA.

V0 = ID (200 Ω) = (2.5 mA) (200 Ω) =0.5 V. Then,

VDS =0.5 V − 5 V = −4.5 V

The bias state check is VGS >VDS +Vtp

−3.5 > −4.5+(−1.0) = -5.5.

So, the transistor is in saturated bias state and the solutions are correct.

**Question #3:**

**Find ID and VO for Vtp = –0.6 V, Kp = 20 μA/V2, and W/L = 3**.

 Assume a saturated bias state:

ID = (20 µA) (3) (-2.2− -0.6)2 = 153.6 µA.

V0 = ID (7500 Ω) – 3 = (153.6 µA) (7500 Ω) – 3 =1.152 – 3 = -1.848V.

**Question #4:**

**Calculate ID, VDS, and verify the assumed bias state of transistor M1 for Vtp = –0.4 V, Kp = 60 μA/V2, and W/L =2**.



Assume a saturated bias state and

Since VGS is not known, we must search for another expression to supplement this equation. We can use the KVL statement

VGS = 1.2 − (VDD −(ID\*RS)) = 1.2 − 2.5 + ID\*RS = −1.3+(10 kΩ) ID

We substitute this into the saturated current expression to get

ID = (60 µA) (2) [−1.3+(10 kΩ) \*ID +0.4]2 = 120 µA [−0.9+(10 kΩ) ID ]2

This quadratic equation in ID gives solutions: ID = 35.66 µA, 227.8 µA.

The valid solution is ID = 35.66 µA, since the other solution for ID when multiplied by the sum of the two resistors gives a voltage greater than the power supply. VDS is then

VDS = ID\*(20 kΩ) −VDD = (35.56 µ A) (20 kΩ) – 2.5 = −1.789V

And

VS = VDD −ID\*RS = 2.5−(35.56 µ A) (10kΩ) = 2.144 V.

Verify the bias state

VGS =VG −VS =1.2−2.144 = −0.944 V

Transistor M1 is in saturation since

VGS >VDS +Vtp

−0.944V > −1.789V − 0.4V

**Question #5:**

**Which region of the iv curve determine delay?**

* Linear region.

**Question #6:**

**How can that match with RC?**

Voltage looks like a ramp for RC too as shown below:



**Question #7:**

**Answer the following question:**

1. **Describe the basic components of a CMOS transistor?**

NMOS and PMOS transistors work as driver transistors. when one transistor is ON, other is OFF.



1. **Draw a CMOS invertor and regions of operation.**





1. **why do VLSI chips have multiple metal layers? What are these used for? Why so many?**

Routing (interconnecting standard cells) is done over standard cells. As technology is shrinking standard cell size is decreasing and they are packed in very small area but interconnect scaling proportion to the standard cell size. So, interconnect density is increasing. It is not possible to route VLSI chips using single layer. We need multiple layer of metals to route.

1. **What is drive strength?**

Drive strength is the capacity of a cell to drive a value to the cell connected to its output. Larger the load, larger is the drive required to "force" the values at the output.

1. **Are N and P devices sizing the same? Why?**

No, because µn > µp (faster) so we make the width of PMOS larger and proportional with ratio$ \frac{µn}{µp} $ since L is fixed from DR.

1. **How do you measure wire delay? SLOPES?**

Delay: find $R=\frac{ρL}{A} and c=\frac{εA}{D}$ then time constant $τ=RC $ Slopes: from timing analysis we take 10%-90% or 20%-80% from the signal when go from low to high or from high to low and measure the slope between those points.

1. **Effect of wires dimensions on cap and resistance?**

$c=\frac{εA}{D}$ and wires are not parallel plates, but obey trends so Increasing area increases capacitance also Increasing distance decreases capacitance.

1. **Current flow in CMOS? From where to where?**

In one complete cycle of CMOS logic, current flows from VDD to the load capacitance to charge it and then flows from the charged load capacitance (CL) to ground during discharge.

1. **What is delay of logic cell? Where the delay of net comes from?**

Cell delay - Any logic cell is a combination of RC networks. A signal passing through a RC network will get delayed. Cell delay is a function of output loading and input slew rate. Net Delay- refers to the total time needed to charge or discharge all the parasitic of a given net. And this came from: The input transition time (or slew rate), the total load “seen” by the output transistors and net capacitance and “downstream” pin capacitances. These will affect how quickly the input and output transistors can “switch”.

1. **If you have wire as in the figure below, how do you calculate its resistance?**



* $R=\frac{ρL}{A}=\frac{ρ ×Lingth}{width ×Hight}$
1. **If we have 2 wires (plates as in figure below, how do you calculate the capacitance between them?**



$$c=\frac{εA}{D}=\frac{ε×Lingth×Width}{Spacing}$$