**Maher Saleem 1130258
IC HW#2**

**Sec2**

# Q1(

**Label all G,D,S , VDD, GND, Vout for the inverter below**



# Q2(



# Q3(





# Q4(

 Noise Margin: Label all voltages VOH, VOL, NMH and NML , VIL, VIH , High output, High Input, Low output, Low input in the figure below?



Q5( **The High output excursion should not be larger than the high input excursion, same for low** **excursion, What will happen if this is violated ?**

If this is violated, one of the corresponding noise margins is negative. Noise margins provide a cushion for noise immunity.

# Q6.

1. Switch Is open
Vgs = Vg – Vs =Vclk – Vout = 0
cut off region
vout = 0
2. Switch is closed
Vgs = Vclk
saturation region
Vout = Vin – Vt (since it’s NMos)

# Q7(

1. Switch Is open
Vgs = Vg – Vs =Vdd – Vout= vdd
cut off region
vout = 0
2. Switch in closed
Vgs = Vg – Vs = 0 – 0 = 0
saturation region
vout = Vin = ‘1’

# Q8)



Weak PMOS takes along of time for rise , Weak NMOS take long time for fall.

Q9 ) **List the following interconnect fabrication steps in chronological order:**

• 5)Deposit metal everywhere.
\*2)Expose photoresist using mask.
• 3)Remove all photoresist.
•1) Etch metal.
• 4)Deposit photoresist.

# Q10)



Q12.
