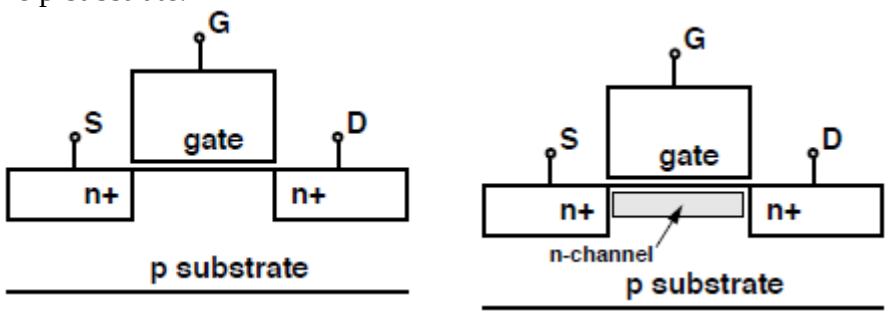
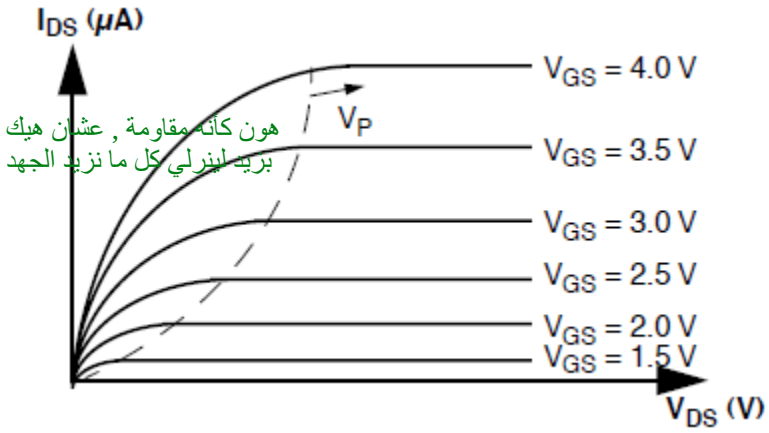
1. **How does an n-type MOSFET work? Why does the current saturate at high V_{DS}? Do not write more than two pages. Diagrams are always helpful.**

An n-type MOSFET consists of a p-substrate implanted n-type active regions. Initially when there is no bias given to any of the gate, [bulk,] drain, and source, no conduction takes place. For conduction to take place, $V_{GS} > V_{TH}$, where V_{TH} is the threshold voltage.
As you increase V_{GS} [beyond] V_{TH}, but V_{DS} is still zero, no conduction takes place, but an n-channel starts getting formed because of the positive voltage at the gate. The channel is formed due to electrons flowing in from the n+ regions1 and also due to to some minority electrons of the p-substrate.



Now, as you increase V_{DS} beyond zero, electrons start to flow from source to drain and hence conventional current flows from drain to source. We get curves like this:



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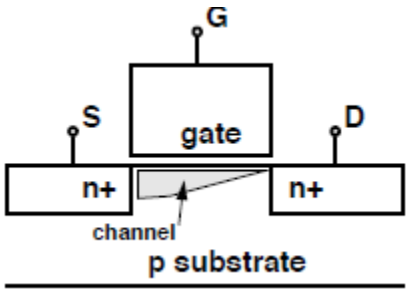
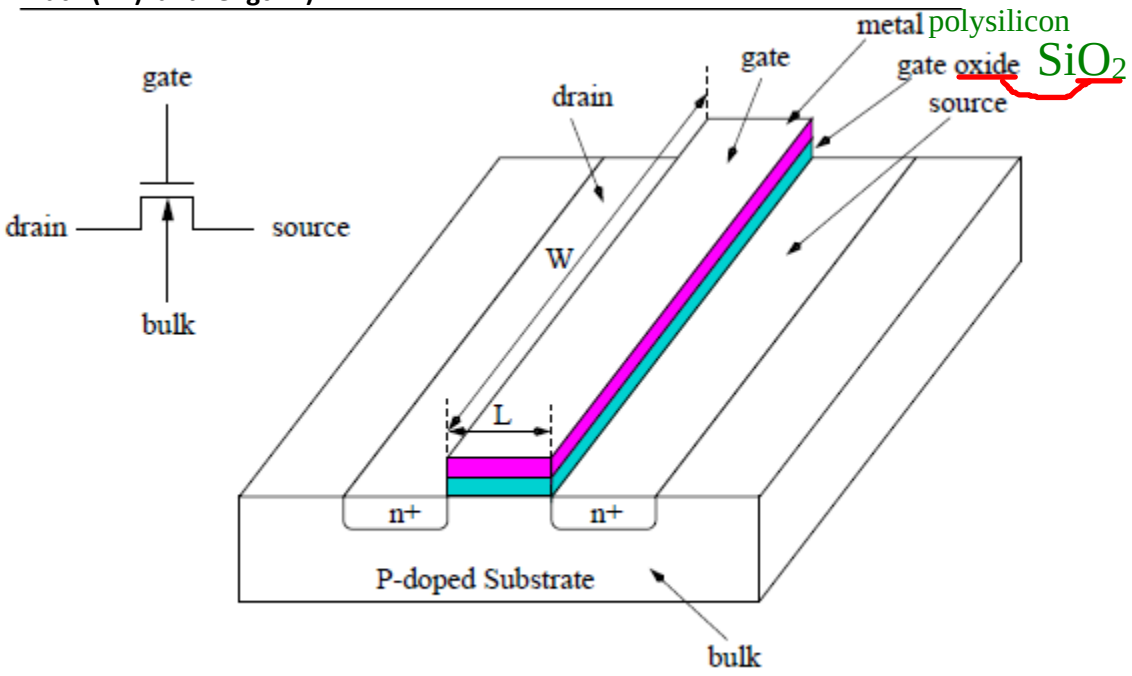
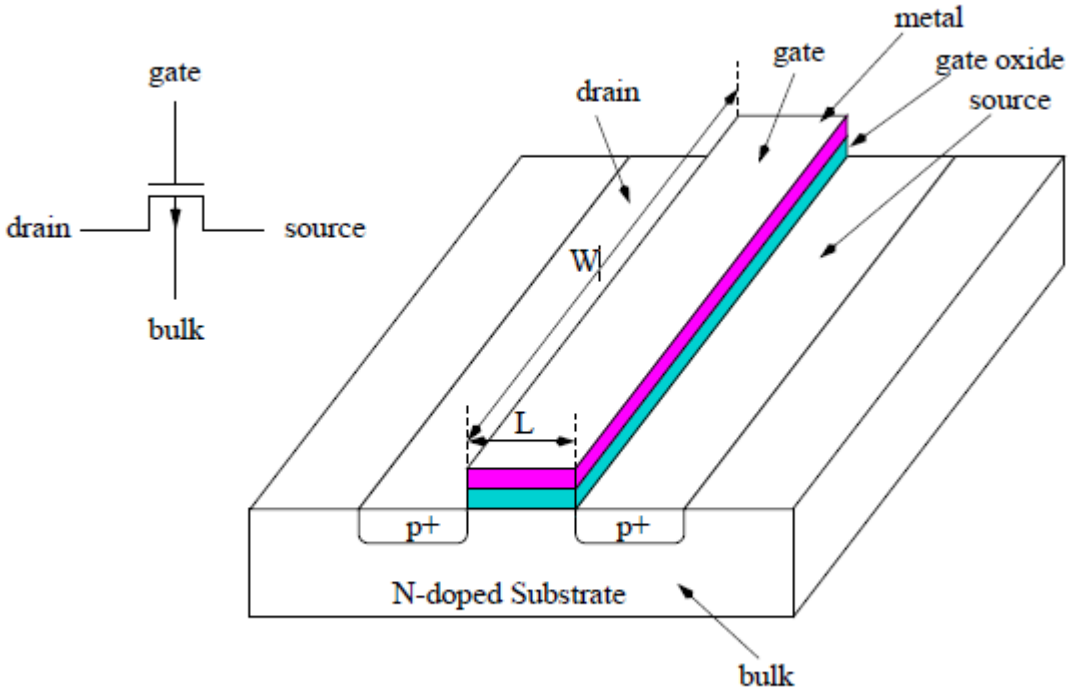
So we can observe that the current increases with increases in V_{DS}. But we can see that the current saturates after some value of V_{DS}; this value is called the pinch-off voltage. The current saturates at high V_{DB} because the junction of drain and bulk (substrate) starts getting reversebiased.
This happens also because $V_{GS} – V_{DS} < V_{TH}$.2 As the MOSFET acts like a resistor, there is a voltage drop across the channel. The farther you go from the drain, the greater the drop, and hence the lesser the reverse bias and the thicker the channel. All this happens after $V_{GS} – V_{DS} < V_{TH}$.



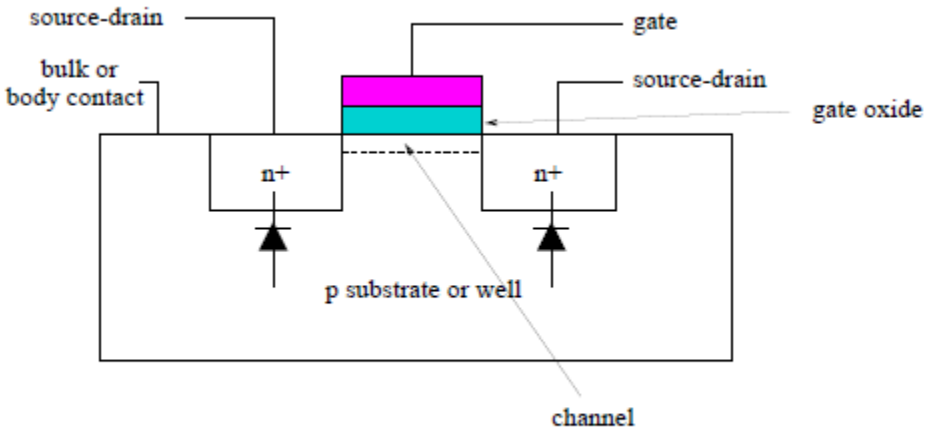
2. Draw or Name all device parts for cross section of n-type transistor as shown below (also mark width (W) and length L) :



N Transistor



P Transistor



Cross-section of NMOS transistor

3. Explain the three region of operation of the NMOS device , draw the three region of operation (I-V curve)

So, there are three regions of conduction

- **Cut-off :** $V_{gs} < V_T$
- **Linear :** $0 < V_{ds} < V_{gs} - V_T$
- **Saturation :** $0 < V_{gs} - V_T < V_{ds}$

- **Cut-off :** $I_{ds} = 0$ (for now)
  when $V_{gs} < V_T$

- **Linear :** $I_{ds} = \beta([V_{gs} - V_T]\ V_{ds} - \frac{V_{ds}^2}{2})$
  when $0 < V_{ds} < V_{gs} - V_T$

- **Saturation :** $I_{ds} = \frac{\beta}{2}(V_{gs} - V_T)^2$ (for now)
  when $0 < V_{gs} - V_T < V_{ds}$
  This is obtained by using $V_{ds} = V_{gs} - V_T$ in the equation for linear I_{ds} (see comment two pages prior to this one)

- Where $\beta = \frac{\mu\varepsilon}{t_{ox}}(\frac{W}{L})$

4. Explain how does the current depends on the process /Geometry of the device ?

Note that β depends on process dependent factors

- $\beta\ \alpha\ \mu$, the surface mobility of electrons in the channel. $\mu = \frac{avg\ \ carrier\ \ drift\ \ velocity}{Electric\ \ field} = \frac{v}{E}$. For PMOS, it is the surface mobility of holes in the channel
- $\beta\ \alpha\ \varepsilon$, the permittivity of the gate oxide $= k \cdot \varepsilon_0$, where $k \equiv$ dielectric constant and $\varepsilon_0 \equiv$ permittivity of free space

Note that β depends on geometric factors too (these are in a circuit designer's control)

- $\beta \alpha W$, the width of the device. This is usually called device "size". So we increase W for a larger drive capability
- $\beta \alpha \frac{1}{L}$, the channel length. Due to processing limitations this has a minimum (minimum process feature size). Current minimums are ~ 0.2μm
- Sometimes we intentionally choose $L > L_{min}$. A latch is a common example

5. What does Vt depends on ?
   - Gate and insulator materials, thickness of insulator, channel doping density - process dependent factors
   - V_{sb} (body effect), temperature (inversely) - operational factors