Layout Design, Analysis and Implementation of Combinational and Sequential Circuits using Microwind

Ms.Amrita Pahadia [#1], Dr. Uma Rathore Bhatt [*2]

[#1]*Student, Electronics & Instrumentation, Institute of Engg. &Technology, DAVV, Indore (India)*
[#2] *Asst.Professor, Electronics & Telecommunication Institute of Engg. &Technology, DAVV, Indore (India)*

Abstract *— To design and analyse various combinational and sequential circuits. In the present thesis we worked on 45nm and 90 nm technologies. Using afore mentioned technologies; the layout for various sequential and combinational circuits has been designed in microwind 3.5 version tool and DSCH software. We designed and analyze three combinational circuit viz. multiplexer, half adder, full adder, 4 bit barrel shifter and one sequential circuit viz. 4bit up down counter.The combinational and sequential circuits are implemented by the use of stick diagram layout designing method with microwind 3.5 version tool and DSCH software. In microwind we designed stick diagram layout and in DSCH we designed schematic diagram of all logic operation. Design of low power circuit with high speed is the essential priority of VLSI tech. For this we designed various circuits which provide optimum results. The 45 nm technology layout for basic building block (multiplexer in our case) of all the circuits has been designed in microwind 3.5 version tool and DSCH software. The simulation is also performed for 90 nm technology. Simulation results show that the proposed design for the afore mentioned circuits is greater in terms of power consumption, temperature sustainability, noise immunity and frequency as compared to existing designs.*

Keywords —*Power consumption, Temperature, Packing Density*

Introduction -The digital logic circuits are basic building blocks of the digital systems (digital computers). These digital logic circuits can be classified into two categories such as combinational logic circuits and sequential logic circuits.The logic circuits that are implemented using Boolean circuits whose output logic value depends only on the input logic values can be called as combinational logic circuits. Combinational Logic Circuits are made up from basic logic NAND, NOR, NOT gates that are "combined" or connected together to produce more complicated switching circuits. Common combinational circuits made up from individual logic gates that carry out a desired application include Multiplexers, Demtiplexers, Encoders,Decoders, Full and Half Adders etc.Any combinational circuit can be implemented with only NAND And NOR gates as these are classed as "universal" gates.The simple logic circuit whose output logic value depends on the input logic values and also on the stored information is called as sequential logic circuits.The driving force behind the manufacture of integrated circuits is miniaturization, and process technology boils down to the size of the finished transistor and other components. The smaller the transistors, the more transistors in the same area, the faster they switch, the less energy.We are using 45nm technology to design various circuits and also we are comparing the 45nm with 90nm technology.

I. METHODOLOGY

Designing of various circuits in our work with the help of microwind 3.5 version is playing key role that results in fast and optimal results in term of various parameter analysis like power consumption,delay,packing density ,output analysis etc.The MICROWIND 3 is a comprehensive solution for designing and simulating microelectronic circuits at layout level with different modules for layout designs up to 45 nm, schematic editor, mixed signal and analog simulator, memory simulator, real-time 3D display of the atomic structure of silicon and virtual fabrication process in 3-D view, verilog and SPICE support; combined in one package. Microwind is a tool for designing and simulating circuits at layout level

Another simulation tool we are using is DSCH The DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis and user friendly

II.LAYOUT DESIGN AND SIMULATION OF ALL CMOS LOGIC GATES:

A.CMOS OR gate: Logic diagram of CMOS OR gate: Fig .1 shows the design of 2 input CMOS OR gate .For any of the high input OR gate results in high output.

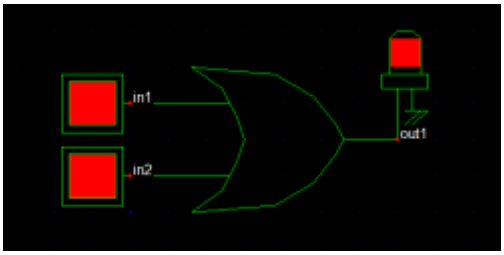

Fig 1 Logic diagram of CMOS OR gate

- Design of CMOS OR gate

Layout diagram and simulated output waveform of two input OR gate is shown in fig 1.2 respectively .This design represents the vertical red strip for gate terminal of CMOS i.e. two inputs .yellow cross red Section in pull up network is PMOS, and green cross red section for NMOS.

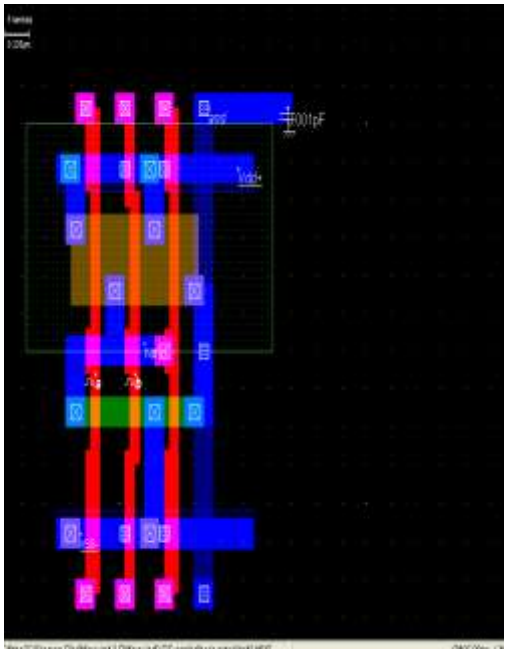

Fig 2 Layout design of CMOS OR gate

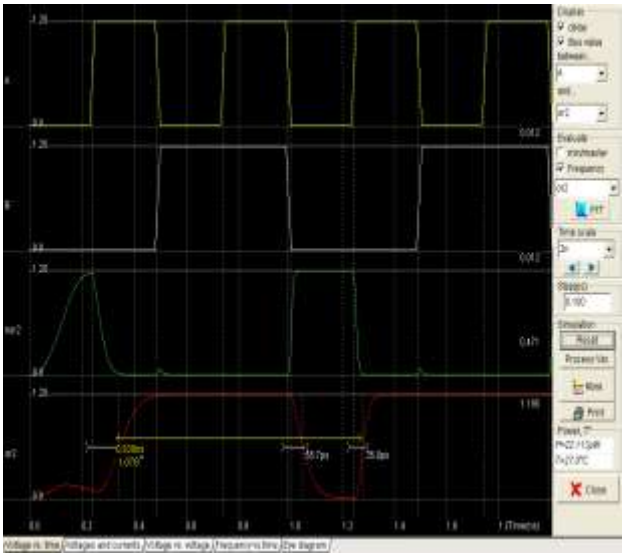

Fig 3 Output waveform of CMOS OR gate

B.CMOS AND gate:

Logic diagram of AND gate:Two input CMOS AND gate logic diagram is shown in figure 4.

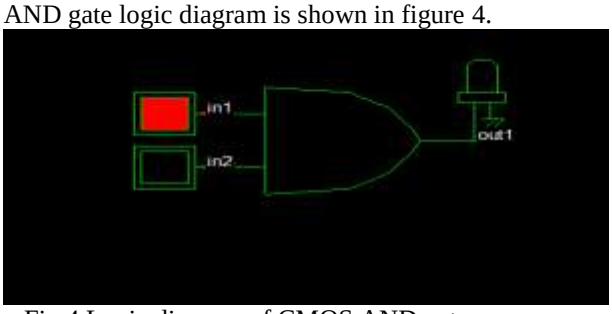

Fig 4 Logic diagram of CMOS AND gate

- Design of CMOS AND gate:

The layout design and output waveform of 2 input AND gate is obtained after designing as shown in fig.4 & 5 respectively. From the output waveform of CMOS AND gate the waveform the truth table .i.e. for any of the low input of AND gate output is low.

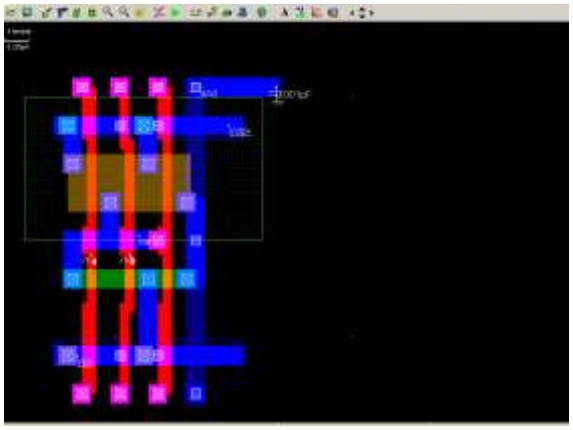

Fig 5 Layout design of CMOS AND gate

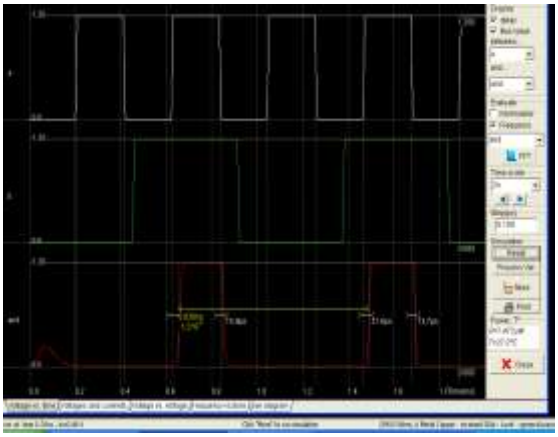

Fig.6 Output waveform of CMOS AND gate

A.LAYOUT DESIGN AND SIMULATION OF VARIOUS COMBINATIONAL CIRCUITS

I. MULTIPLEXERS

Multiplexer means many into one. A multiplexer is a circuit used to select and route any one of the several input signals to a signal output.

2:1 MUX logic diagram: The logic diagram of 2:1 mux shown below designedin DSCH tool .To select one of the input at output led helps to indicate the Condition of input.

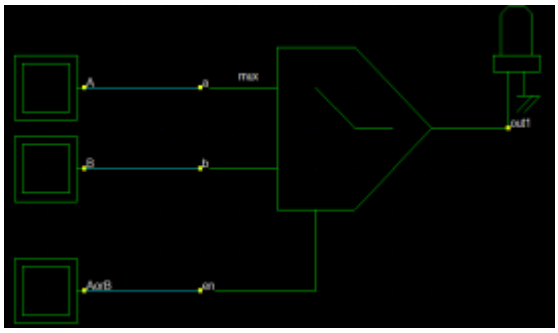

Fig. 7 Logic diagram of 2:1 MUX

Literature Review

In VLSI design conventional 2:1 multiplexers are available and all these multiplexers are designed using number of PMOS and NMOS .All these are designed in 90nm and 45nm technologies .Till now NMOS 2:1 MUX[8],CMOS 2:1 MUX,MDL 2:1 MUX,DCVSL 2:1 MUX were designed using TANNER EDA tool .The proposed design of multiplexer is MDCVSL which gives best results in term of power consumption and temperature parameters when simulated using 45nm and 90nm technology.In our work we have used DSCH and MICROWIND 3.5 version tool to design multiplexers and other combinational and sequential circuits .We have compared all these multiplexers for power consumption and temperature parameters for supply voltage at 45nm and 90nm technology node. This paper give the best 2:1 MUX for designing barrel shifter and/or rotators, which is basic building block of microprocessor CPU which can typically specify the direction of shift (left or right), the type of shift (circular, arithmetic, or logical), and amount of shift typically 1 to n-bits, but sometimes 1 to n bits [9].

II Various existing design of multiplexers

- **NMOS 2:1 multiplexer circuit**

The logic diagram of NMOS 2:1 MUX is shown in Figure. There are two select lines S, S1 and inputs are a, b. Gate terminals of NMOS are connected with select lines. This circuit is based on Complementary Pass Transistor Logic.

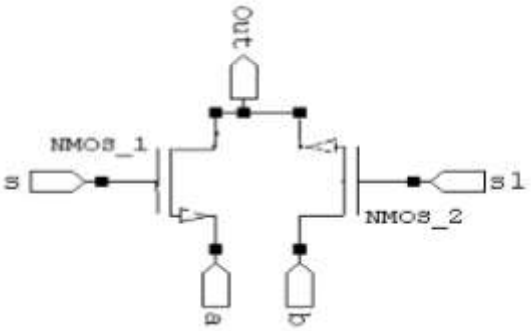

Fig 8 Logic diagram of NMOS 2:1 MUX

- **CMOS 2:1 multiplexer circuit** :

Figure shows the logic diagram of CMOS 2:1 multiplexer [4] based double pass transistor logic [7]. DPL reduce some of the inverter stages required for complementary pass transistor logic by using both N and P channel transistors

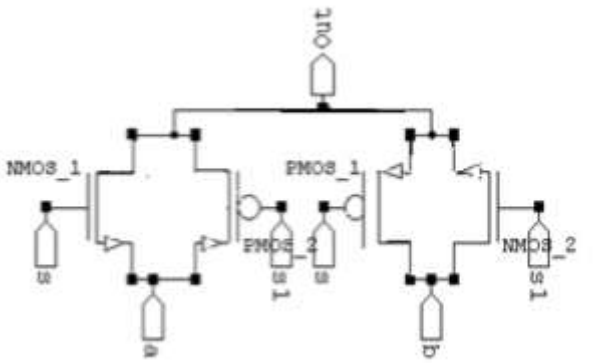

Fig 9 Logic diagram of CMOS 2:1 MUX

- **MDL 2:1 multiplexer circuit :**

The logic diagram of MDL2:1 mux circuit is shown in figure 10. MDL stands for multiplexer double with level restoration block. With addition of restoration block we can avoid swing problems and this is the main advantage of circuit.

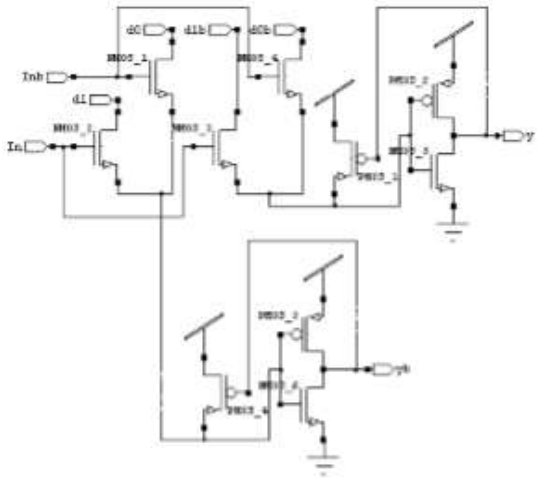

Fig 10 Logic diagram of MDL 2:1 MUX

- DCVSL 2:1multiplexer circuit

The Prior technique–of designing low power 2:1 Mux Presented is Differential Cascode Voltage Switch Logic (DCVSL) circuit. Schematic of DCVSL circuit is shown in the Figure Cascode Voltage Switch Logic (CVSL) refers to a CMOS-type logic family [4] which is designed for certain advantages.

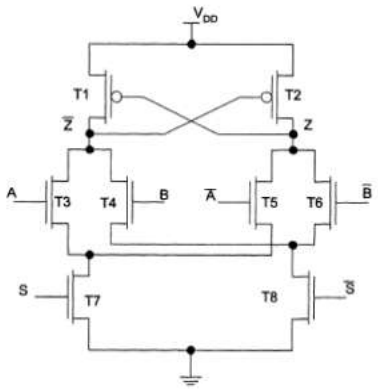

Fig 11. Logic diagram of DCVSL 2:1 MUX

A logic function and its inverse are automatically implemented in this logic style. The pull-down network implemented by the NMOS logic tree generated complementary output. The advantage of DCVSL is in its logic density that is achieved by elimination of large PFETS from each logic function.

- Layout design of DCVSL

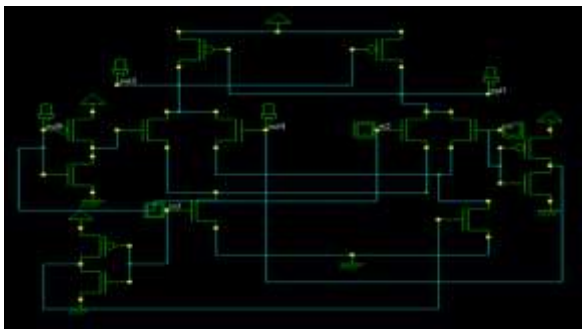

Fig.12 Layout design of Existing 2:1 Multiplexer Design (DCVSL)

PROPOSED 2:1 MULTIPLEXER DESIGN:

- MDCVSL

This multiplexer uses two logic trees and are capable of processing complex functions within a single circuit delay[8].due to the transmission gate topology in the proposed design the circuit shows optimized results in terms of threshold loss ,which further causes reduction in overall power consumption of the circuit

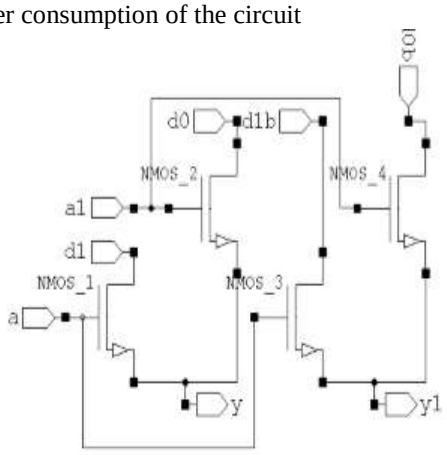

Fig 13 Logic diagram of MDCVSL 2:1 MUX

- **Layout design of MDCVSL**:

Figureshows the Layout diagram of MDCVSL 2:1 multiplexer in DSCH is designed as shown in fig. 14 .This design is obtained using CMOS i.e.combination of PMOS and NMOS . After designing the layout diagram its verilog file is generated so that after compilation of the verilog file output of 2:1 multiplexer can be verified and circuit parameters can be evaluated.

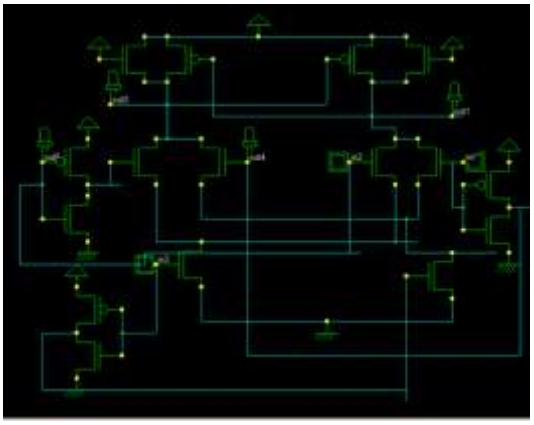

Fig 14 Logic diagram of MDCVSL 2:1 MUX using CMOS

- **Layout design of proposed 2:1 MUX:**

Fig 15 shows the layout diagram of 2:1 multiplexer obtained by making the verilog file in DSCH and the design obtained for layout by compiling the verilog file in microwind 3.5 version through this layout we can estimate the area so that desired parameter of optimal packing density can be improved.

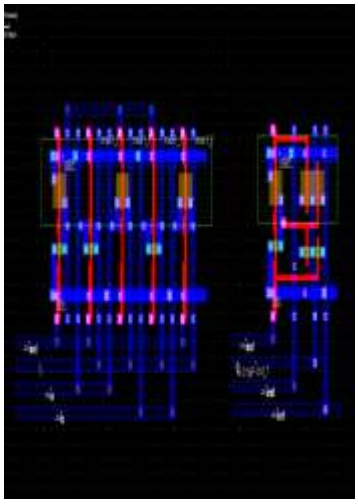

Fig 15 Layout diagram of proposed 2:1 multiplexer

Timing diagram of 2:1 MUX: The timing diagram of 2:1 Multiplexer: This timing diagram obtained after simulation in DSCH tool which evaluate the function and verify the truth table

2:1multiplexer..**240mA**

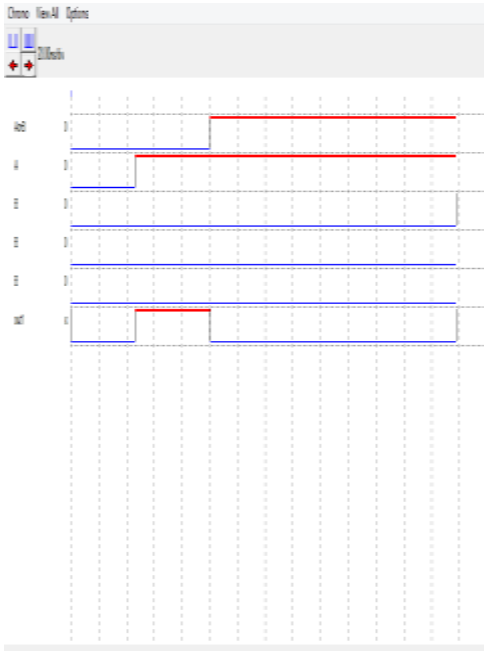

Fig. 16 Timing diagram of 2:1 MUX

3.3 RESULTS AND DISCUSSION OF VARIOUS EXISTING 2:1 MUX

We have analysed the various 2:1 multiplexer i.e. CMOS 2:1 MUX, MSL 2:1 MUX, MD 2:1 MUX, DCVSL and MDCVSL 2:1 (PROPOSED) .The design of various existing 2:1 multiplexers are compared with proposed design in terms of power consumption for different values of supply voltage shown in graph . We have mentioned all the simulated values in table for DCVSL 2:1 mux and MDCVSL 2:1 mux designed in 45nm as well as 90nm technology.

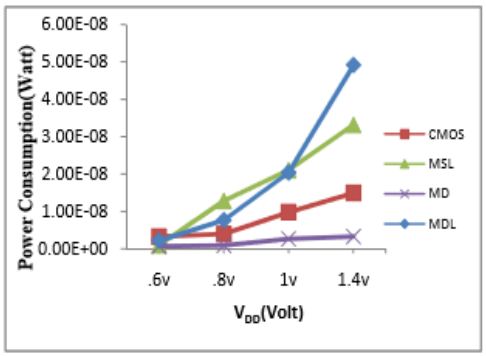

Fig 17 VDD versus power consumption analysis of different 2:1 MUX

TABLE I Analysis of power consumption

VDD (v)	Power Consumption for 90 nm of proposed design	Power Consumption for 45 nm of proposed design	Power Consumption for 90 nm of Existing design	Power Consumption for 45 nm of Existing design
0.6	15.626 µw	7.916 µw	20.427 µw	9.542 µw
0.8	33.836 µw	16.653 µw	46.004 µw	20.253 µw
1	59.422 µw	29.276 µw	82.201 µw	35.462 µw
1.2	92.763 µw	46.172 µw	0.129 mw	55.495 µw
1.4	0.134 mw	67.730 µw	0.186 mw	80.622 µw

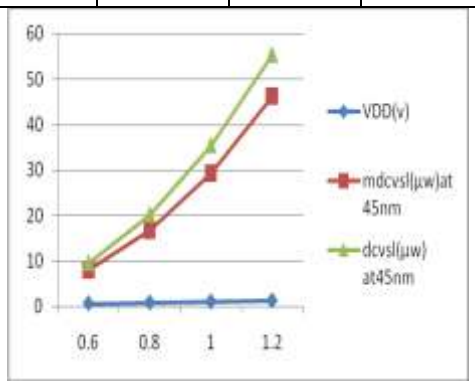

Fig.18 Shows graph between Vdd versus power consumption for 45nm technology node

After analysis we found optimal and comparable results for most required parameters that is the power consumption after comparison of existing multiplexer and proposed multiplexer designed in two technologies 90nm and 45nm technology .

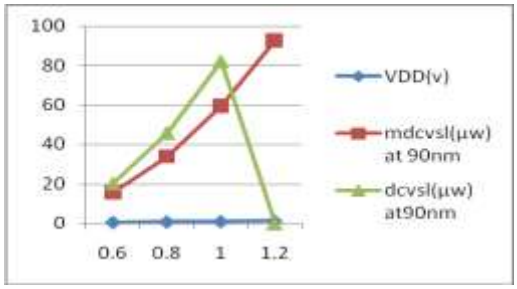

Fig.19 shows graph between Vdd versus power consumption for 90nm technology node

The result obtained for proposed design in terms of power consumption are shown as following:

TABLE II Analysis of result

Proposed mux at 45nm	Power consumption=30.0278%
Existing mux at 45nm	Power consumption=36.1026%
Proposed mux at 90nm	Power consumption=60.1298%
Existing mux at 90nm	Power consumption=82.8202%

It is clear from above table that for proposed design power consumption is very less as compared to existing design.

II.HALF ADDER: A Half Adder is a logical circuit that performs an addition operation on two binary digits. The most important feature of Half Adder is that it is only used for addition of two binary digits not more than that

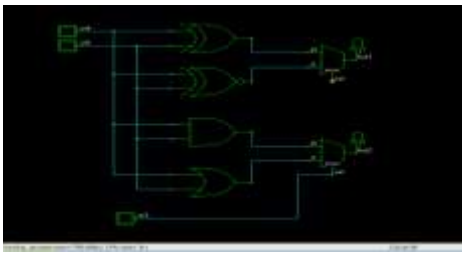

Fig .20 Logic diagram of half adder using 2:1 mux

Simulation of half adder using multiplexer in 45nm and 90nm technology node

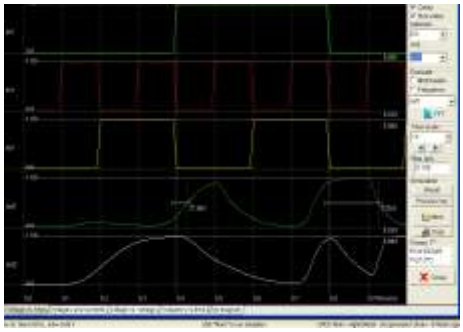

Fig.21 Ouput diagram of half adder at 45nm

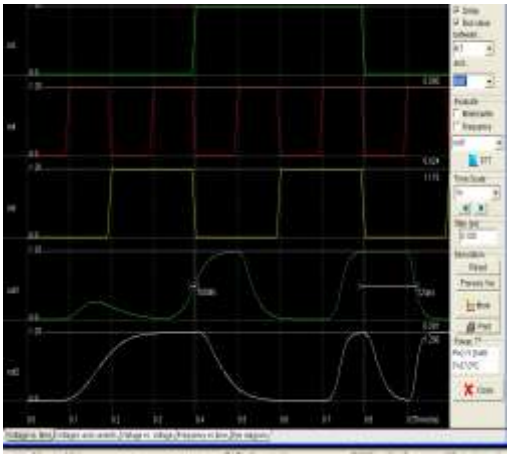

Fig 22 Ouput diagram of half adder at 90nm

RESULT OF HALF ADDER DESIGN :

The result of half adder designed using multiplexer in 45nm and 90nm technology obtained are comparable for power consumption parameters as shown by output wave-forms are as:

TECHNOLOGY NODE	POWER CONSUMPTION
AT 45nm	34.622 µw
AT 90nm	0.112 mw

III.FULL ADDER:A Full Adder is a logical circuit that performs an addition operation on three binary digits. The most important feature of Full Adder is that it can be used for addition of three binary digits not more than that.

Design of full adder:

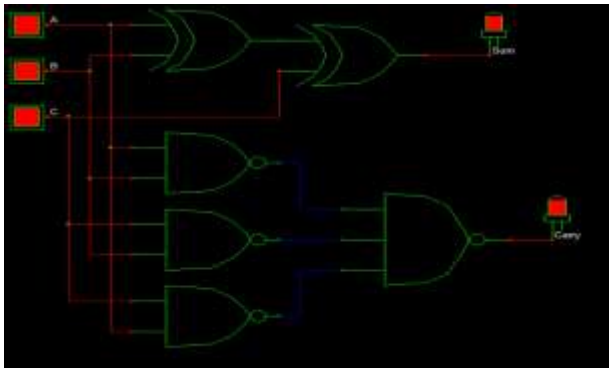

Fig 23 Schematic diagram of full adder

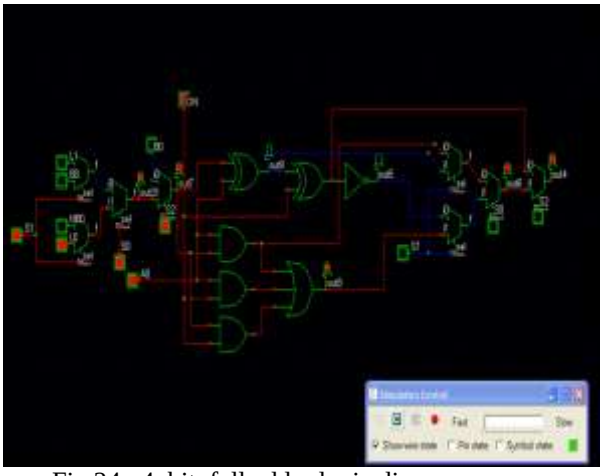

Fig 24 4 bit full adder logic diagram

Simulation of full adder using multiplexer in 45nm and 90nm technology node is shownbelow.

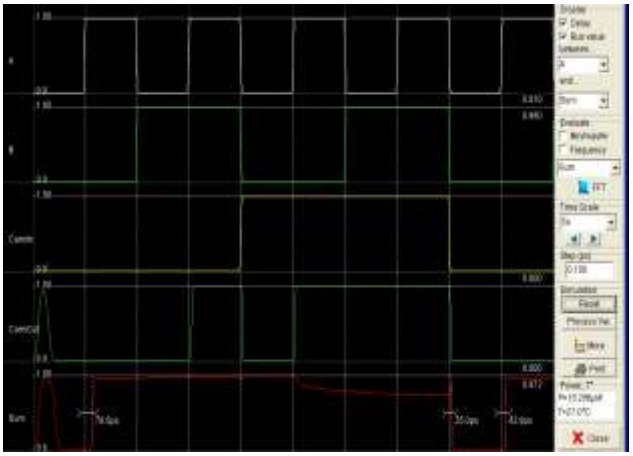

Fig 25 Output diagram of full adder at 45nm

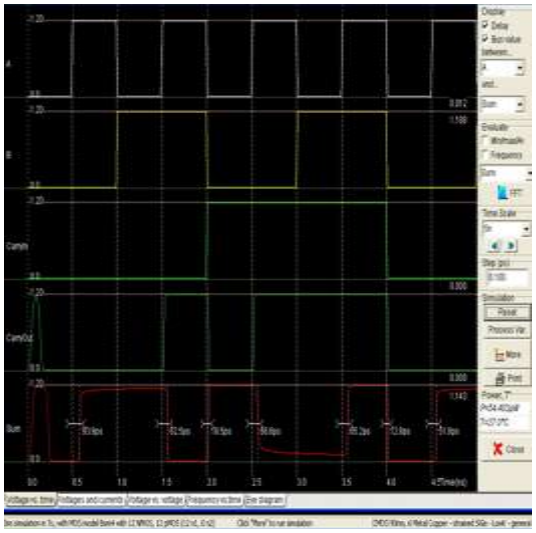

Fig 26 Output diagram of full adder at 90nm

RESULT OF FULL ADDER DESIGN

TECHNOLOGY NODE	POWER CONSUMPTION
AT 45nm	15.286 µw
AT 90nm	54.403 µw

III.DESIGN OF SEQUENTIAL CIRCUIT

Counter is a sequential circuit. A digital circuit which is used for counting pulses is known counter. Counter is the widest application of flip-flops. It is a group of flip-flops with a clock signal applied. Synchronous counter: If the "clock" pulses are applied to all the flip flop in a Counter simultaneously, then such a counter is synchronous counter [13].

EXAMPLES OF SEQUENTIAL CIRCUIT

UP DOWN COUNTER:

Up down counter is an example of synchronous counter ,i.e. it is required to give the clock pulses to each flip-flop.Updown Counter basically used for counting the bits .In our design we are using four flip-flop so we can count 16 bits i.e. from 15,14,13,12.....0.The design shown below is simulated figure in DSCH tool .The design of up-down counter can be analyzed in microwind tool after making verilog file in DSCH and compiling it in microwind. Timing diagram represents the simulation of up-down counter .i.e. 15 to 0 ,as we have four full adders to design the up-down counter so we can perform operation of 16 digits from up to down[15].The timing diagram obtained below also indicate the maximum value of current requited for the designed circuit.The maximum value of current for our design is Imax=0.520mA

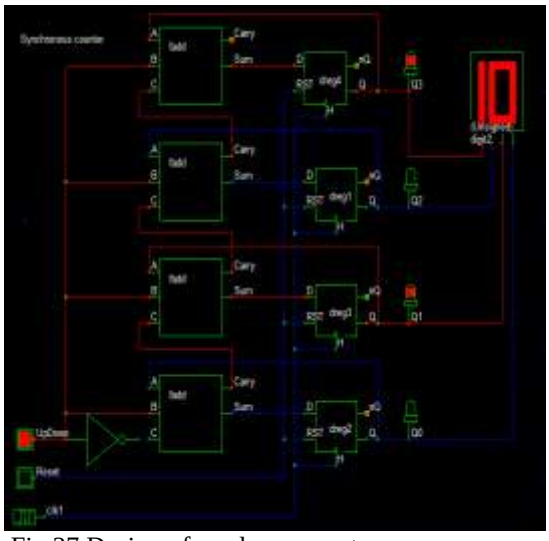

Fig 27 Design of up-down counter

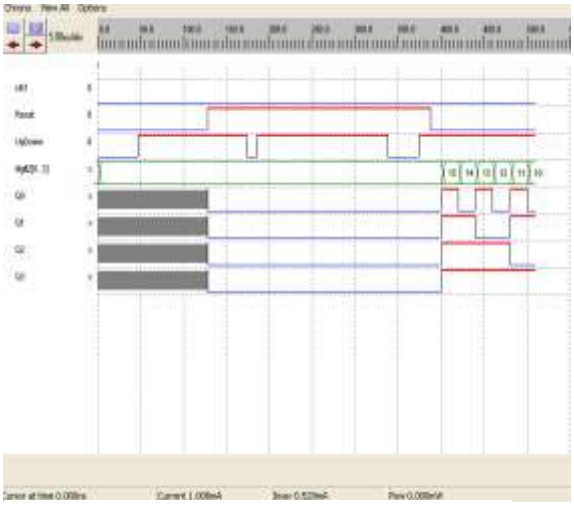

Fig 28 Timing diagram of UP –DOWN counter

5.1CONCLUSION

Power, delay and packing density are the constituent factors in VLSI design that limits the performance of any circuit. This work presents a simple approach to reduce the power consumption and increased packing density required to design circuit on chip because of the technology we have used i.e. 45nm.The post layout simulation have been done for the proposed circuit in order to show improvement in power consumption for different values of oversupply voltages and temperature. The basic logic behind using this technology is that the channel length i.e. the distance between source and drain terminal is being reduced so the device get more faster and the area required is alsoget reduced. As compare to 90nm technology the circuits designed in 45nm technology produce improved results in terms of reduced power consumption, delay and area which make it simple and efficient for VLSI hardware implementation.

5.2 FUTURE SCOPE

In this work we designed 2:1 multiplexers and using this multiplexer we implemented half adder, full adder, barrel shifter ,up-down counter .We analyze the performance metric of these circuits in terms of power consumption, delay and packing density. This work may be evaluate to optimize the other parameters like frequency, number of gate clocks, length etc.can be further extended for higher number of bits to evaluate for parameters like area, delay and power .steps may be taken to optimize the other parameters like frequency, number of gate clocks, length etc.By the proposed MDCVSL multiplexer improved version of integrated circuits may be designed.

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