Faculty of Engineering & Technology Electrical & Computer Engineering Department

INTEGRATED CIRCUIT - ENCS 3330

IC HW1

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Section: 2

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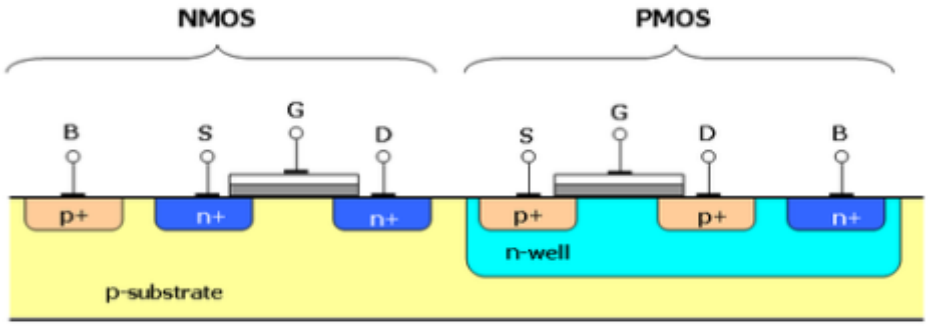
Q1: Define CMOS?

Answer: The technology used to build integrated circuits is known as CMOS, which stands for "Complementary Metal-Oxide Semiconductor." Many digital logic and analog circuits use CMOS technology.

Q2: What are the two types of transistor? How do they work, show operation region of each device?

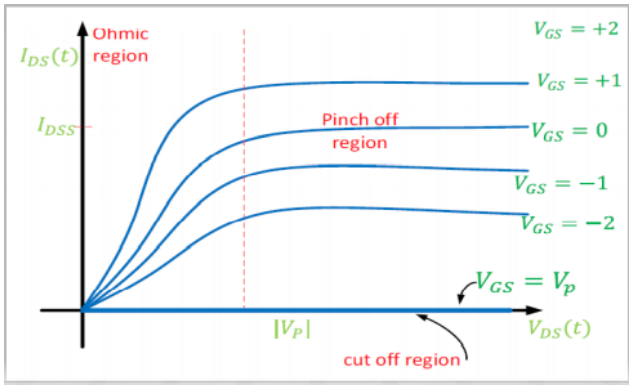
Answer: There are two kinds of semiconductors in CMOS: p-type and N-type. Because CMOS semiconductors contain both NMOS and PMOS circuits, they contain two kinds of semiconductors. Based on how the circuit is constructed, these two semiconductors work together to form logic gates.



And now we want to put the difference between NMOS, PMOS:

NMOS:

NMOS is laid on a p-type substrate and the majority of electrons are carried It is therefore faster than PMOS, but it is not immune to NOISE like PMOS.



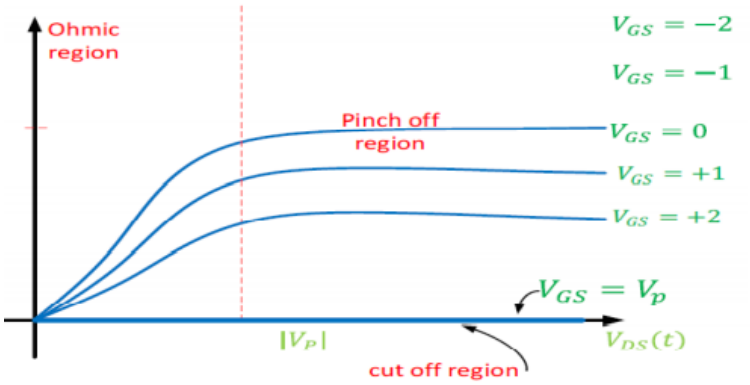
When Vgs < Vt , NMOS OFF

When Vds < Vgs -Vt , NMOS LINEAR

When Vds > Vgs – Vt , NMOS SATURATION

PMOS:

However, PMOS is laid on an N-type substrate, the majority of PMOS carriers are holes, and NMOS is faster than PMOS but not immune to NOISE.



When Vsg < |Vt|, PMOS OFF

When Vsd < Vsg – |Vt| , PMOS LINEAR

When Vsd > Vsg – |Vt|, PMOS SATURATION

While PMOS has the same Working Region as NMOS, but with a negative VGS.

Q3: What are the main IC parasitic?

Answer:

1- Diodes.
2- Resistors.
3- Inductors.
4- Capacitors.
5- Transistors (Bipolar).

Q4: Explain What do we mean by process node? And how does that affect IC characteristics?

Answer: The process technology node refers to a specific semiconductor manufacturing process. In addition to, different circuit generations and architectures are often associated with different nodes. The smaller the technology node, the smaller the feature size, resulting in smaller transistors that are faster and more energy efficient. The term "process node" used to refer to a number of distinct characteristics of a transistor, including the gate length and M1 half-pitch.

Q5: What are the basic steps for CMOS IC fabrication?

Answer:

1- **Step1: Substrate:** Primarily, start the process with a P-substrate.
2- **Step2: Oxidation:** The oxidation process is done by using high-purity oxygen and hydrogen, which are exposed in an oxidation furnace approximately at 1000 degree centigrade.
3- **Step3: Photoresist:** A light-sensitive polymer that softens whenever exposed to light is called as Photoresist layer. It is formed.
4- **Step4: Masking:** The photoresist is exposed to UV rays through the N-well mask
5- **Step5: Photoresist removal:** A part of the photoresist layer is removed by treating the wafer with the basic or acidic solution.
6- **Step6: Removal of SiO2 using acid etching:** The SiO2 oxidation layer is removed through the open area made by the removal of photoresist using hydrofluoric acid.
7- **Step7: Removal of photoresist:** The entire photoresist layer is stripped off
8- **Step8: Formation of the N-well:** By using ion implantation or diffusion process N-well is formed.
9- **Step9: Removal of SiO2:** Using the hydrofluoric acid, the remaining SiO2 is removed.
10- **Step10: Deposition of polysilicon:** Chemical Vapor Deposition (CVD) process is used to deposit a very thin layer of gate oxide.
11- **Step11: Removing the layer barring a small area for the Gates:** Except the two small regions required for forming the Gates of NMOS and PMOS, the remaining layer is stripped off.

12- **Step12: Oxidation process:** Next, an oxidation layer is formed on this layer with two small regions for the formation of the gate terminals of NMOS and PMOS.
13- **Step13: Masking and N-diffusion:** By using the masking process small gaps are made for the purpose of N-diffusion.
14- **Step14: Oxide stripping**
15- **Step15: P-diffusion:** Similar to the above N-diffusion process, the P-diffusion regions are diffused to form the terminals of the PMOS.
16- **Step16: Thick field oxide:** A thick-field oxide is formed in all regions except the terminals of the PMOS and NMOS.
17- **Step17: Metallization:** Aluminum is sputtered on the whole wafer.
18- **Step18: Removal of excess metal:** The excess metal is removed from the wafer layer.
19- **Step19: Terminals:** The terminals of the PMOS and NMOS are made from respective gaps.
20- **Step20: Assigning the names of the terminals of the NMOS and PMOS.**