Faculty of Engineering & Technology Electrical & Computer Engineering Department

INTEGRATED CIRCUIT - ENCS 3330

IC HW2

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Section: 2

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Q1: Explain all Levels of IC Design?

Digital Standard Cells: Basic cells that execute specific functions (e.g., AND, OR, etc.) or more complicated functions (e.g., Multiplexers, Latches, Flip-Flops, etc.) and are used as building blocks for broad digital circuits. Intellectual Property (IP) Blocks: Large blocks used in large designs that execute finished functions (DAC, ADC, PLL, etc.). I/O (Input/Output) Cells :Implement the connection between the IC's internal circuitry and the external world (PCB). Digital ICs: Large integrated circuits (e.g., processors, GPUs, etc.) that are delivered to end users.

Q2: What do we mean by technology file, technology scaling and how does that affect functionality, cost and power of the design?

The deliberate injection of impurities into an intrinsic semiconductor with the aim of modulating its electrical, optical, and structural properties is known as doping the semiconductor.

N-type semiconductors are created by doping an intrinsic semiconductor with an electron donor element during manufacture. The term n-type comes from the negative charge of the electron. In n-type semiconductors, electrons are the majority carriers and holes are the minority carriers.

P-type semiconductors are created by doping an intrinsic semiconductor with an electron acceptor element during manufacture. The term p-type refers to the positive charge of a hole. As opposed to n-type semiconductors, p-type semiconductors have a larger hole concentration than electron concentration. In p-type semiconductors, holes are the majority carriers and electrons are the minority carriers.

Q3: Draw the cross section physical view of the MOS transistor and then Derive the current equation for PMOS and NMOS in all region of operation?

If a positive voltage is applied to the gate in NMOS, holes on the p-type substrate's surface would be repelled by the electric field produced by the voltage. At first, the holes would actually be repelled, leaving only immobile (negative) atoms of the acceptor form on the surface, resulting in a depletion area on the surface.

For PMOS, if a negative voltage is applied at the gate, electrons which are at the surface of the n-type substrate will be repelled by the electric field generated by the voltage applied. At first, the electrons will simply be repelled and what will remain on the surface will be immobile (positive) atoms of the acceptor type, which creates a depletion region on the surface.

The capacitance of the gate and substrate will increase in this process.

Q4: What is the difference between Wafer, Die and Package?

The stages or steps involved in designing an IC begin with Device Definition and Feature Analysis, followed by Architectural or System Level Design. Then we must design the system's logic and build the modules. Moving on to the gate stage, where the logic can be implemented using gates. After that, transistors are used to implement the gates themselves.. Finally, we move on to work on the device level, which is each transistor in the circuit.

Q5: IC Component Types?

The CMOS process requires large number of steps. The first step is to obtain the base material for manufacturing process, which is wafer, it is obtained by cutting a single crystal ingot into thin slices. In each processing step, a certain area of the chip needs to be masked out using the appropriate mask, to accomplish the mask we need to apply photolithography technique through the manufacturing process. The photolithography process requires some steps, Oxidation layering is optional step and used to form an insulation layer and also forms the transistor gates. Photoresist coating is applied after that, it is a light sensitive material applied evenly on the wafer, and when exposed to light it will make the affected regions insoluble (or the opposite if a positive photoresist is used). Stepper exposure, a glass mask (or reticle), containing the patterns that we want to transfer to the silicon , is brought in close proximity to the wafer. Photoresist development and bake, Once the exposed photoresist is removed, the wafer is “soft-baked” at a low temperature to harden the remaining photoresist. Acid Etching, material is selectively removed from areas of the wafer that are not covered by photoresist. After that we will use a special tool (SRD) to clean the wafer and then dry it using nitrogen.

After that, Diffusion or Ion Implantation is applied, this process is important to create the source and drain regions, well and substrate contacts, the doping of polysilicon, and the adjustment of the device threshold. The Ion Implantation is widely used because it allows an independent control of depth and dosage. Any CMOS process requires the repetitive deposition of layers of a material over the complete wafer, and this can be done using various techniques according to the material. Once a material has been deposited, etching is used to selectively form patterns such as wires and contact holes. Either the wet etching process or the dry (or plasma) etching can be used. Finally, in modern CMOS processes, multiple patterned metal interconnect layers are superimposed onto each other.

Q6: What do we mean by Doping the Semiconductor? What is the difference between Ntype and Ptype materials?

Doping the semiconductor is the intentional introduction of impurities into an intrinsic semiconductor for the purpose of modulating its electrical, optical and structural properties.

When a small amount of pentavalent impurity is added to a pure semiconductor, it produces an extrinsic semiconductor with a significant number of free electrons, and is known as an N-type semiconductor.

P-type semiconductors are formed when a small amount of a trivalent impurity is added to a pure semiconductor, resulting in a large number of holes. The addition of trivalent impurities such as Gallium and Indium to the semiconductor material results in a significant number of holes.

Q7: Explain how do we generate a depletion layer and how does that affect the capacitance?

For NMOS, if a positive voltage (< V_{TH}) is applied at the gate, holes which are at the surface of the p-type substrate will be repelled by the electric field generated by the voltage applied. At first, the holes will simply be repelled and what will remain on the surface will be immobile (negative) atoms, which creates a depletion region on the surface.

When a negative voltage is applied to the gate of a PMOS device, electrons on the n-type substrate's surface are repelled by the electric field generated by the voltage. At first, the electrons would simply be repelled, leaving only immobile (positive) ions on the surface, resulting in a depletion area on the surface.

The capacitance for the both PMOS and NMOS will be reduced in when a depletion layer is created because the distance between charges has increased.

Q8: Define threshold voltage and what are the main factors that affect threshold voltage of the device?

For NMOS: Threshold voltage is the V_{GS} that below it the transistor's current (I_{DS}) effectively drops to zero.

For PMOS: Threshold voltage is the V_{GS} that above it the transistor's current (I_{DS}) effectively drops to zero.

Threshold voltage is affected in this way:

Negative bulk bias and or positive source bias ==> source-bulk diode in

reverse bias ==> larger Vt

The 'bulk charge' term in the Vt equation changes with the

reverse bulk-source bias

following equation represents the body effect:

$$Vt = Vto + \gamma\left[\sqrt{|2\phi f| + |Vsb|} - \sqrt{|2\phi f|}\right]$$

where $\gamma = \frac{1}{Cox}\sqrt{2q\varepsilon N_B}$ **(γ ~ 0.3-1.4 $V^{0.5}$)**

A higher Vt leads to lower device currents (i.e. slower circuits).

• Transistor matching is also degraded by the 'body effect'

• Low Vt devices can be obtained by forward body bias (0.3-0.5 Vcc)

• Note: transistors in stack have "body effect" since Vs > Vbulk.

Also the temperature affects the threshold voltage according to the following equation:

Vt(T):

$$V_T = V_{T0} + \alpha(T - T_0)$$

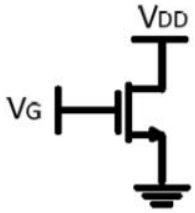
When T increases, Vt also increases.

Vt dependency means that low an high Vt scale differently with temperature Shutting down units (power saving) introduce dynamic thermal variation.

Q9: In each region of operation, how do we treat or model the MOS transistor?

We can use the following equations to model or treat an NMOS device, the voltage we need to apply is shown beside each region of operation:

Region of operation	Characteristic equation	V_{GS}	V_{DS}
Cut-off	$I_{DS}=0$	$<V_{TH}$	-
Linear or triode	$I_{DS} = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)$	$>V_{TH}$	$<V_{GS}- V_{TH}$
Saturation	$I_{DS} = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \cdot (1 + \lambda \cdot V_{DS})$	$>V_{TH}$	$>V_{GS}- V_{TH}$



In the same way we can treat a PMOS device according to the following equations:

Region of operation	Characteristic equation	$\lvert V_{GS}\rvert$	$\lvert V_{DS}\rvert$
Cut-off	$\lvert I_{DS}\rvert=0$	$<\lvert V_{TH}\rvert$	-
Linear or triode	$\lvert I_{DS}\rvert = \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(\lvert V_{GS}\rvert - \lvert V_{TH}\rvert - \frac{\lvert V_{DS}\rvert}{2}\right) \cdot \lvert V_{DS}\rvert$	$>\lvert V_{TH}\rvert$	$<\lvert V_{GS}\rvert- \lvert V_{TH}\rvert$
Saturation	$\lvert I_{DS}\rvert = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot (\lvert V_{GS}\rvert - \lvert V_{TH}\rvert)^2 \cdot (1 + \lambda \cdot \lvert V_{DS}\rvert)$	$>\lvert V_{TH}\rvert$	$>\lvert V_{GS}\rvert- \lvert V_{TH}\rvert$

Q10: Define leakage current in MOS transistor and explain the main factors that affect threshold voltage of the device?

Leakage current or sub-threshold current is the current that shows when we reduce gate voltage to Vt or less, the current does not abruptly drop to zero. Around Vt the current drops off in an exponential manner with a slope of ~1decade/100mV.

Leakage current can be approximated as: Ids ~ Io*exp[q(Vgs-Vt)/nkT]

Q11: Explain the Main factors that affect reliability of chip/device?

1. Hot-e degradation: When a MOS transistor is in saturation, the electric field across the pinch-off region may be high enough that carriers gain there enough energy to excite electron-hole pairs. The holes (electrons) usually flow towards the p-substrate (n-well) in an n-ch (p-ch) device, increasing the substrate currents (bad for latch-up!). the reliability concern is that part of the hot-e can penetrate the gate oxide.
2. Vt Stability: The ac performance of a transistor may be affected after applying a dc voltage to the transistor's gate for a long time. This effect is called 'Vt stability'. It is primarily caused by the charging/discharging of slow interface states and by mobile ions drift in the oxide.
3. Gate Stress: Every process has a maximum allowed voltage stress on the transistors, The thin gate oxide has a certain density of defects that may ruin the transistor if a high voltage is applied to the gate.

Q12: What do we mean by Hot-e degradation for MOS device?

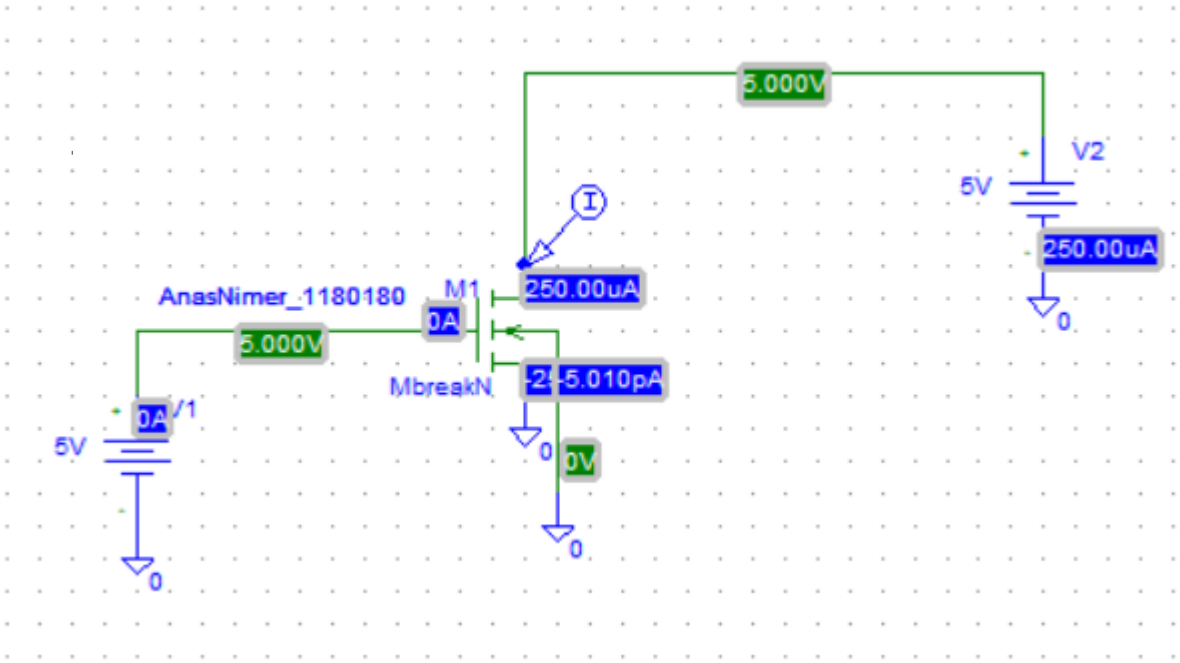
When a MOS transistor reaches equilibrium, the electric field around the pinch-off region can be strong enough to excite electron-hole pairs.

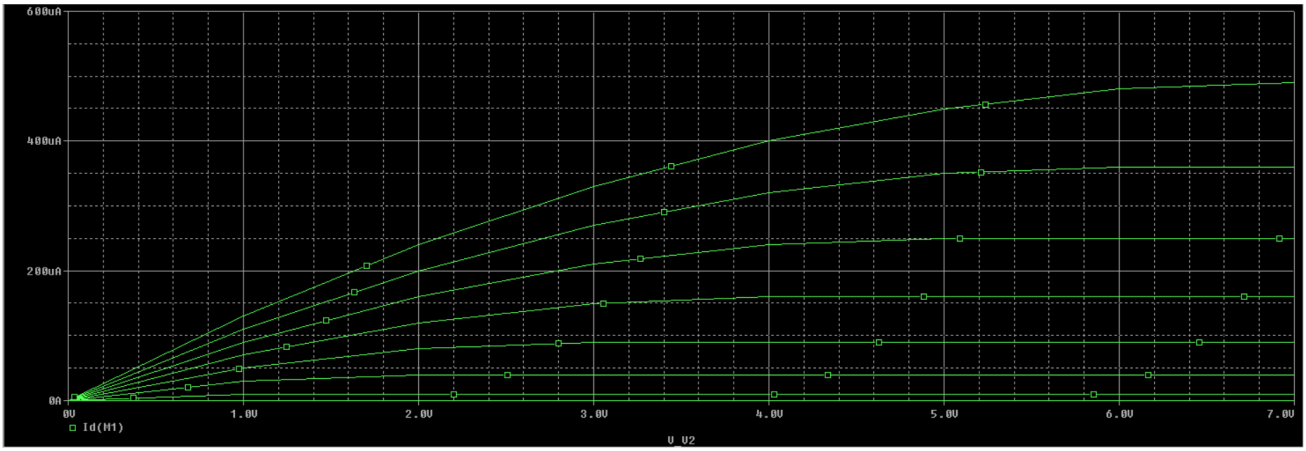
The holes (electrons) usually flow towards the p-substrate (n-well) in an n-ch (p-ch) device, increasing the substrate currents (bad for latch-up).

the reliability concern is that part of the hot-e can penetrate the gate oxide. Electrons that penetrated the gate oxide remain trapped there (in normal operating conditions).

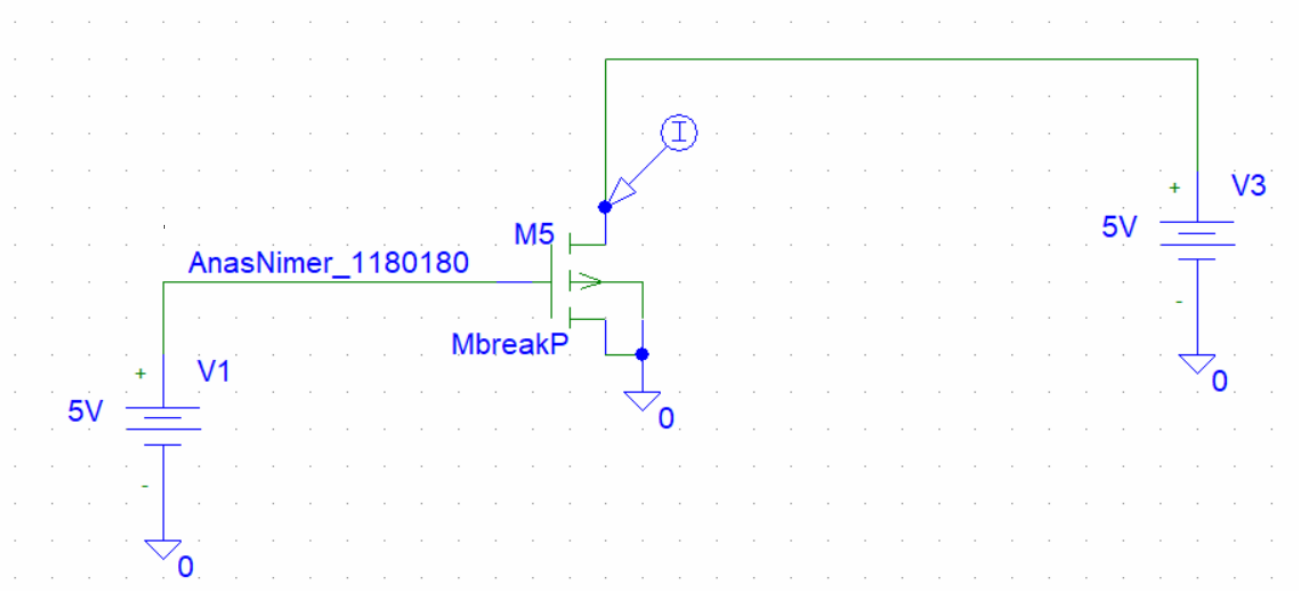
Q13:

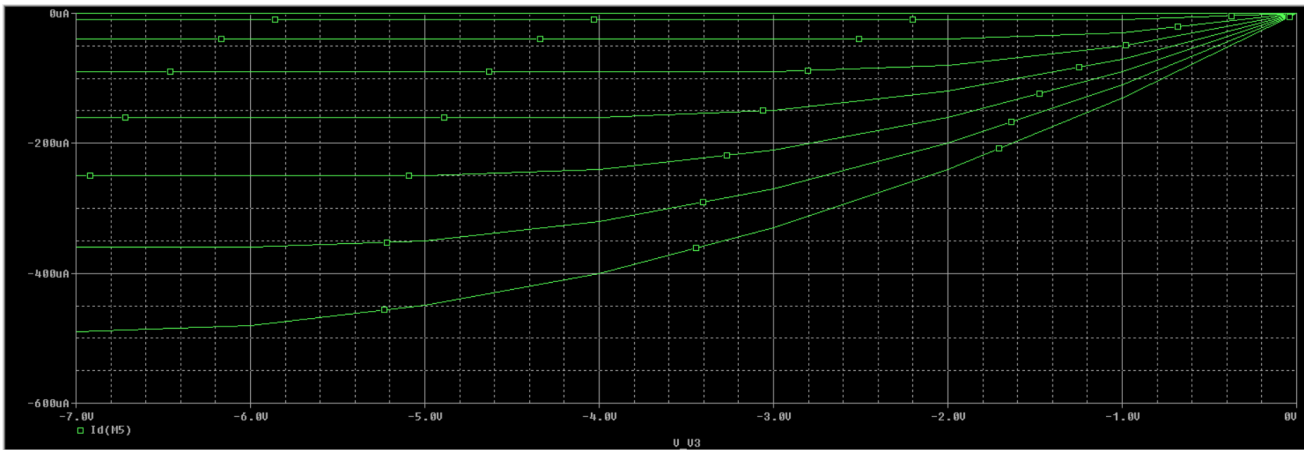
DC sweep analysis, Ids vs Vds graphs. Vgs from 0 to 7 volt, step size = 1V





Vgs from 0 to -7 volt, step size = 1V

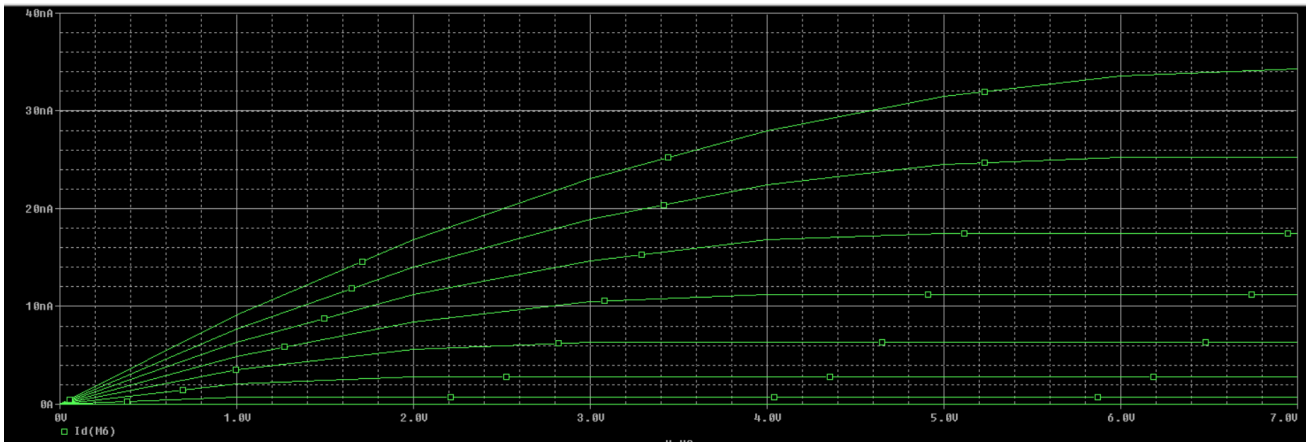




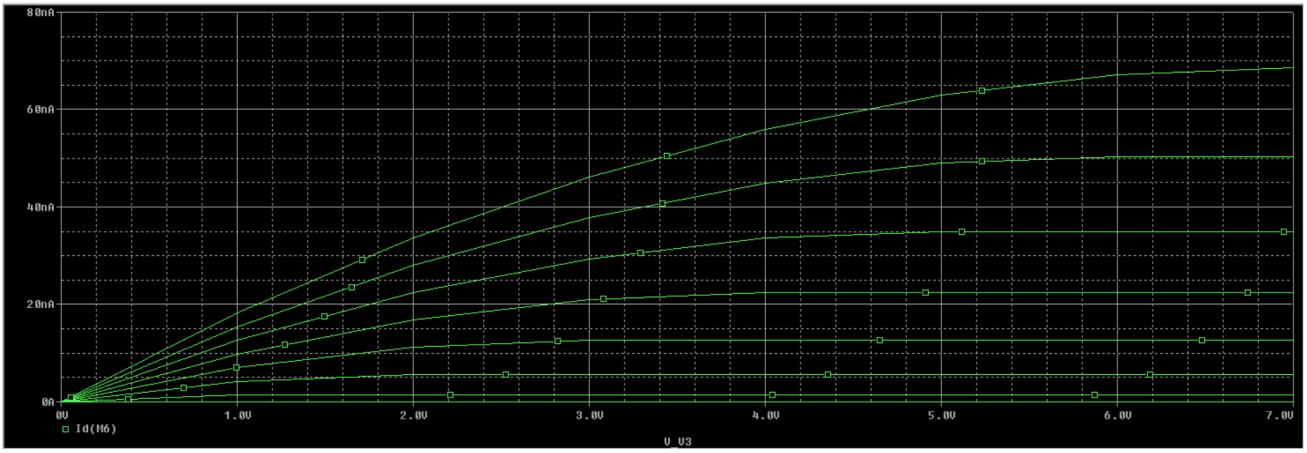
Effect of changing device width:

NMOS:

1- Changed width to 7n, notice how y-axis scaling changed which means plot was shifted.

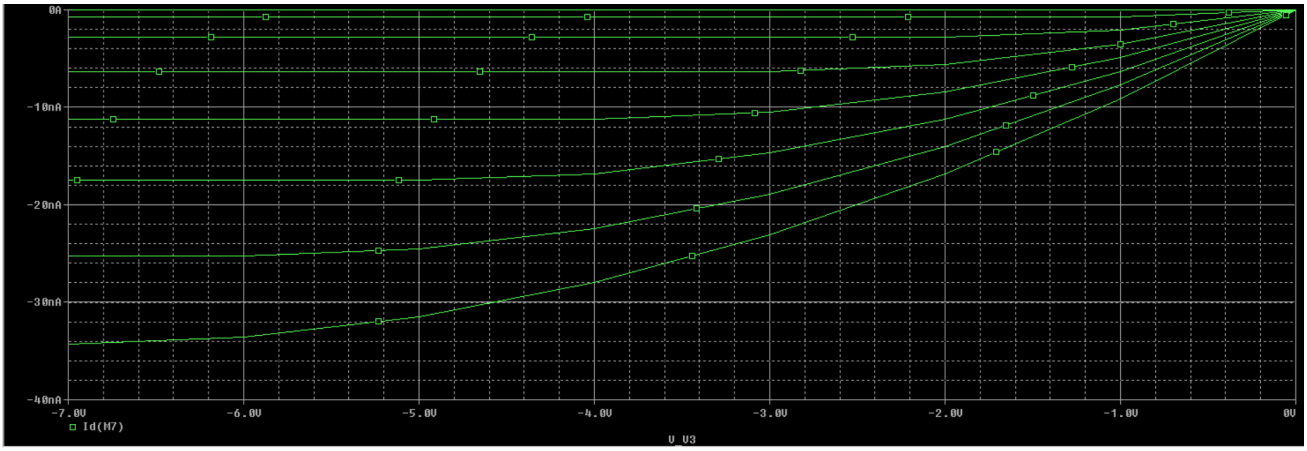


2- Changed width to 14n (notice the change in y-axis which represents current):



PMOS:

1- Changed width to 7n, notice how y-axis scaling changed which means plot was shifted.



2- Changed width to 14n (notice the change in y-axis which represents current):