

# **Faculty of Engineering & Technology**

# **Electrical & Computer Engineering Department**

**ENCS333**

**Homework#1**

**Prepared by : Tareq Shannak**

**ID Number : 1181404**

**Instructor : Dr. Khader Mohammad**

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# Question 1

This question about IC History: the past, current and future. Please read chapter. **Summarize in 2 paragraph the history of the past, current and future of IC design.**

## Sol:

According to Moore’s Law, the number of transistors in ICs doubles every 18 months. At present, the number of transistors in ICs has reached dozens of billions. Also Clock frequency doubles every two years, die size grows by 14% every year, powers increase about ten times every 3 years, power densities increase twice every year, the minimum length of gate is divided by two every 5.4 years and cost of transistors reduce twice every 1.5 years.

Technology in past was very tall unlike the technology which Intel reached it (7nm) in 2016. From past to current time, the number of pins, IC size, maximum power and number of transistors in cm2 increase, it is expected that in future these attributes and values will also increase.

# Question 2

Read Chapter 2and summarize in less than two paragraph **The CMOS Manufacturing Process.**

## Sol:

The CMOS process requires that both n-channel (NMOS) and p-channel (PMOS) transistors be built in the same silicon material. To accommodate both types of devices, special regions called wells must be created in which the semiconductor material is opposite to the type of the channel. A PMOS transistor has to be created in either an n-type substrate or an n-well, while an NMOS device resides in either a p-type substrate or a p-well. The cross section features an n-well CMOS process, where the NMOS transistors are implemented in the p-doped substrate, and the PMOS devices are located in the n-well. Modern processes are increasingly using a dual-well approach that uses both n- and p-wells, grown on top on an epitaxial layer. We will restrict the remainder of this discussion to the latter process (without loss of generality).

The CMOS process requires a large number of steps, each of which consists of a sequence of basic operations. A number of these steps and/or operations are executed very repetitively in the course of the manufacturing process. Rather than diving directly into a description of the overall process flow, we first discuss the starting material followed by a detailed perspective on some of the most-often recurring operations.

# Question 3

CMOS Devices: SPICE and deep sub-micron issues

1. Using any source, explain what do we mean by CMOS?
2. What do we need to run SPICE simulations for CMOS? Give an example?

## Sol:

1. Stands of Complementary Metal Oxide Semiconductor, which works as inverter using MOS transistors.
2. Just Ntype and Ptype MOS and square wave input which will be inverted.

# Question 4

In one or two paragraph, explain the difference between Wafer, Die and Package in terms of design and engineers who can work /design each stage.

## Sol:

Wafer is a thin of semiconductor can be produced from crystal silicon and wafer are used in fabrication of IC while a Die is a block of semiconducting material on which a function circuit is built. A wafer is cut into many smaller pieces and each single piece is called Die. Then printed circuit board are used to simplify integration and handling dies are packaged in various forms. The supporting case in which die is encapsulated is known as package. IC packaging is the last stage of device fabrication.

# Question 5

List in not more than one paragraph the IC Component Types?

## Sol:

Input/Output (I/O) Cells: Implement the connection between IC inner circuitry and PCB. Digital Standard Cells: Basic cells performing functions used as building blocks for large digital circuits. Intellectual Property (IP) Blocks: Large blocks performing completed functions used in large designs. Digital ICs: Large ICs (e.g. processor, GPU, etc.), distributed to end-users.

# Question 6

## What do we mean by Doping the Semiconductor? What is the difference between Ntype and Ptype materials?

## Sol:

A manufacturing process that adds free charge carriers (free electron or hole) into a pure semiconductor material to increase its conductivity. There is two categories: Ntype or Ptype. Ntype is by adding (to silicon) atom which has 5 valence electrons as phosphorus, this atom forms covalent bonds with 4 adjacent silicon atoms, while the fifth becomes a conduction electron since it is not attached to any atom. Unlike the Ntype, Ptype is by adding atom which has 3 valence electrons as boron or gallium, so it will create a hole. The majority carriers in Ntype are electrons and the minority carriers are holes unlike Ptype.

# Question 7

Explain how do we generate a depletion layer and how does that affect the capacitance for both NMOS and PMOS

## Sol:

When a positive voltage now is applied to the gate in Ntype, which is done by introducing positive charge Q to the gate, then some positively charged holes in the semiconductor nearest the gate are repelled by the positive charge on the gate, and exit the device through the bottom contact. They leave behind a depleted region that is insulating because no mobile holes remain; only the immobile, negatively charged acceptor impurities. The greater the positive charge placed on the gate, the more positive the applied gate voltage, and the more holes that leave the semiconductor surface, enlarging the depletion region. (In this device there is a limit to how wide the depletion width may become. It is set by the onset of an inversion layer of carriers in a thin layer, or channel, near the surface.

# Question 8

Explain all Levels of IC Design?

## Sol:

# Interconnect Level 1 —Die-to-Package-Substrate

1. Interconnect Level 2—Package Substrate to Board
2. Multi-Chip Modules—Die-to-Board

* Device Model
* Transistor
* Gate
* Module
* System/ Architecture

# Question 9

## What do we mean by technology file, technology scaling and how does that affect functionality, cost and power of the design?

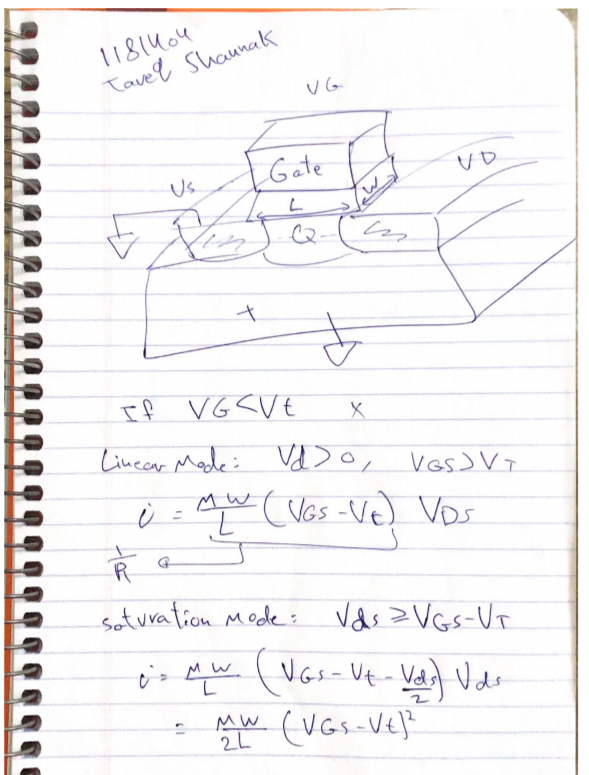
## Sol:

Technology means the gate length and it shrinks by 0.7/generation, with every generation can integrate 2x more, functions per chip; chip cost does not increase significantly, Cost of a function decreases by 2x. It get faster, cheaper, smaller and less power, but the power densities increase. Scaling increases the switching speed, reduces chip size and reduces power dissipation.

# Question 10

## Draw the cross section physical view of the MOS transistor and then derive the current equation for PMOS and NMOS in all region of operation.

## Sol:



# Question 11 & Question 12 are repeated