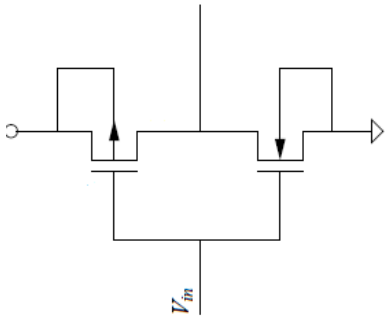
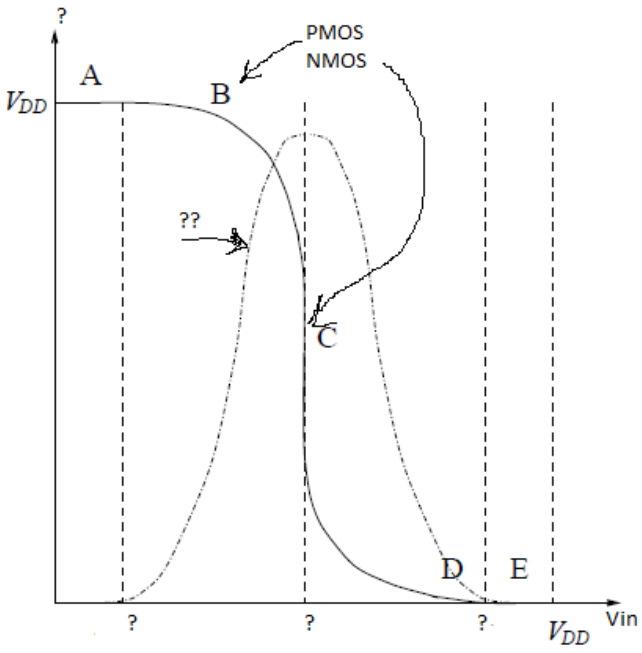
1. **Label all G,D,S , VDD, GND, Vout for the inverter below**



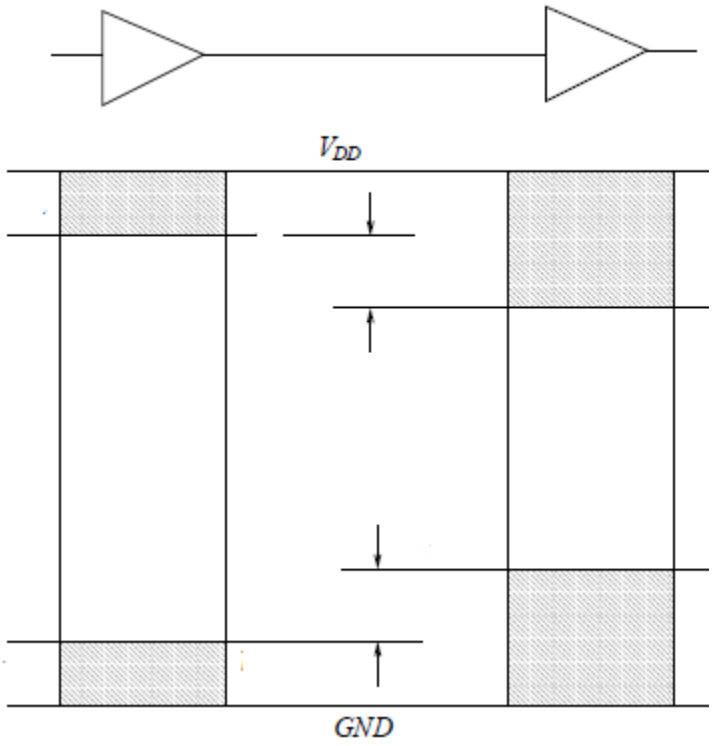

2. **Add labels for each ( ? ) voltages , current (i), Vout, Vin and the status ( cut ofF, Linear, Saturation) for the PMOS and NMOS in each region (AB,B,C,D)**




3. **For each region as in question 2, complete the table below**

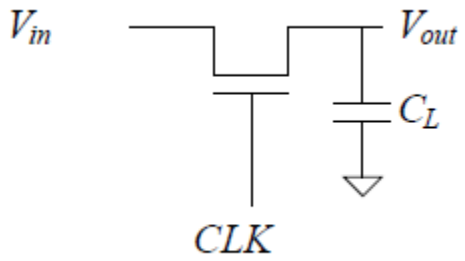
| Region | Condition | PMOS | NMOS | Vout |
|---|---|---|---|---|
| A | | | | |
| B | | | | |
| C | | | | |
| D | | | | |
| E | | | | |

4. **Noise Margin: Label all voltages VOH, VOL, NMH and NML , VIL, VIH , High output, High Input, Low output, Low input in the figure below?**




5. **The High output excursion should not be larger than the high input excursion, same for low excursion, What will happen if this is violated ?**

6. **Given a circuit below :**



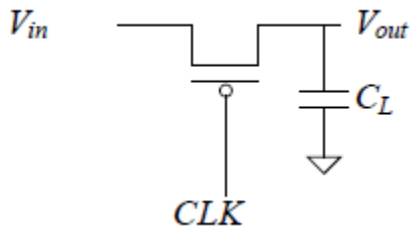

Assume Vout =0 initially,

1) If CLK =0, what will be
   - Vgs =
   - What region the device will be in =

- Vout =

2) If CLK =VDD, what will be
   - Vgs =
   - What region the device will be in =
   - Vout =

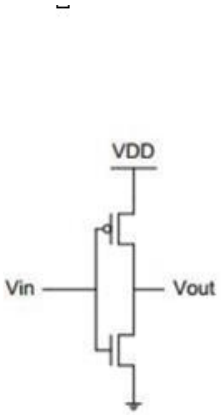
**7. Given a circuit below :**

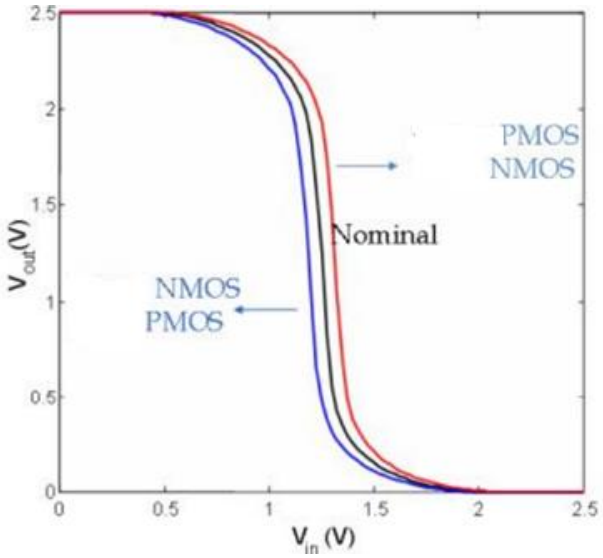



Assume Vout =0 initially,

3) If CLK =VDD, what will be
   - Vgs =
   - What region the device will be in =
   - Vout =
4) If CLK =0, what will be
   - Vgs =
   - What region the device will be in =
   - Vout =

**8. Givin circuit and simulation recult as shown in figure below, can you elaborate which curve have strong PMOS and which curve have Strong NMOS ?**
**What does Weak NMOS mean ?**
**What Does Weak PMOS mean ?**




**9. List the following interconnect fabrication steps in chronological order:**

- Etch metal.

Expose photoresist using mask.

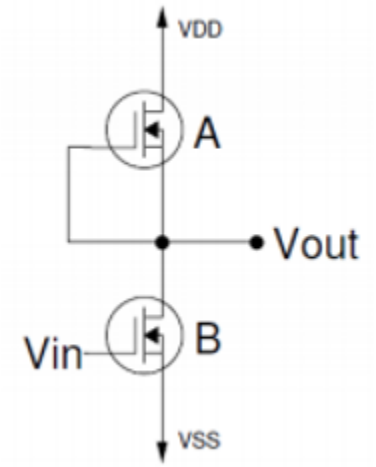
- Remove all photoresist.
- Deposit photoresist.
- Deposit metal everywhere.

**10. If a designer wants a perfectly balanced rise time and fall time for a CMOS inverter driving a capacitive load, what should the ratio of NMOSFET to PMOSFET transistor widths be? Simplifications: Assume, when answering this question, that the fabrication process under consideration allows lines of arbitrary width. When solving this problem, ignore the effect that changing width has on MOSFET capacitance. We will revisit this problem later in the course when we have learned more about MOSFET structure and capacitance.**

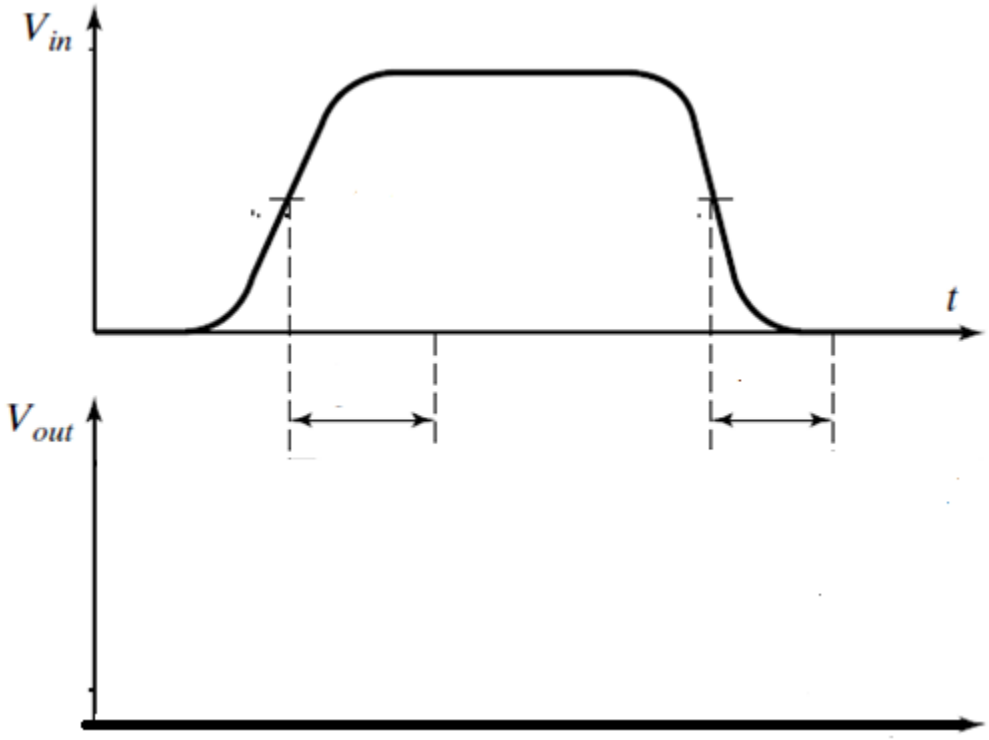
**11. Consider the circuit below.**

Device B is a standard NMOS.
Device A has the same properties as B, except that its device threshold voltage, VT is -0.4 V (it is negative).
Assume that all the current equations and inequality equations (to determine the mode of operation) for the depletion device A are the same as an enhancement-mode NMOSFET. VDD = 2.5 V.

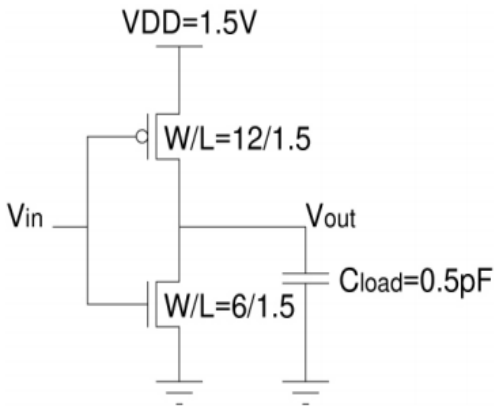
(a) If V in = 0 V, what is V out? In steady state, what is the mode of operation for device A?
(b) Compute the output voltage for V in = 2.5 V.
(c) Find Pav




**12. Inverter propagation delay: time delay between input and output signals; figure of merit of logic speed. Assume figure below showed the input to an inverter, complete the figure by showing /labeling tpHL,tpLH,tf,tr.**



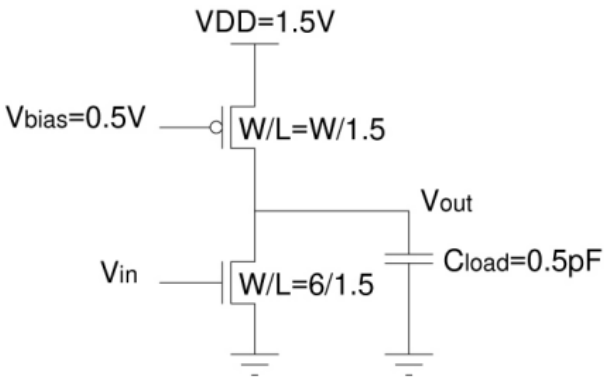
**13. Consider the CMOS inverter pictured below. Take channel length modulation into account.**




| Parameter | NMOS | PMOS |
|---|---|---|
| $V_{TO}$ | 0.5 V | -0.5 V |
| μ | 220 $cm^2/Vs$ | 110 $cm^2/Vs$ |
| λ | 0.1 $V^{-1}$ | 0.1 $V^{-1}$ |
| $T_{ox}$ | 15 nm | 15 nm |

Dimensions of W and L are in μm
a) Calculate VM, the voltage midpoint.
b) Calculate AV, the voltage gain at Vin=VM.
c) Calculate NML and NMH, the noise margin low and noise margin high. d) Calculate tPHL and tPLH, the propagation delay from high-to-low and propagation delay from low-to-high.

**14. Consider the circuit below, which consists of an NMOS device and PMOS current source load. Do not neglect channel length modulation. a) Calculate the width of the PMOS device so its saturation current is 50μA. b) Calculate VM, VOH, VOL. Remember, for hand calculations we assume VOH=VMAX, and VOL=VMIN. c) Calculate the voltage gain of this circuit, when Vin=VM.**


VDD=1.5V
Vbias=0.5V
W/L=W/1.5
Vout
Vin
W/L=6/1.5
Cload=0.5pF