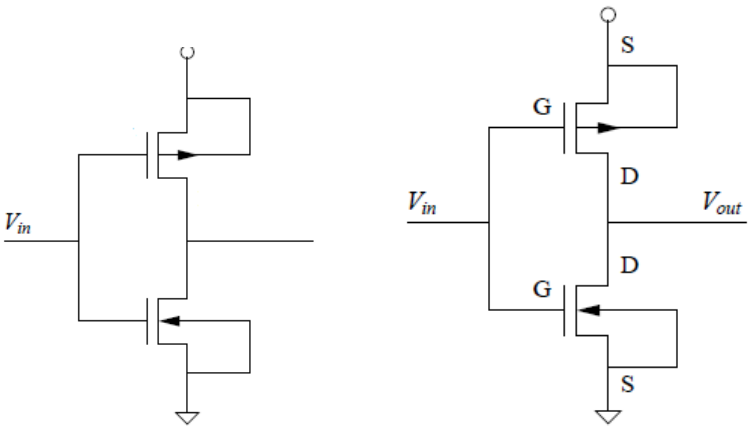
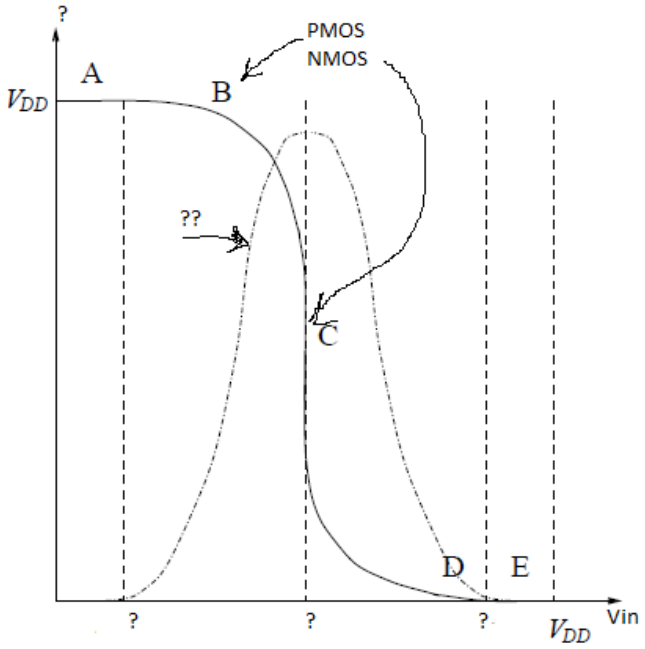
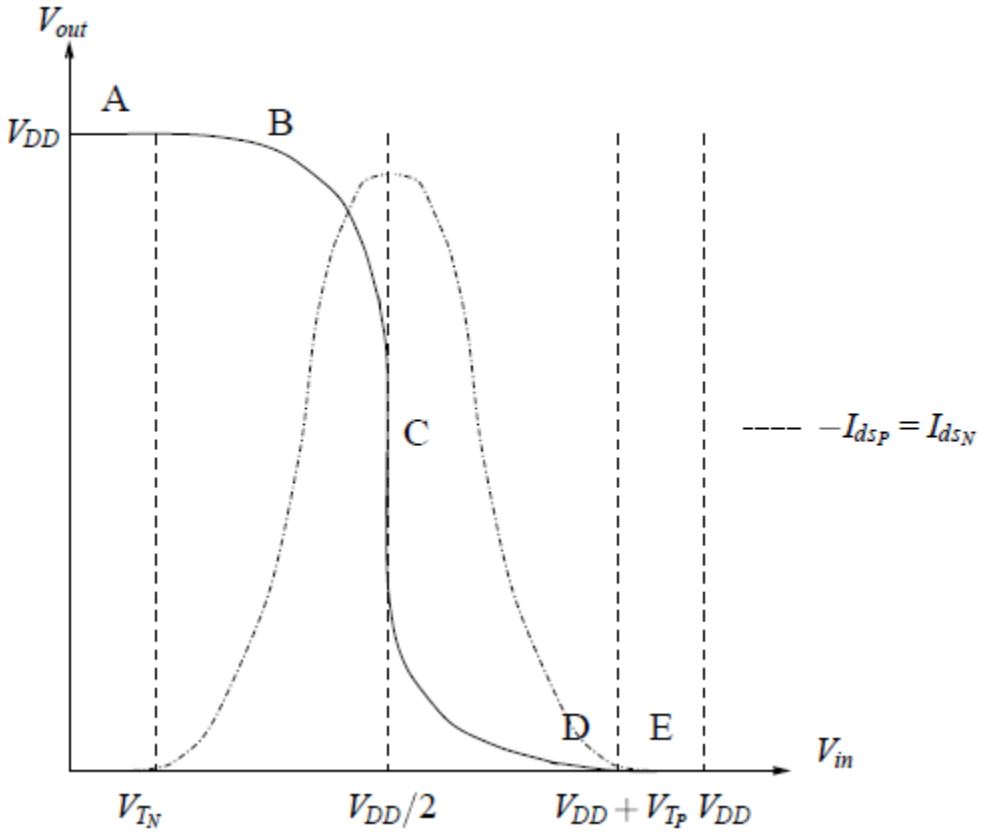
1. **Label all G,D,S , VDD, GND, Vout for the inverter below**



2. **Add labels for each (?) voltages , current (i), Vout, Vin and the status (cut ofF, Linear, Saturation) for the PMOS and NMOS in each region (AB,B,C,D)**


?
PMOS
NMOS
A
B
V_{DD}
??
C
D
E
?
?
?
V_{DD}
Vin

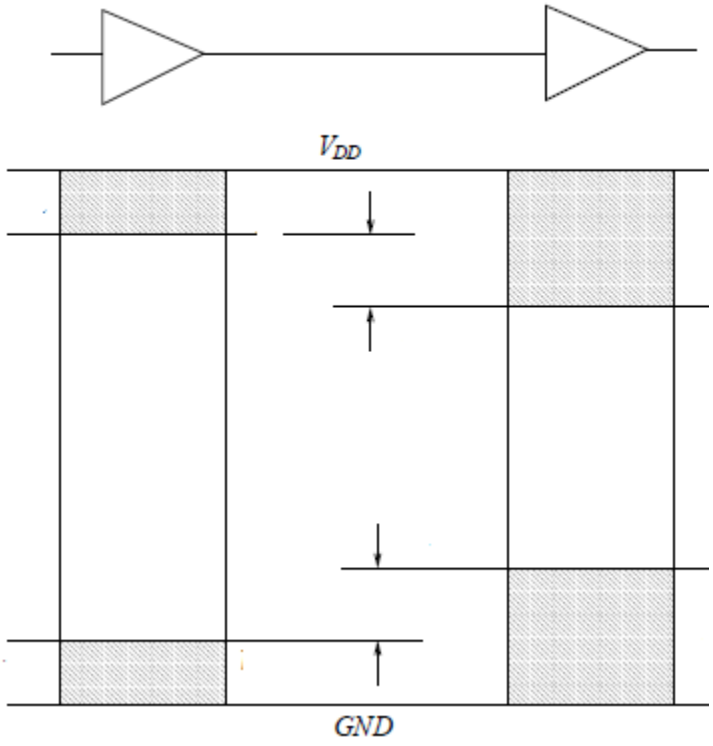

V_{out}
A
B
V_{DD}
C
D
E
V_{in}
---- $-I_{ds_P} = I_{ds_N}$
V_{T_N}
$V_{DD}/2$
$V_{DD} + V_{T_P}$
V_{DD}

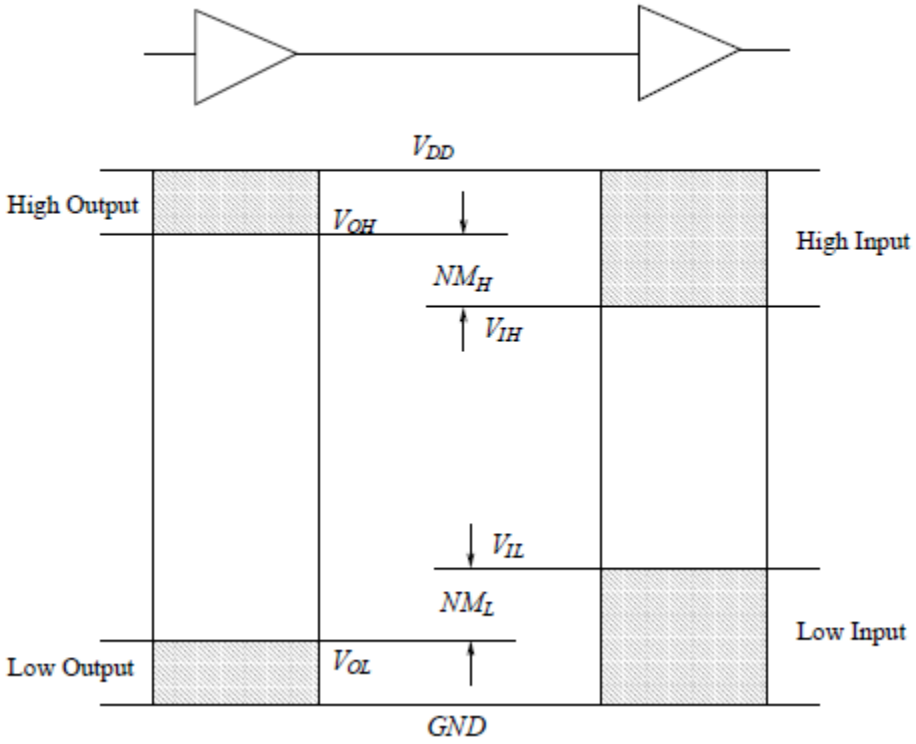
3. For each region as in question 2, complete the table below

Region	Condition	PMOS	NMOS	Vout
A				
B				
C				
D				
E				

Region	Condition	PMOS	NMOS	V_{out}
A	$0 \le V_{in} \le V_{T_N}$	linear	cutoff	V_{DD}
B	$V_{T_N} \le V_{in} \le V_{DD}/2$	linear	sat	see below
C	$V_{in} = V_{DD}/2$	sat	sat	$V_{out} \neq f(V_{in})$
D	$V_{DD}/2 \le V_{in} \le V_{DD} - \lvert V_{T_P} \rvert$	sat	linear	see below
E	$V_{in} \ge V_{DD} - \lvert V_{T_P} \rvert$	cutoff	linear	0

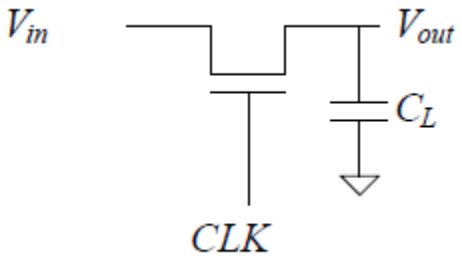
4. Noise Margin: Label all voltages VOH, VOL, NMH and NML , VIL, VIH , High output, High Input, Low output, Low input in the figure below?





5. **The High output excursion should not be larger than the high input excursion, same for low excursion, What will happen if this is violated ?**
   Corresponding noise margin will be negative

6. **Given a circuit below :**



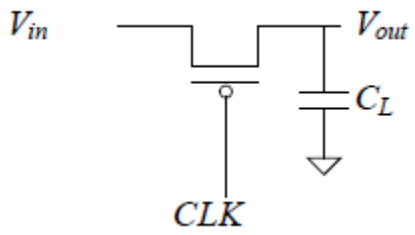
Assume Vout =0 initially,

1) If CLK =0, what will be
   - Vgs =
   - What region the device will be in =
   - Vout =
2) If CLK =VDD, what will be
   - Vgs =
   - What region the device will be in =
   - Vout =

- Assume $V_{out} = 0$ initially. If $CLK = 0$, then $V_{gs} = 0$, and the device is cutoff. Regardless of V_{in}, V_{out} remains at 0V.

- When $CLK = V_{DD}$
  - If $V_{in} = V_{DD}$
    - We have $V_{gs} - V_T = V_{DD} - V_T$, device is in the saturation region. C_L is charged. When $V_{out} = V_{DD} - V_T$, then $V_{gs} - V_T = 0$. Device cuts off. V_{out} stays charged at $V_{DD} - V_T$.
    - However the device is on the **verge** of conduction. If for any reason V_{out} drops again, the device will turn on and pull V_{out} back up to $V_{DD} - V_T$.
    - So a NMOS transmission gate "transmits" a V_{DD} value, but drops the voltage by V_T in the process.

7. Given a circuit below :

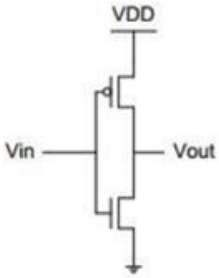


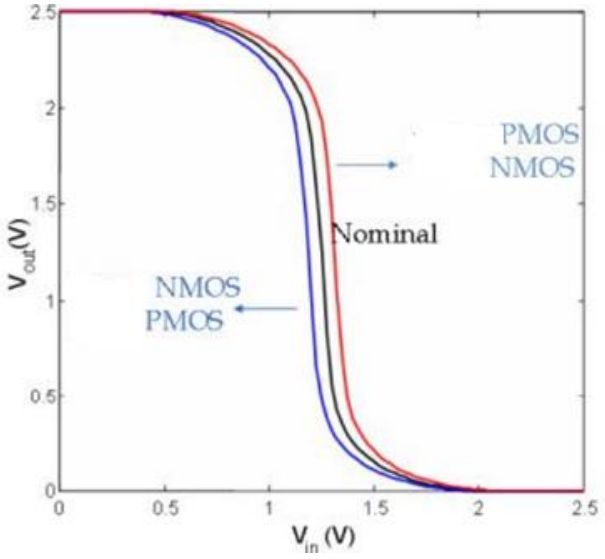
Assume Vout =0 initially,

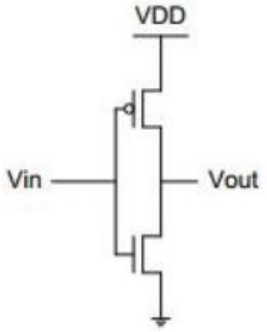
3) If CLK =VDD, what will be
   - Vgs =
   - What region the device will be in =
   - Vout =
4) If CLK =0, what will be
   - Vgs =
   - What region the device will be in =
   - Vout =

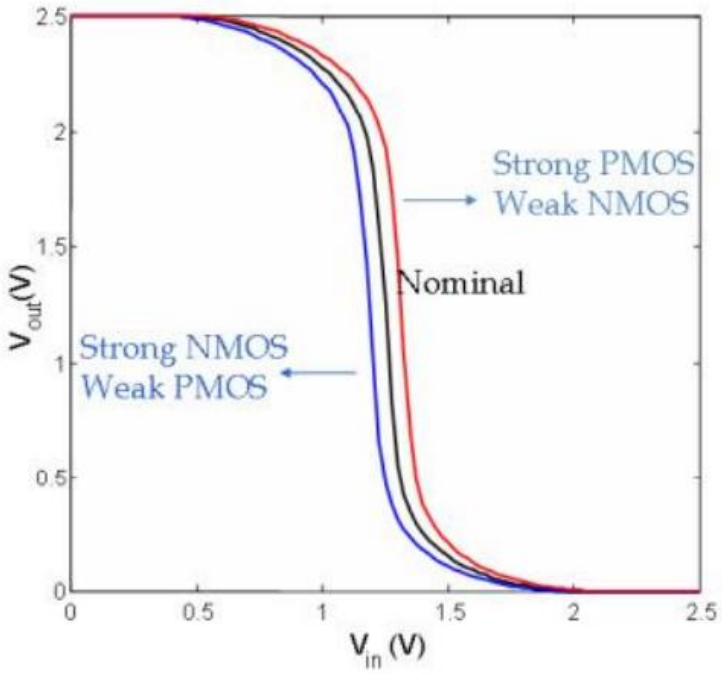
- Operation is similar to NMOS transmission gate
- Assume $V_{out} = 0$ initially. If $CLK = V_{DD}$, then the device is cutoff. Regardless of V_{in}, V_{out} remains at 0V.
- When $CLK = 0V$
  - If $V_{in} = V_{DD}$
    - Device transmits V_{DD} value without degradation
  - If $V_{in} = 0V$
    - Device transmits $0V$ value with degradation, so that $V_{out} = |V_T|$.
    - Series connected PMOS transmission gates incur this degradation just once (like in the NMOS case)

8. Givin circuit and simulation recult as shown in figure below, can you elaborate which curve have strong PMOS and which curve have Strong NMOS ?
What does Weak NMOS mean ?
What Does Weak PMOS mean ?









9. List the following interconnect fabrication steps in chronological order:

- Etch metal.

Expose photoresist using mask.

- Remove all photoresist.
- Deposit photoresist.
- Deposit metal everywhere.

1) Deposit metal everywhere.
2) Deposit photoresist.
3) Expose photoresist using mask.
4) Etch metal.
5) Remove all photoresist.

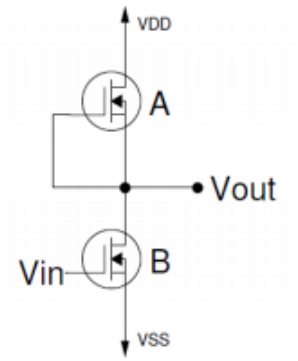
10. If a designer wants a perfectly balanced rise time and fall time for a CMOS inverter driving a capacitive load, what should the ratio of NMOSFET to PMOSFET transistor widths be? Simplifications: Assume, when answering this question, that the fabrication process under consideration allows lines of arbitrary width. When solving this problem, ignore the effect that changing width has on MOSFET capacitance. We will revisit this problem later in the course when we have learned more about MOSFET structure and capacitance.

Since the mobility of electron is normally twice of the mobility of holes, we need to make the width of PMOS twice as large as the width of NMOS.

11. Consider the circuit below.

Device B is a standard NMOS.
Device A has the same properties as B, except that its device threshold voltage, VT is -0.4 V (it is negative).
Assume that all the current equations and inequality equations (to determine the mode of operation) for the depletion device A are the same as an enhancement-mode NMOSFET. VDD = 2.5 V.

(a) If V in = 0 V, what is V out? In steady state, what is the mode of operation for device A?
(b) Compute the output voltage for V in = 2.5 V.
(c) Find Pav



V_{tA}=-0.4V V_{DD}=2.5V

(a) V_{in}=0V; this implies B is off
No current flows through A, but is on since V_{GS}=0 > -0.4V
The mode of operation of A is linear as $V_{GS}-V_t>V_{DS}$ = 0V
(Vout=2.5V as it pulled to VDD)

(b) V_{in}=2.5V and B is on
(i) First assume both A and B is in linear region:
$I_D=k_n'W/L\ [(V_{GS}-V_t)V_{DS}-V_{DS}^2/2]$

Setting two current in two devices equal:

$k_n'W/L\ [(V_{GS\_B}-V_{t\_B})V_{DS\_B}-V_{DS\_B}^2/2] = k_n'W/L\ [(V_{GS\_A}-V_{t\_A})V_{DS\_A}-V_{DS\_A}^2/2]$
$(2.5-0.4)V_{out}-V_{out}^2/2 = 0.4(2.5-V_{out}) - (2.5-V_{out})^2/2$

→ Doesn't solve

(ii) Assume B is in saturation while A is in linear:

$½\ k_n'W/L\ (V_{GS\_B}-V_{t\_B})^2 = k_n'W/L\ [(V_{GS\_A}-V_{t\_A})V_{DS\_A}-V_{DS\_A}^2/2]$
$½\ (2.5-0.4)^2 = 0.4(2.5-V_{out}) - (2.5-V_{out})^2/2$

Vout=2.1+2.062i , 2.1+2.062i → Complex, Not good.

(iii) Assume B is in linear while A is in saturation:

$k_n'W/L\ [(V_{GS\_B}-V_{t\_B})V_{DS\_B}-V_{DS\_B}^2/2]= ½\ k_n'W/L\ (V_{GS\_A}-V_{t\_A})^2$

$(2.5-0.4)V_{out}-V_{out}^2/2 = ½\ (0.4)^2$

V_{out} = 0.038V, 4.16V ($>V_{DD}$)

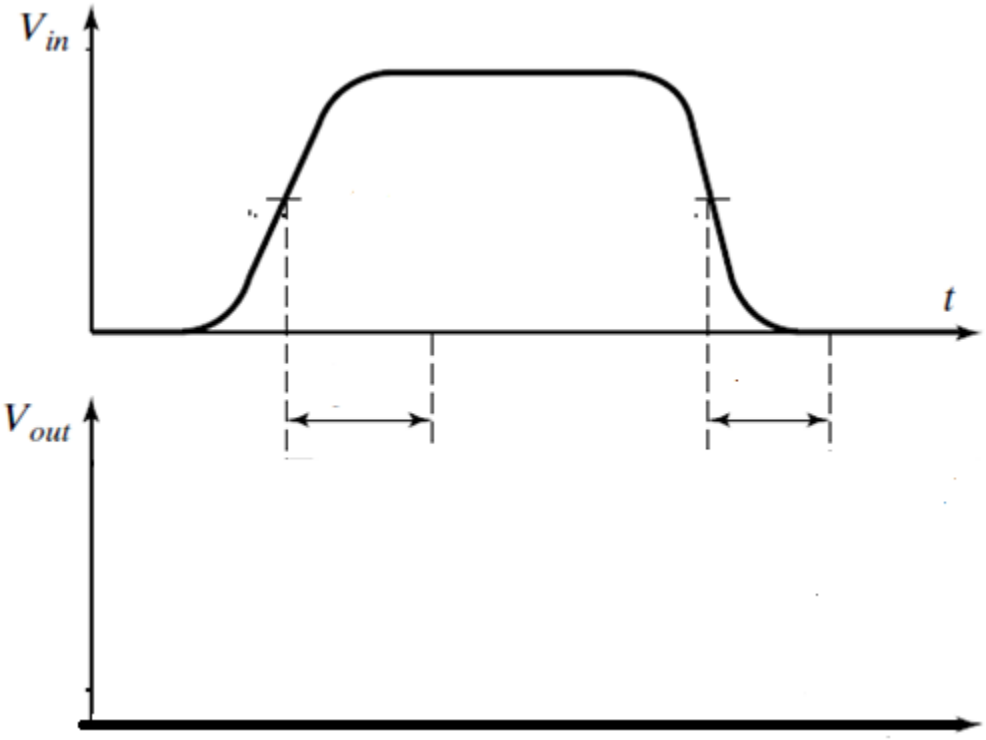
Check B is in linear: $2.5-0.038 > V_t$ → o.k.

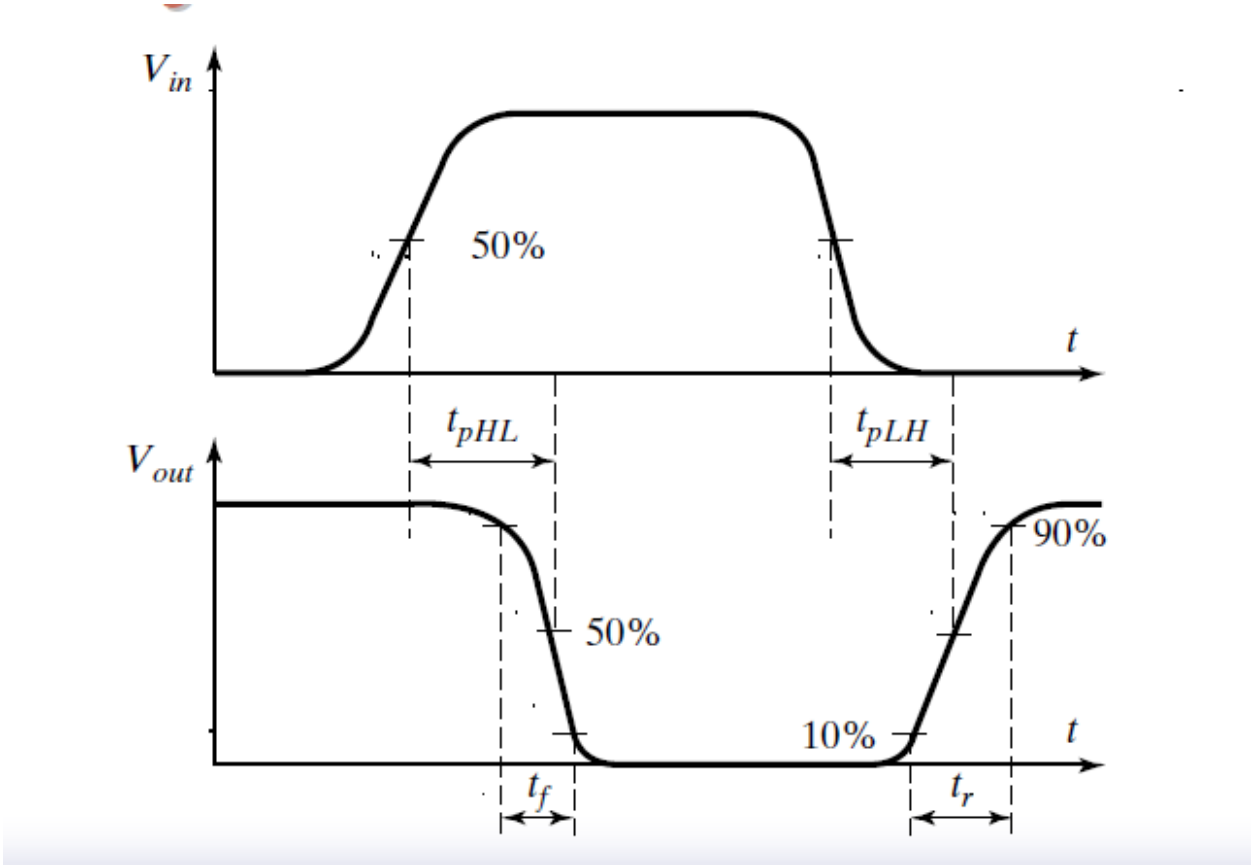
Check A is in saturation: $0-(2.5-0.038) < V_t$ → o.k.

(c) $P_{avg} = 2.5V \cdot I_D \cdot 0.7\ (V_{in}=2.5V) + 2.5V \cdot 0 \cdot 0.3\ (V_{in}=0V)$

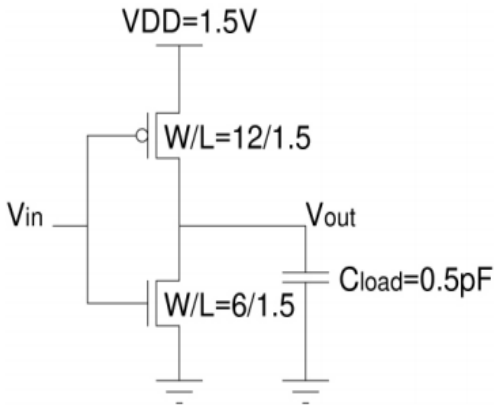
$= 2.5V \cdot (\ ½\ k_n'\ W/L\ (0.4)^2\ ) * 0.7 = 0.14 \cdot k_n' \cdot\ W/L$ Watt

12. Inverter propagation delay: time delay between input and output signals; figure of merit of logic speed. Assume figure below showed the input to an inverter, complete the figure by showing /labeling tpHL,tpLH,tf,tr.





13. Consider the CMOS inverter pictured below. Take channel length modulation into account.



Parameter	NMOS	PMOS
V_{TO}	0.5 V	-0.5 V
μ	220 cm^2/Vs	110 cm^2/Vs
λ	0.1 V^{-1}	0.1 V^{-1}
T_{ox}	15 nm	15 nm

Dimensions of W and L are in µm
a) Calculate VM, the voltage midpoint.
b) Calculate AV, the voltage gain at Vin=VM.
c) Calculate NML and NMH, the noise margin low and noise margin high. d) Calculate tPHL and tPLH, the propagation delay from high-to-low and propagation delay from low-to-high.

a) We set the drain current of the PMOS equal to the drain current of the NMOS, and plug in Vin=Vout=VM.

VM=0.75V b) Voltage gain, Av= -(gmn+gmp)*(ron||rop) gmn=gmp=50µS ron=rop=1.47MΩ Av=-74 c)NML=VM + (VDD-VM)/AV=0.74V NMH= VDD-VM + VM/AV=0.74V d) propagation delay = ΔV*C/ I ΔV = 0.75V = 50% of the total value C= 500fF ID,pmos=ID,nmos= 202µA TPH=TPL =1.856ns

V_M=0.75V

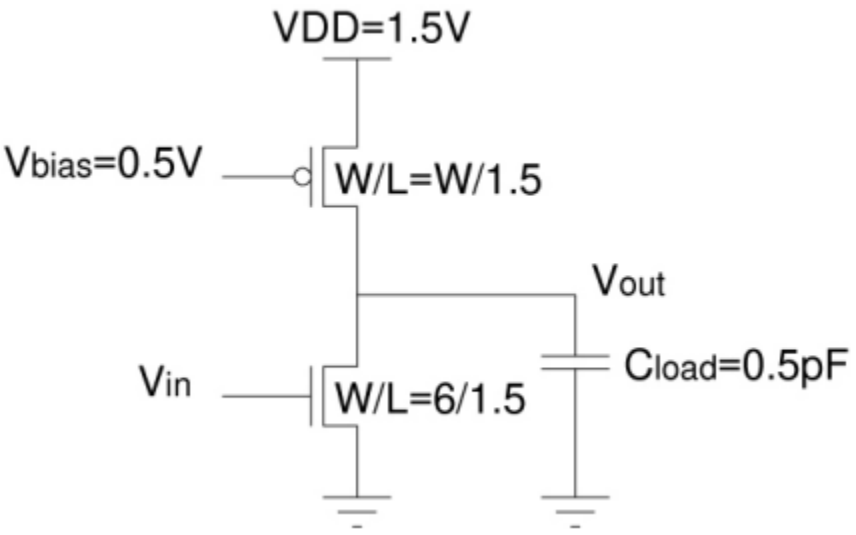
b) Voltage gain, Av= -(g_{mn}+g_{mp})*(r_{on}||r_{op})
g_{mn}=g_{mp}=50µS
r_{on}=r_{op}=1.47MΩ
A_v=-74

c)NM_L=V_M + (V_{DD}-V_M)/A_V=0.74V
NM_H= V_{DD}-V_M + V_M/A_V=0.74V

d) propagation delay = ΔV*C/ I
ΔV = 0.75V = 50% of the total value
C= 500fF
$I_{D,pmos}$=$I_{D,nmos}$= 202µA

T_{PH}=T_{PL} =1.856ns

14. Consider the circuit below, which consists of an NMOS device and PMOS current source load. Do not neglect channel length modulation. a) Calculate the width of the PMOS device so its saturation current is 50µA. b) Calculate VM, VOH, VOL. Remember, for hand calculations we assume VOH=VMAX, and VOL=VMIN. c) Calculate the voltage gain of this circuit, when Vin=VM.



a) $50\mu A = \frac{1}{2}\frac{W}{1.5}\mu_p C_{ox}(1-0.5)^2$

Width of device, W =23.7 microns

b) Setting the saturation drain current of the NMOS equal to that of the PMOS, we find

V_M=1.175V

When the input is low, the NMOS is in cutoff, therefore
$V_{OH}=V_{DD}$

When the input is high, the NMOS is in triode. Setting the current through the NMOS equal to the PMOS,

1.

a) $50\mu A = \frac{1}{2}\frac{W}{1.5}\mu_p C_{ox}(1-0.5)^2$

Width of device, W =23.7 microns

b) Setting the saturation drain current of the NMOS equal to that of the PMOS, we find

V_M=1.175V

When the input is low, the NMOS is in cutoff, therefore
$V_{OH}=V_{DD}$

When the input is high, the NMOS is in triode. Setting the current through the NMOS equal to the PMOS,

$$\frac{1}{2}\frac{23.7}{1.5}\mu_p C_{ox}(1-0.5)^2(1+.1(V_{DD}-V_{min})) = \frac{6}{1.5}\mu C_{ox}\left(V_{DD}-\frac{V_{min}}{2}-0.5\right)V_{min}$$

$V_{MIN}=V_{OL}$= 0.33V

c) For this circuit, the voltage gain is $-g_{mn} * (r_{on}\|r_{op})$

$$g_m = \sqrt{2\frac{W}{L}\mu C_{ox} I_{DSat}} = 0.144 \text{ mA/V}$$

$$r_{on} = r_{op} = \frac{1}{\lambda I_D} \rightarrow I_D = 50\mu A \ , \ r_o = 200k\Omega$$

A_v=-14