1. Need to understand and solve all HW questions

   Area will be covered in Midetrm:

   - Semiconductor material: pn-junction, NMOS, PMOS
   - IC Manufacturing Process
   - Design Metrics CMOS
   - Transistor Devices
   - The CMOS inverter
   - Combinational logic structures
   - Layout design rules
   - basic gates
   - Static & Dynamic CMOS Logic

2. What are the main design matrices ?

3. Determine the region of operation (Cut off, Linear, Saturation, ..) in the following configurations.

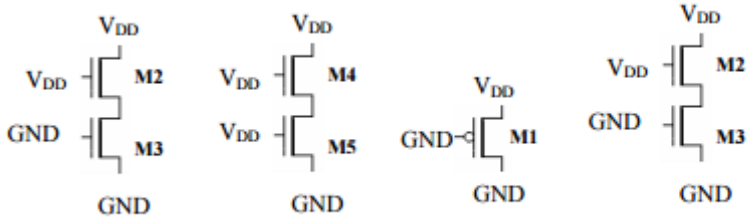
   See slides for detail answer

Ans: The three modes are: : The three modes are: (a) Accumulation mode when Accumulation mode when Vgs is much less than is much less than Vt (b) Depletion Depletion mode when mode when Vgs is equal to is equal to Vt (c) Inversion Inversion mode when mode when Vgs is greater than is greater than Vt

4. What are the three regions of operation of a MOS transistor?

Ans: The three regions are: : The three regions are: Cut-off region: This is essentially the accumulation mode, where there is no effective flow of current between the source and drain. Non-saturated region saturated region: This is the active, active, linear or week inversion region, where the drain current is dependent on both the gate and Ajit Pal, IIT Kharagpur drain voltages. Saturated region: This is the strong inversion region, where the drain current is independent of the drain drain current is independent of the drain-to-source voltage but urce voltage but depends on the gate voltage.

5. Determine the region of operation (Cut off, Linear, Saturation, Vel. saturation) in the following configurations. You may assume that all transistors have identical sizes. VDD = 2.5V. Explain your reasoning, and show your derivations if needed .



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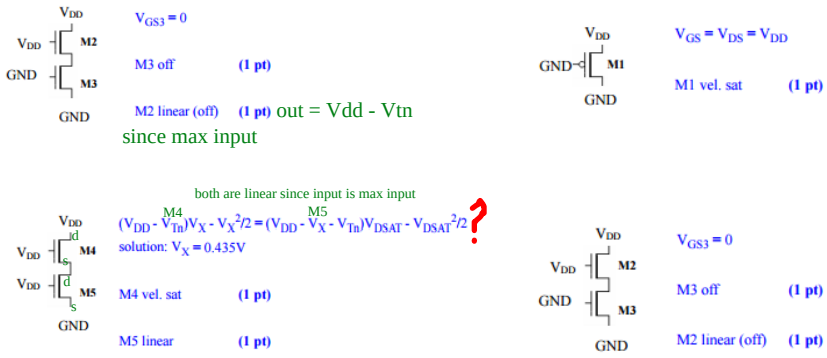


6. How does Increasing W of devices affect it's resistance, Gate capacitance and transconductance ?

decreases the resistance; allows more current to flow

Kn

A resistor: $R_n = \frac{1}{\mu_n C_{ox}(V_{GS} - V_{Tn})}\left(\frac{L}{W}\right)$

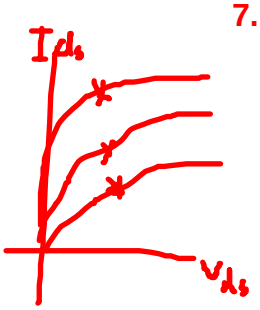
- (among other things ...) Increasing W decreases the resistance; allows more current to flow

Oxide capacitance $C_{ox} = \varepsilon_{ox}/t_{ox}$ [F/cm^2]

Transconductance $\beta_n = \mu_n C_{ox}\left(\frac{W}{L}\right) = k'_n\left(\frac{W}{L}\right)$

Gate capacitance $C_G = C_{ox}WL$ [F]

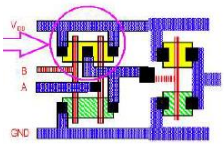
Area



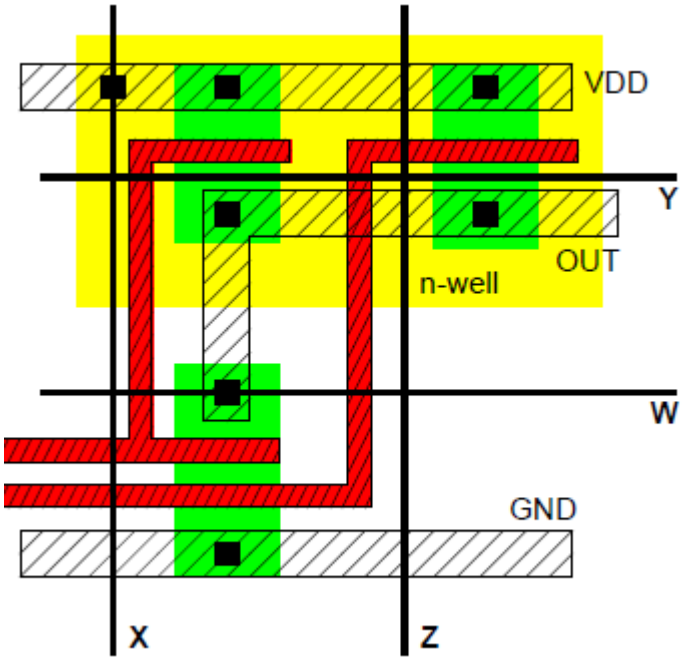
7. What is transconductance of a MOS transistor? Explain its role in the operation of the transistor.

Ans: Trans-conductance is represented by the change in drain current for change in gate voltage for constant value of drain voltage. This parameter is somewhat similar to β, the current gain of bipolar junction transistors. The Answer to the Questions of Lec Answer to the Questions of Lec-4 Ajit Pal, IIT Kharagpur the current gain of bipolar junction transistors. The following equation shows the dependence of on various parameters. As MOS transistors are voltage controlled devices, this parameter plays an important role in identifying the efficiency of the MOS transistor.

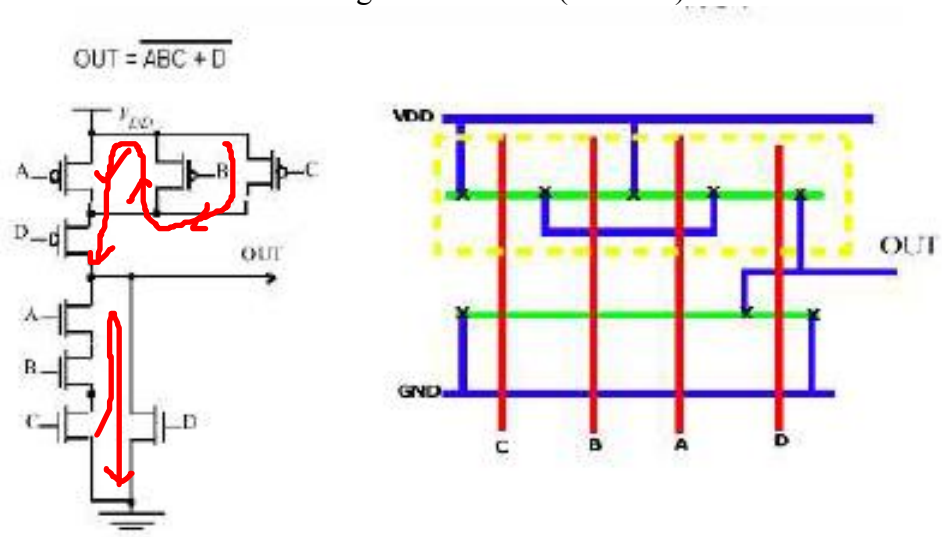
8. Explain the behaviour of a nMOS transistor as a switch.
9. Explain the behaviour of a pMOS transistor as a switch.
10. How one nMOS and one pMOS transistor are combined to behave like an ideal switch.
11. The input of a lightly loaded transmission gate is slowly changes from HIGH level to LOW level. How the currents through the two transistors vary?
12. . How its ON-resistance of a transmission gate changes as the input varies from 0 V to Vdd, when the output has a light capacitive load.
13. Draw stick digral/layout for 2-INPUT AND?



14. Mark or point to the active, via/contact , M1, poly , NWELL IN THE FIGURE BELOW



15. Draw schematic and stick diagram for Out= (ABC+D)'



16. What is the difference between Average, maximum and instantious power?

See slide notes for answer

17. Q4. Why leakage power dissipation has become an important issue in deep submicron technology?What are the main factors that affects leakage ?

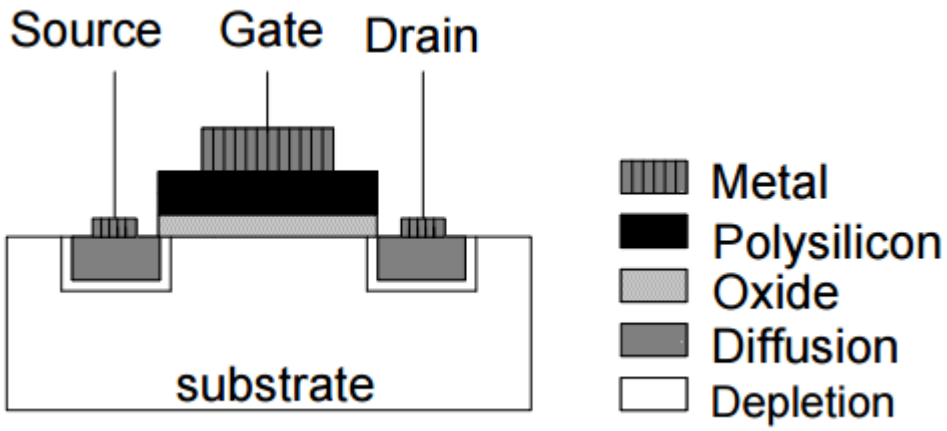
See slide notes for answer

Ans: In deep submicron technology deep submicron technology the leakage component the leakage component becomes a significant percentage of the total power and the leakage current increases at a

faster rate than dynamic power amic power in new technology generations. That is why the leakage pow generations. That is why the leakage power has become an important issue.

18. Show the basic structure of a MOS transistor.

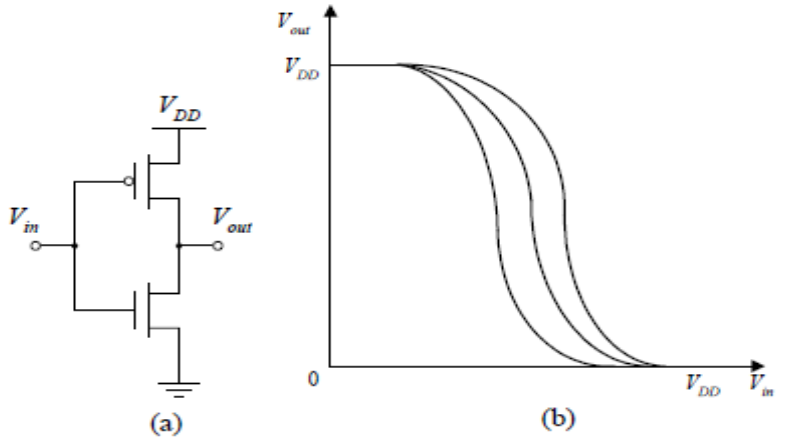
Ans: The basic structure of a MOS transistor is given below. On a lightly doped substrate of silicon two islands of diffusion regions called as source and drain, of opposite polarity of that of the substrate, are created. Between these two regions, a thin insulating layer of silicon dioxide is formed and on top of this a conducting material made of poly-silicon or metal called gate is deposited.

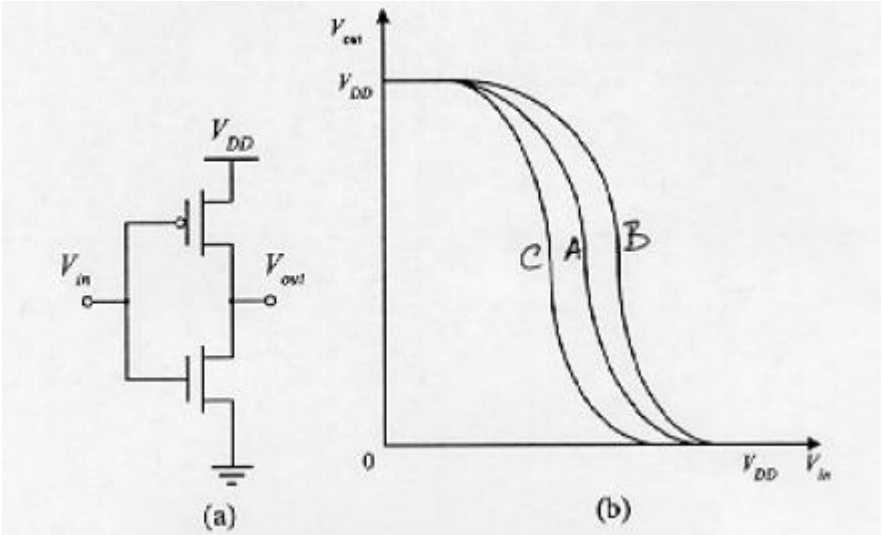


19. What are the commonly used conducting layers used in IC fabrication?

Ans: Fabrication involves fabrication of Fabrication involves fabrication of patterned laye atterned layers of the rs of the three conducting materials: metal, poly-silicon silicon and diffusion by using a series of photolithographic techniques and chemical processes involving oxidation of silicon, diffusion of impurities into the silicon and deposition and etching of aluminum or Ajit Pal, IIT Kharagpur polysilicon polysilicon on the silicon to provide interconnectio on the silicon to provide interconnection

20. Consider the CMOS inverter from below. If the NMOS transistor has channel width Wn and the PMOS transistor has channel width, Wp, label the voltage transfer characteristics from FIG. 2.b that correspond to following device sizes:
    A: W_n = 5μm, W_p = 5μm
    B: W_n = 1μm, W_p = 5μm
    C: W_n = 5μm, W_p = 1μm





Maximum, symmetrical margins $\Rightarrow V_M = \frac{V_{OH_1} + V_{OL_1}}{2}$

$V_M = 1V$

$$\frac{W_{p2}}{W_{n2}} = \frac{K_n' V_{DSAT_n}(V_M - V_{TN} - V_{DSAT_n}/2)}{K_p' V_{DSAT_p}(V_{DD} - V_M + V_{TP} + V_{DSAT_p}/2)} =$$

(Both transistors in vel. saturation)

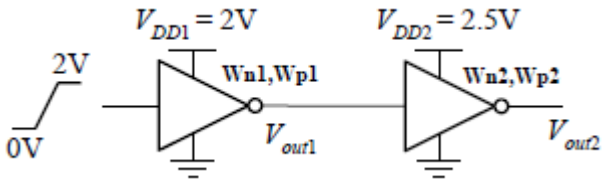
$$= \frac{115\mu}{30\mu}\ \frac{0.6}{1}\ \frac{0.3}{0.6} = 1.15$$

$W_{p2} = W_{n2} \times 1.15 = 5.75\mu m$

$W_{p2} = 5.75\mu m$

21. A CMOS inverter with supply voltage VDD1 = 2V, has to interface to a second CMOS inverter with VDD2 = 2.5V supply, as shown below

The transistor widths of the second inverter W_{n2}, W_{p2}, should be determined to assure reliable interfacing, since the high output voltage level of the first inverter is V_{OH1} = 2V. If W_{n2} = 5μm, determine the value of W_{p2}, such that these inverters are interfaced with maximum and symmetrical noise margins.



Maximum, symmetrical margins $\Rightarrow V_M = \frac{V_{OH_1} + V_{OL_1}}{2}$

$V_M = 1V$

$$\frac{W_{p2}}{W_{n2}} = \frac{K_n' V_{DSAT_n}(V_M - V_{T_n} - V_{DSAT_n}/2)}{K_p' V_{DSAT_p}(V_{DD} - V_M + V_{T_p} + V_{DSAT_p}/2)} =$$

(Both transistors in sat. saturation)

$$= \frac{115\mu}{30\mu}\,\frac{0.6}{1}\,\frac{0.3}{0.6} = 1.15$$

$W_{p2} = W_{n2} \times 1.15 = 5.75\mu m$

$W_{p2} = 5.75\mu m$

22. The inverter from FIG. below . has Wn = 1 mm and Wp = 2.5mm. VDD = 2.5V. Determine the value of VOH. Assume that the PMOS transistor operates in triode region and

$\left|\frac{V_{DS}}{2}\right| \ll |V_{GS} - V_T|$, Determine VoH also the value of V_{OL}.

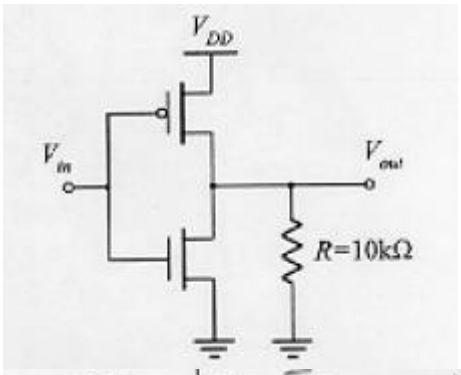


FIG. 4 CMOS inverter with resistive load

$$I_D = k' \frac{W_P}{L_P}\left[(V_{GS} - V_{TP})V_{DS} - \frac{V_{DS}^2}{2}\right] \approx$$

$$\approx k' \frac{W_P}{L_P}(V_{GS} - V_{TP})V_{DS} \quad ; \quad V_{DS} = V_{OH} - V_{DD}$$

$$V_{OH} = R \cdot I_D = R \cdot k' \frac{W}{L} \cdot (V_{GS} - V_{TP}) \cdot (-V_{DD} + V_{OH})$$

$$V_{OH} = \frac{Rk' \frac{W}{L}(V_{GS} - V_{TP})V_{DD}}{1 - Rk' \frac{W}{L}(V_{GS} - V_T)} = 2.16\,V$$

$V_{OL} = 0V$; PMOS is OFF

$V_{OH} = 2.16V$
$V_{OL} = 0V$

FORMULAS AND EQUATIONS

Diode

$$I_D = I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} \times [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \text{ (sat)}$$

$$I_D = \upsilon_{sat} C_{ox} W\left(V_{GS} - V_T - \frac{V_{DSAT}}{2}\right)(1 + \lambda V_{DS}) \text{ (velocity sat)}$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right) \text{ (triode)}$$

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) \text{ (subthreshold)}$$

Deep Submicron MOS Unified Model

$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$

and $V_{GT} = V_{GS} - V_T$

MOS Switch Model

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69 R_{eq} C_L = \frac{C_L(V_{swing}/2)}{I_{avg}}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M \approx \frac{rV_{DD}}{1+r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$\text{with } g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L\left(\frac{R_{eqn} + R_{eqp}}{2}\right)$$

$$P_{av} = C_L V_{DD}^2 f$$

Interconnect

Lumped *RC*: $t_p = 0.69\,RC$

Distributed *RC*: $t_p = 0.38\,RC$

RC-chain:

$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o}$$