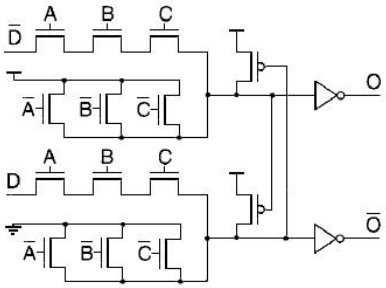
1. What is the logic function of the following gate?



O=ABCD

FORMULAS AND EQUATIONS

Diode

$$I_D = I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} \times [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \text{ (sat)}$$

$$I_D = \upsilon_{sat} C_{ox} W\left(V_{GS} - V_T - \frac{V_{DSAT}}{2}\right)(1 + \lambda V_{DS}) \text{ (velocity sat)}$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right) \text{ (triode)}$$

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) \text{ (subthreshold)}$$

Deep Submicron MOS Unified Model

$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$

and $V_{GT} = V_{GS} - V_T$

MOS Switch Model

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69 R_{eq} C_L = \frac{C_L(V_{swing}/2)}{I_{avg}}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M \approx \frac{rV_{DD}}{1+r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

with $g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L\left(\frac{R_{eqn} + R_{eqp}}{2}\right)$$

$$P_{av} = C_L V_{DD}^2 f$$

Interconnect

Lumped *RC*: $t_p = 0.69\ RC$

Distributed *RC*: $t_p = 0.38\ RC$

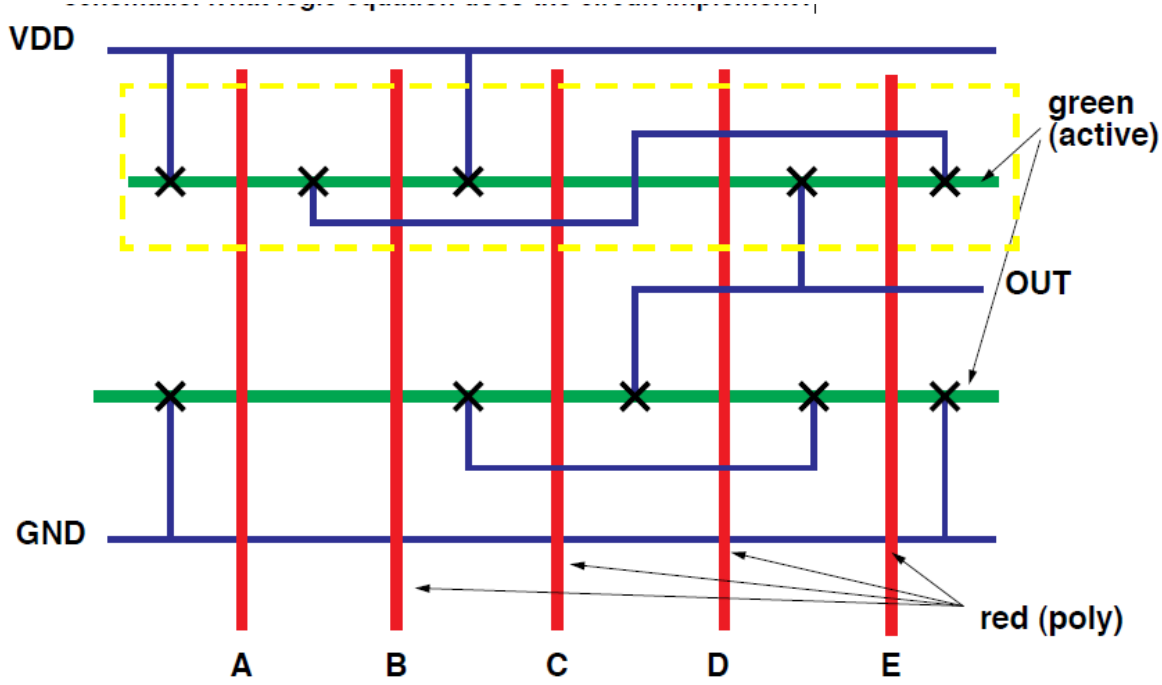
RC-chain:

$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o}$$

2. Consider the following stick diagram. Draw the electrically equivalent transistor-level Schematic. What logic equation does the circuit implement?



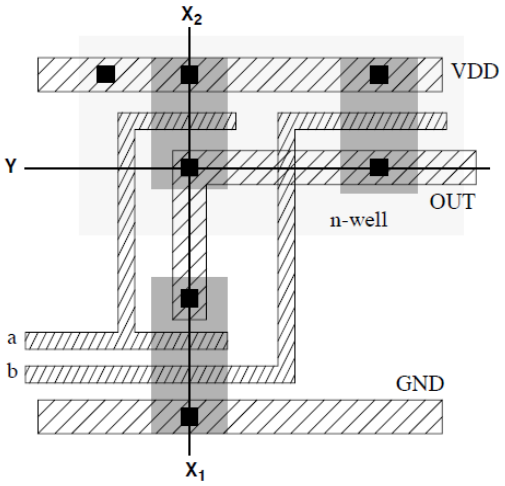
O=~(AB+E).(C+D)

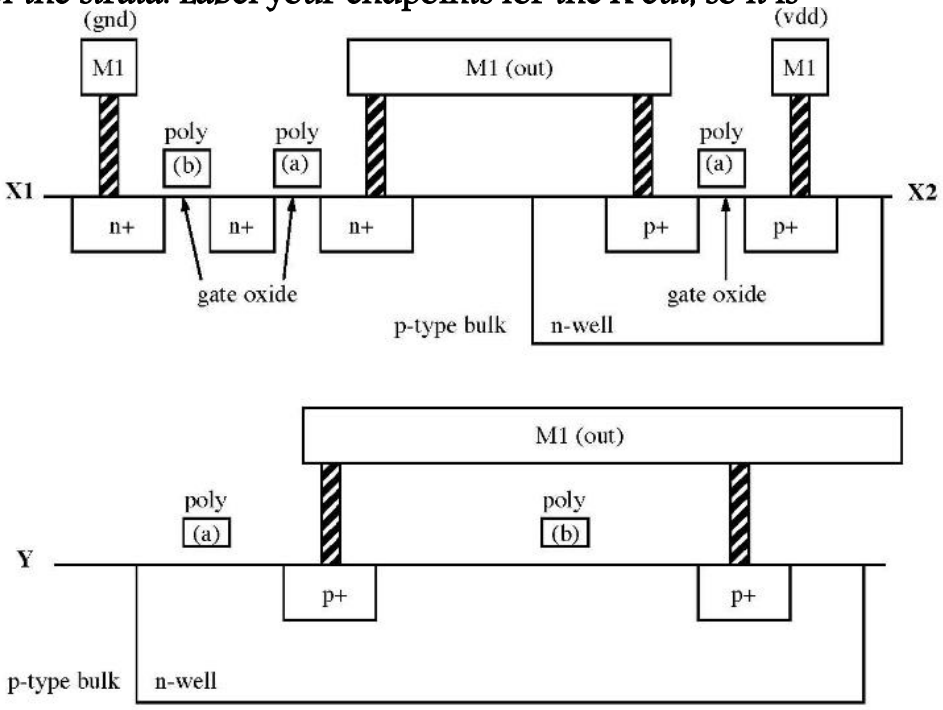
3. Consider the logical expression

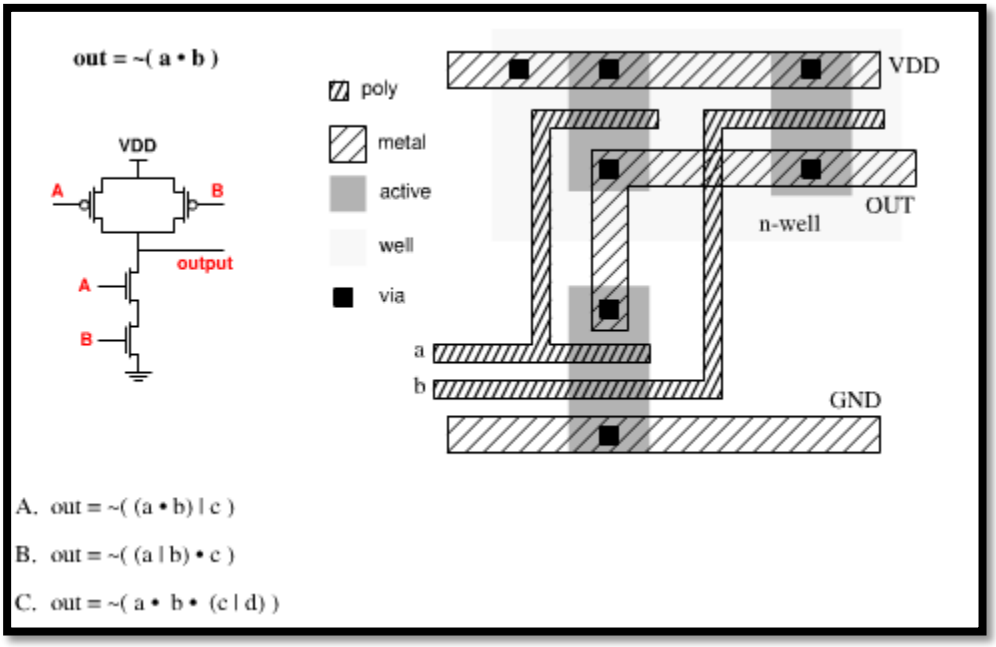
out= ~((a+b) • (c+d))

. Convert this to a schematic diagram for static CMOS logic, then convert it to a stick-diagram layout (as in question 1).

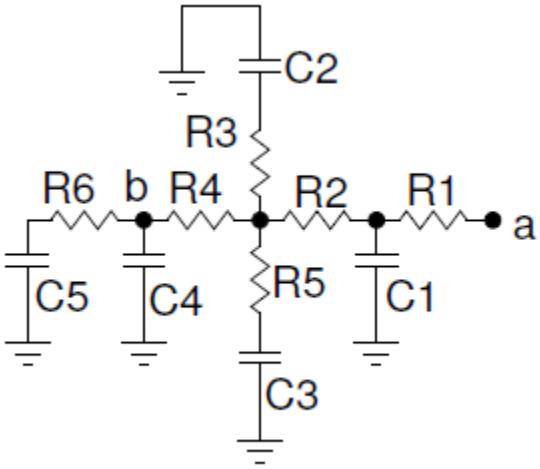
4. Provide a side-view diagram for each of the cuts X and Y through the layout below. Be sure to label each of the strata. Label your endpoints for the X cut, so it is clear which end is which.





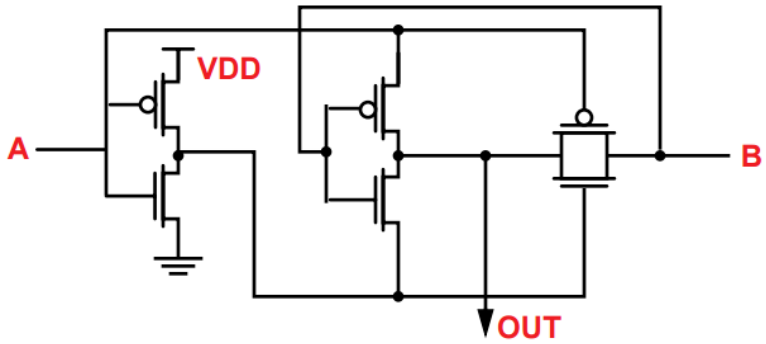


5. Determine the Elmore delay from Node a to Node b in the following circuit.

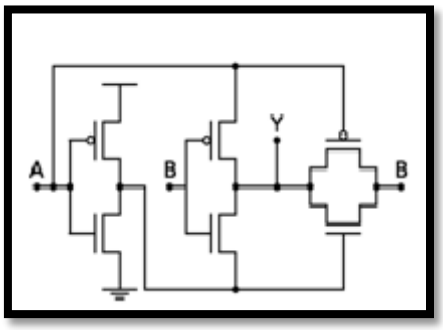


$$\tau_{ab} = R1(C1+C2+C3+C4+C5)+R2(C2+C3+C4+C5)+R4(C4+C5)$$

6. What is the output function of the following circuit?



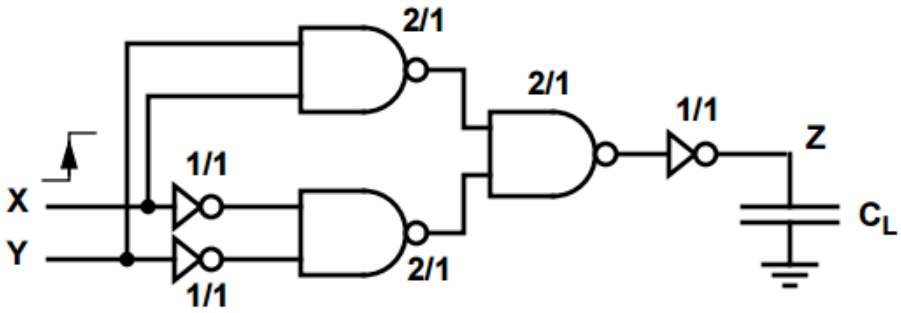
XOR



7. Consider the CMOS circuit shown below In the figure, the W/L ratios for each gate apply to both NMOS and PMOS transistors. We want to determine the delay from a rising transition (0 → 1) ……

A. Assuming that the rise and fall times are good approximations of the propagation delay, determine the delay from X to Z, in terms of τ, when Y = 0.

B. Now, assume that Y = 1. What is the new value for the propagation delay from X to Z? Can you comment on this?



2. $T = R_n C_n$

A| • transition in bottom NAND 0 to 1 $t_{PLH} = 0.69 \times \frac{2R_n}{1} \times C_n = 0.69 R_n C_n$ ④

• no transition in top NAND stays 1

• transition in top NOT from 1 to 0 $t_p = 0.69 R_n C_n$ ③

• no transition in bottom NOT

• last NAND 1 to 0 $t_{PHL} = 0.69 \times \frac{R_n}{2} \times C_n = 0.345 R_n C_n$ ②

• last NOT 0 to 1 $t_p = 0.69 R_n C_n \cdot 10 = 6.9 R_n C_n$ ①

total = $R_n C_n (6.9^{①} + 0.345^{②} + 0.69^{③} + 0.69^{④}) = \boxed{8.625 R_n C_n}$

B| • transition in top NAND from 1 to 0 $t_{PHL} = 0.345 R_n C_n$ ②

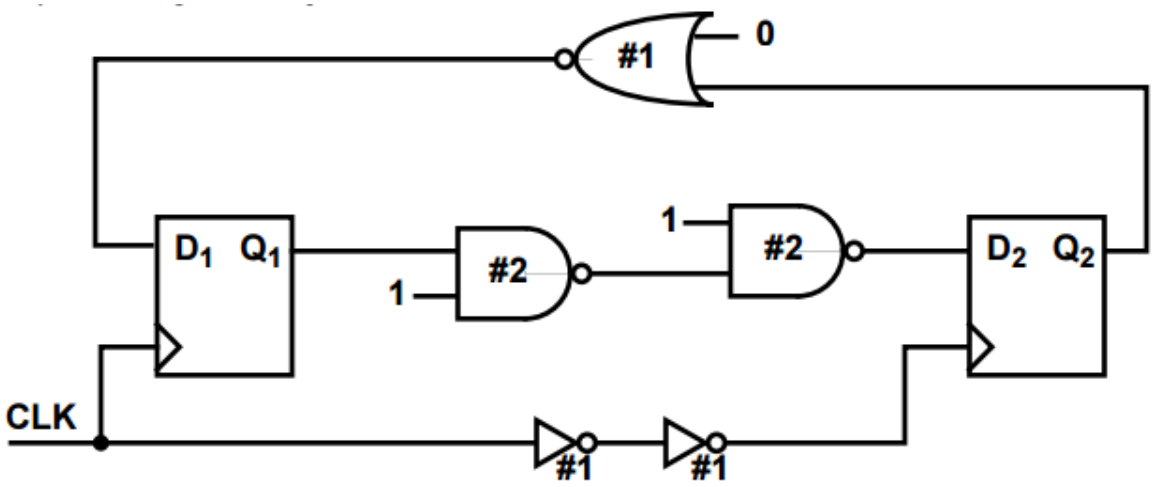
• no change in bottom NAND, so we can ignore transition in top NOT

• last NAND 0 to 1 $t_{PLH} = 0.69 \times 2R_n/2 \cdot C_n = 0.69 R_n C_n$ ①

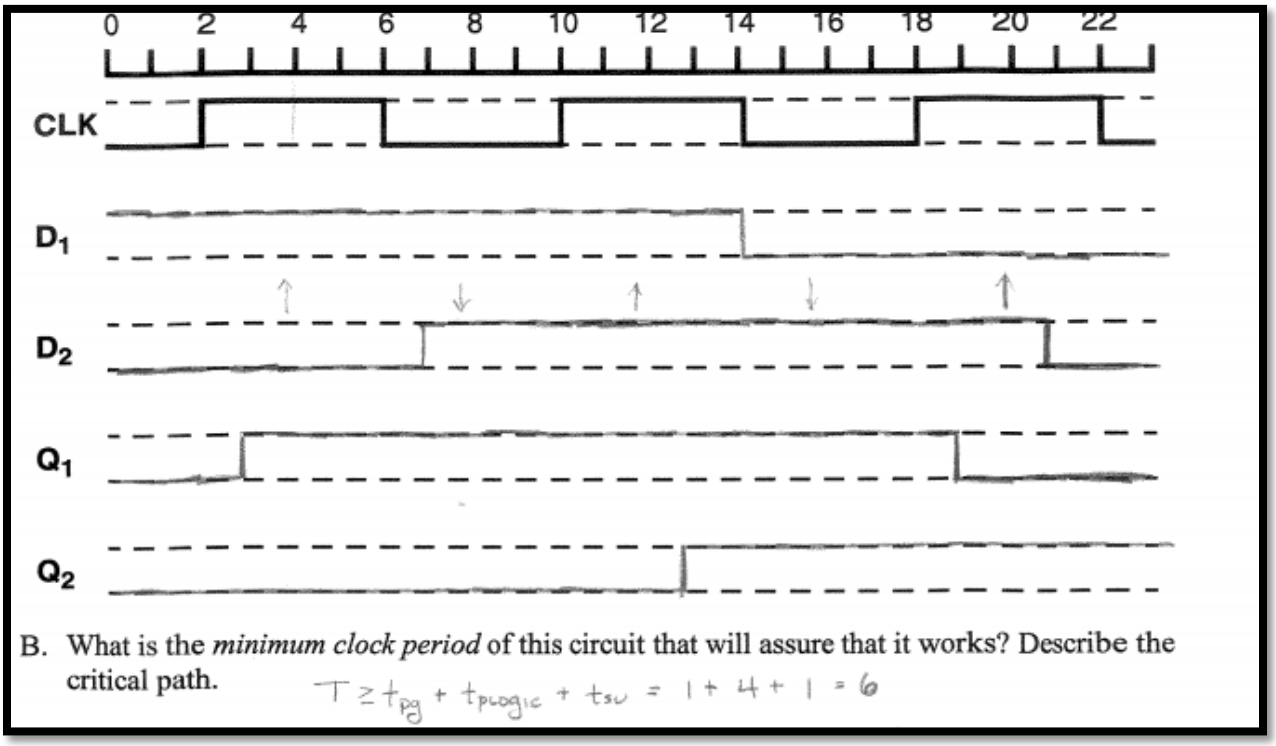
• last NOT 1 to 0 $t_p = 6.9 R_n C_n$

total = $R_n C_n (6.9^{①} + 0.69^{③} + 0.345^{②}) = \boxed{7.935 R_n C_n}$

8. The circuit shown below uses two identical rising edge triggered Flip-Flops. Assume that for both Flip-Flops, ……



A.Complete the following timing diagram for the circuit. Assume the initial states of Q1 and Q2 are 0, and have remained at 0 for a long time (but no clock edge has come along yet to latch the 1 value at D1).

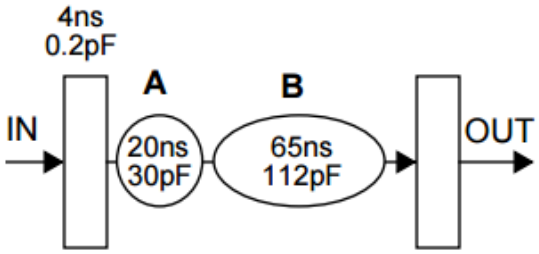


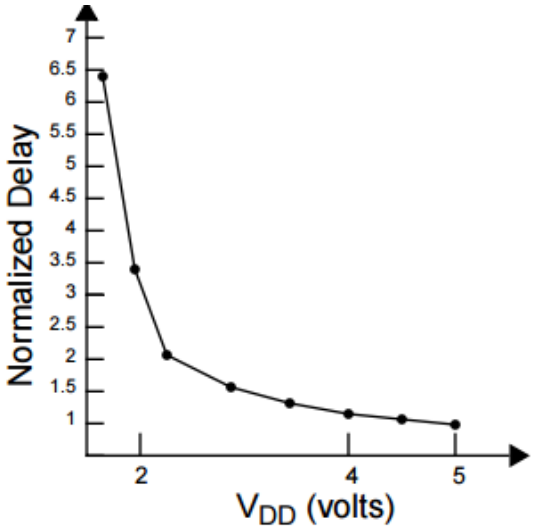
B. What is the *minimum clock period* of this circuit that will assure that it works? Describe the critical path. $T \geq t_{pg} + t_{pcogic} + t_{su} = 1 + 4 + 1 = 6$

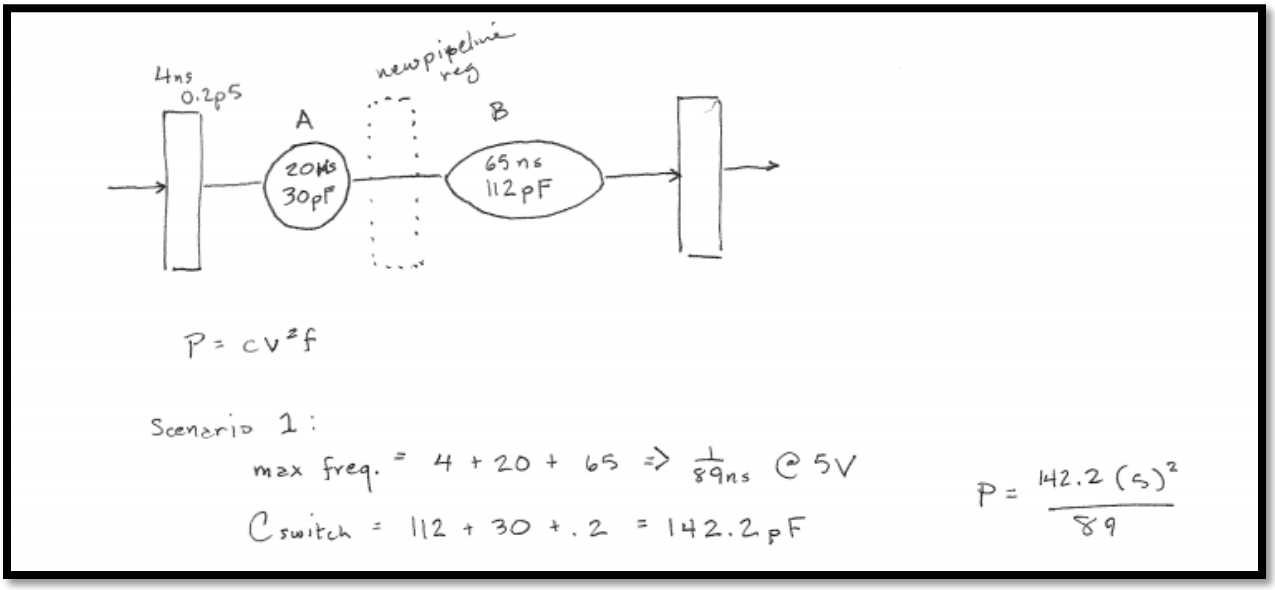
B. What is the minimum clock period of this circuit that will assure that it works? Describe the critical path.

Above

9. **Consider the circuit below, left. Modules A and B have a delay of 20nsec and 65nsec at 5V and switch 30pF and 112pF, …..**







Scenario 2:

max freq. = 4 + 65 (new pipeline reg, B) $\Rightarrow \frac{1}{69ns}$ @ 5V

but we will still be running @ $\frac{1}{89}$ ns, so voltage can change

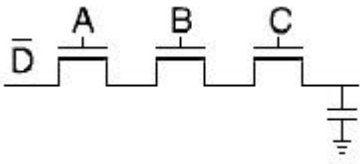
$C_{switch} = 112 + 30 + .2 + .2 = 142.4pF$

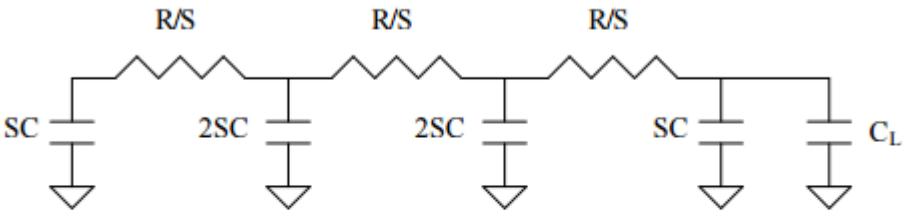
$P = \frac{142.4 (V^2)}{89}$ $\quad V \approx 5 \cdot \frac{69}{89}$

Compared: $\frac{\text{Scenario 2}}{\text{Scenario 1}} \approx \frac{24.04}{39.94} \approx 60\%$

40% power savings

10. The serial NMOS transistors in the logic section of the CPL gate shown below are clearly on the critical path. We have extracted that critical path in the figure shown below. …..





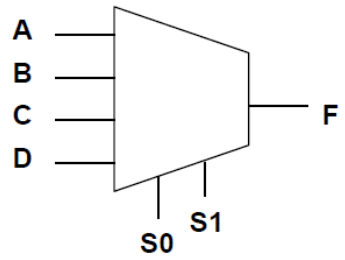
The RC network under worst case input pattern can be modeled as above.

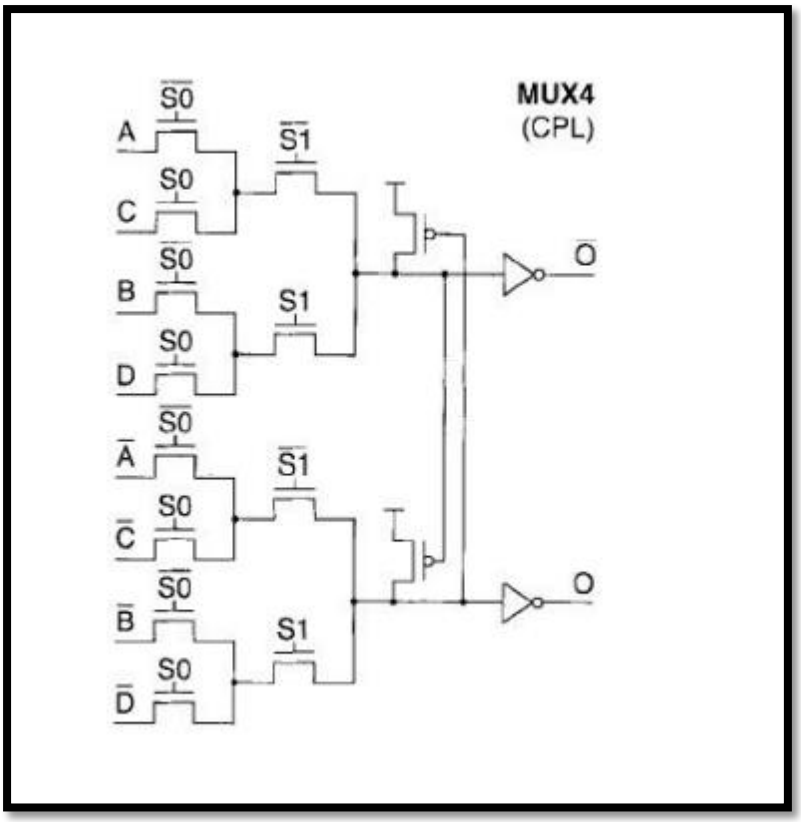
$T_p = 0.69*((R/S)*(2SC) + (2R/S)*(2SC) + (3R/S)*(SC+C_L))$
$= 0.69 * (9RC + 3RC_L/S)$

Size the transistors large to reduce delay.

11. Design a 4 input multiplexer (see the truth-table below for its fuction) in the complementary pass-transistor logic style using a minimum number of transistors.

S0	S1	Output
0	0	A
0	1	B
1	0	C
1	1	D





1) You have a carry-bypass adder with 4 bits per stage but you find that it is too slow
for large total number of bits. Being lazy to go for a different design, you pipeline the
adder. A 12-bit section of your circuit is shown in Fig. 4. Answer the questions (a)-(b)
in terms of the total number of bits, *N*, and the following one-bit delays:

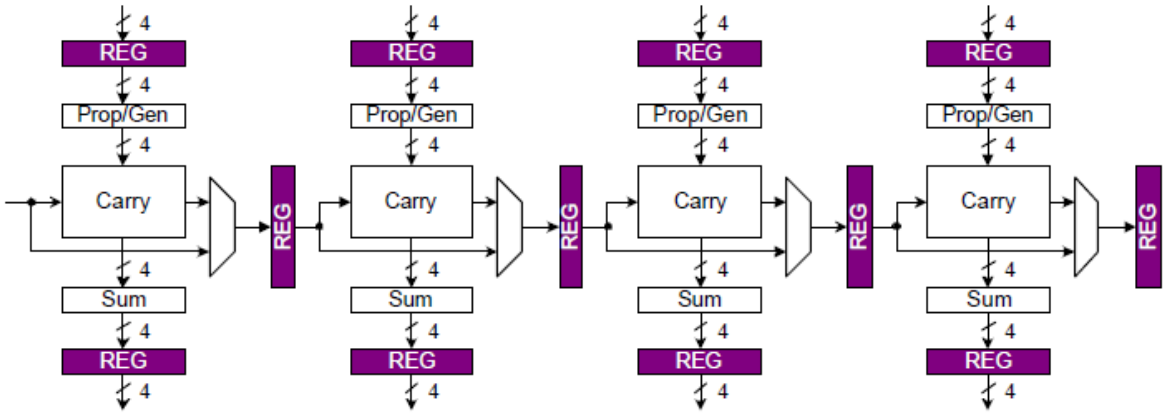
tppg delay through the propagate/generate block = 0.6ns

tpcarry delay of a single carry bit = 1ns

tpsum delay of a single sum bit = 2ns

tpmux delay of the multiplexer = 0.4ns

tpreg delay of the register = 0.5ns



a) (4 pts) What is the minimum clock period you can use for your N-bit adder? (i.e.

The worst-case scenario occurs in the first block, where input carry is not available and needs to be generated.

The worst-case carry propagation delay is:

$$tp(carry) = tp_{reg} + tp_{pg} + 4tp_{carry} + tp_{mux} = 5.5ns$$

The worst-case sum propagation delay is:

$$tp(sum) = tp_{reg} + tp_{pg} + 3tp_{carry} + tp_{sum} = 6.1ns$$

The minimum clock period is therefore:

$$T_{Clk}^{min} = \max\{tp(carry), tp(sum)\} = 6.1ns$$

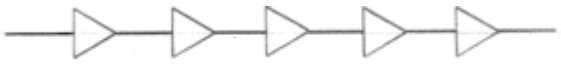
The clock period does not depend on the number of bits

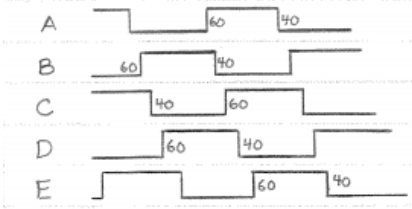
b) (3 pts) How many clock cycles does it take for the first N-bit addition to complete?

There are total of $B_{tot} = (N/4 - 1)$ blocks needed for an N-bit addition. Each block computes with inputs of the preceding blocks. Therefore, it takes $N/4 - 1$ clock cycles to complete N-bit addition.

The latency is linearly dependent on the number of bits.

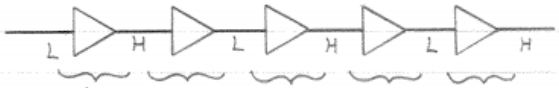
11.16 Consider a ring oscillator consisting of five inverters, each having $t_{PLH} = 60$ ns and $t_{PHL} = 40$ ns. Sketch one of the output waveforms, and specify its frequency and the percentage of the cycle during which the output is high.





$t_{PLH} = 60ns$
$t_{PHL} = 40ns$

When output is high,



60ns + 40ns + 60ns + 40ns + 60ns = 260ns

When output is low,

40ns + 60ns + 40ns + 60ns + 40ns = 240ns

Period = (240ns + 260ns) = 500ns
Frequency = 1/Period = 2MHz

% of cycle for which the output is high

$\frac{260ns}{500ns} = .52$ or 52%

11.17 A ring-of-eleven oscillator is found to oscillate at 20 MHz. Find the propagation delay of the inverter.

For 11 inverters, there are 2(11) = 22 transitions whose average length is

$$t_p = \left[\frac{1}{20\times10^6}\right]\left(\frac{1}{22}\right) = 2.27ns$$