1. **What is the logic function of the following gate?**

****



1. **Consider the following stick diagram. Draw the electrically equivalent transistor-level Schematic. What logic equation does the circuit implement?**



1. **Consider the logical expression**

out= ~( (a+b) • (c+d) )

**. Convert this to a schematic diagram for static CMOS logic, then convert it to a stick-diagram layout (as in question 1).**

1. **Provide a side-view diagram for each of the cuts X and Y through the layout below. Be sure to label each of the strata. Label your endpoints for the X cut, so it is clear which end is which.**



1. **Determine the Elmore delay from Node a to Node b in the following circuit.**



1. **What is the output function of the following circuit?**



1. **Consider the CMOS circuit shown below In the figure, the W/L ratios for each gate apply to both NMOS and PMOS transistors. We want to determine the delay from a rising transition (0 → 1) on input X to the output Z. Let us denote by τ = RnCn the product of the effective on-resistance and gate capacitance of the minimum-sized NMOS transistor, i.e. (W/L)n = 1/1. For the minimum-sized PMOS transistor, we have Rp = 2Rn . Also, the output Z drive load is CL = 10Cn .**

**A. Assuming that the rise and fall times are good approximations of the propagation delay, determine the delay from X to Z, in terms of τ, when Y = 0.**

**B. Now, assume that Y = 1. What is the new value for the propagation delay from X to Z? Can you comment on this?**



1. **The circuit shown below uses two identical rising edge triggered Flip-Flops. Assume that for both Flip-Flops, the setup time is one time unit, the propagation delay is one time unit, and the hold time is two time units. The gates, buffers and inverters in this circuit are annotated with their propagation delays in the same time units. Assume that maximum and minimum propagation delay for these gates are equivalent..**



1. **Complete the following timing diagram for the circuit. Assume the initial states of Q1 and Q2 are 0, and have remained at 0 for a long time (but no clock edge has come along yet to latch the 1 value at D1).**





* **What is the minimum clock period of this circuit that will assure that it works? Describe the critical path.**
1. **Consider the circuit below, left. Modules A and B have a delay of 20nsec and 65nsec at 5V and switch 30pF and 112pF, respectively. Each register has a delay of 4nsec and switches 0.2pF. Adding a pipeline register between A and B allows for reduction of the supply voltage while maintaining the throughput. How much power can be saved this way? (Delay with respect to VDD can be approximated from the plot on the right.)Hint :P=CFV^2**



1. **The serial NMOS transistors in the logic section of the CPL gate shown below are clearly on the critical path. We have extracted that critical path in the figure shown below. We want to investigate sizing of these transistors so that the delay is minimized. You may assume that a minimum sized NMOS transistor has an on-resistance equal to R. In addition, the only parasitic capacitances that you should consider are Cgs = Cgd = C (again for a minimum sized transistor). Finally, we decided all three transistors should remain of the same size S during the sizing. Derive an expression for the propagation delay of this**

**critical path as a function of R, C, the load capacitance CL and S. Determine qualitatively how you would size the devices to make the propagation delay minimum**.

****

****

1. **Design a 4 input multiplexer (see the truth-table below for its fuction) in the complementary pass-transistor logic style using a minimum number of transistors.**



1. You have a carry-bypass adder with 4 bits per stage but you find that it is too slow

for large total number of bits. Being lazy to go for a different design, you pipeline the

adder. A 12-bit section of your circuit is shown in Fig. 4. Answer the questions (a)-(b)

in terms of the total number of bits, *N*, and the following one-bit delays:

tppg delay through the propagate/generate block = 0.6ns

tpcarry delay of a single carry bit = 1ns

tpsum delay of a single sum bit = 2ns

tpmux delay of the multiplexer = 0.4ns

tpreg delay of the register = 0.5ns



**a) (4 pts)** What is the minimum clock period you can use for your N-bit adder? (i.e.

throughput time). Give your reasoning for full credit. Is the clock period dependent on

the total number of bits, N?

**The worst-case scenario occurs in the first block, where input carry is not**

**available and needs to be generated.**

**The worst-case carry propagation delay is:**

**tp(carry) = tpreg + tppg + 4tpcarry + tpmux = 5.5ns**

**The worst-case sum propagation delay is:**

**tp(sum) = tpreg + tppg + 3tpcarry + tpsum = 6.1ns**

**The minimum clock period is therefore:**

**TClk**

**min = max {tp(carry), tp(sum)} = 6.1ns**

**The clock period does not depend on the number of bits**



**b) (3 pts)** How many clock cycles does it take for the first N-bit addition to complete?

(i.e. latency) Is the latency linearly dependent on the number of bits?

**There are total of Btot = (N/4 – 1) blocks needed for an N-bit addition. Each**

**block computes with inputs of the preceding blocks. Therefore, it takes N/4 – 1**

**clock cycles to complete N-bit addition.**

**The latency is linearly dependent on the number of bits.**













