Faculty of Engineering and Technology

Department of Electrical and Computer Engineering

DIGITAL INTEGRATED CIRCUITS

Homework - 1

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Section: 3

Date: 7 April 2022

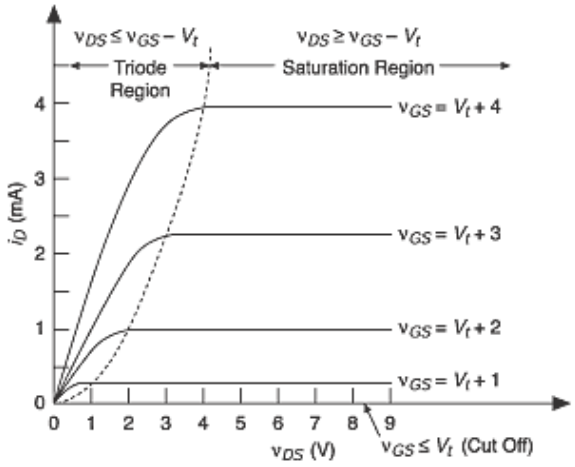
1. **Define CMOS?**

   The term CMOS (short for complementary metal-oxide-semiconductor) refers to the small amount of memory on a computer motherboard that holds the BIOS settings. The system time and date, as well as hardware settings, are among the BIOS options.

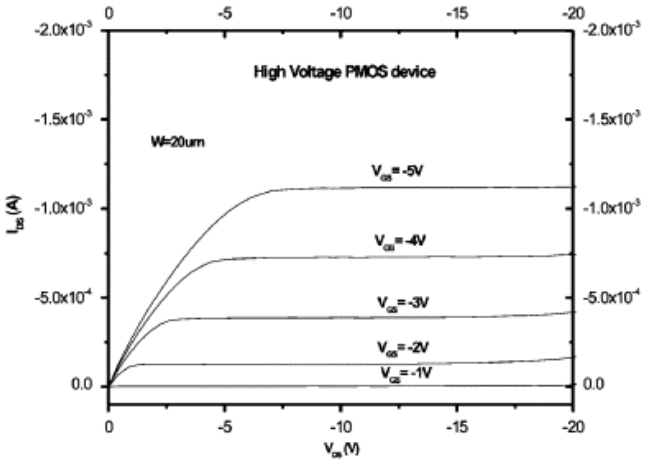
2. **What are the two types of transistors? How do they work, show operation region of each device?**

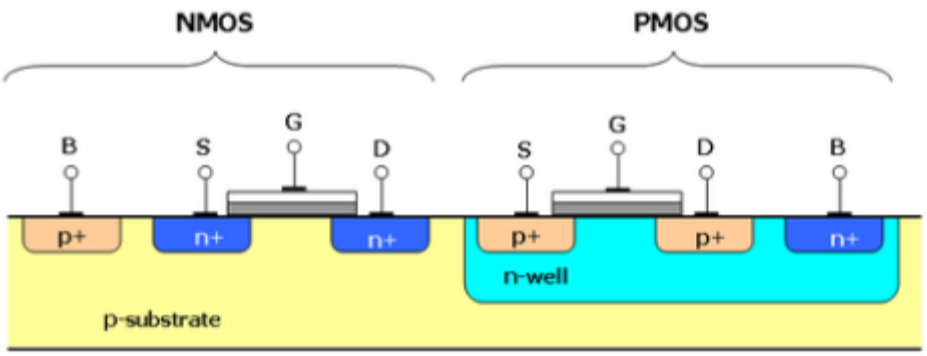
   P channel and N channel semiconductor devices are also known as PMOS and NMOS. NMOS is laid on a p-type substrate, and the majority of the carriers are electrons, whereas PMOS is laid on an N-type substrate, and the majority of the carriers are holes. NMOS is faster than PMOS, but it is not as noise resistant. PMOS has the same working region as NMOS, but with a negative VGS.

- working Region of NMOS ➔



- working Region of PMOS ➔





- When a voltage is applied to the gate, the NMOS operates as follows:
  - Vgs < Vt OFF
  - Vds < Vgs -Vt LINEAR
  - Vds > Vgs – Vt SATURATION

- When a voltage is applied to the gate, the PMOS operates as follows:
  - Vsg < |Vt| OFF
  - Vsd < Vsg – |Vt| LINEAR
  - Vsd > Vsg – |Vt| SATURATION

3. **<u>What is the main IC parasitic?</u>**
   - Inductance
   - Capacitance
   - Resistance
   - Transistors (Bipolar).
   - Diodes.

4. **<u>Explain What do we mean by process node? And how does that affect IC characteristics</u>**

Distinct generations and topologies of circuits are generally associated with different nodes. The smaller the technology node, the smaller the feature size, resulting in tiny transistors that are speedier and more energy efficient. The term "process node" used to refer to a variety of various characteristics of a transistor, including the gate length and M1 half-pitch.

The technology utilized in this device is determined by the process node, which is a standardized procedure used across a wide range of items. The process for many products makes yield and process improvement considerably easier, because instead of having a distinct team for each tiny product group, the same resources can address complicated problems requiring multiple phases for many products at the same time.

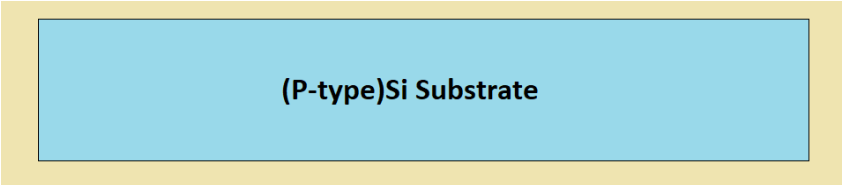
When a result, the process node has an impact on IC characteristics. For example, as L increases, more electrons or holes are required to connect the channel between drain and source. As a result, the process node affects Vt, which in turn affects the other values.

It also has an impact on the cost of IC, as it is determined by the technology utilized in IC.

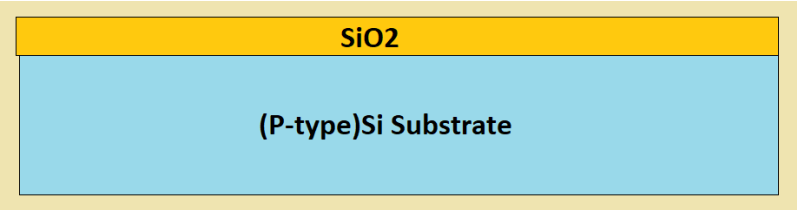
Also, when technology allows the channel to be linked quickly, the IC becomes faster. It also has an impact on the power and timing.

5. **What are the basic steps for CMOS IC fabrication?**

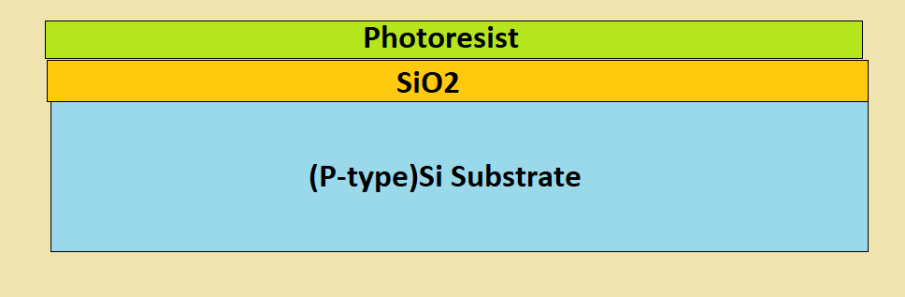
Step1: Substrate ➔ Primarily, start the process with a P-substrate



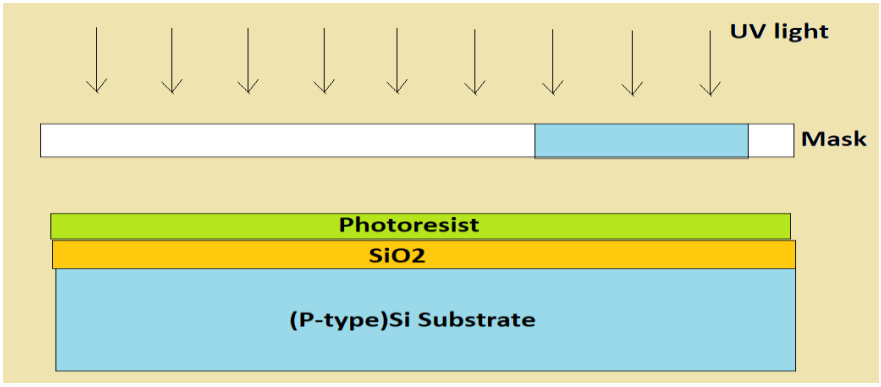
Step2: Oxidation ➔ The oxidation process is done by using high-purity oxygen and hydrogen, which are exposed in an oxidation furnace approximately at 1000 degree centigrade.



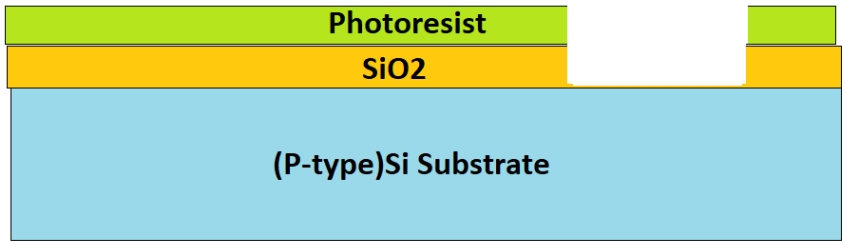
Step3: Photoresist ➔ A light-sensitive polymer that softens whenever exposed to light is called as Photoresist layer. It is formed.



Step4: Masking ➔ To protect other parts of wafers when working on specific place or area of the wafer

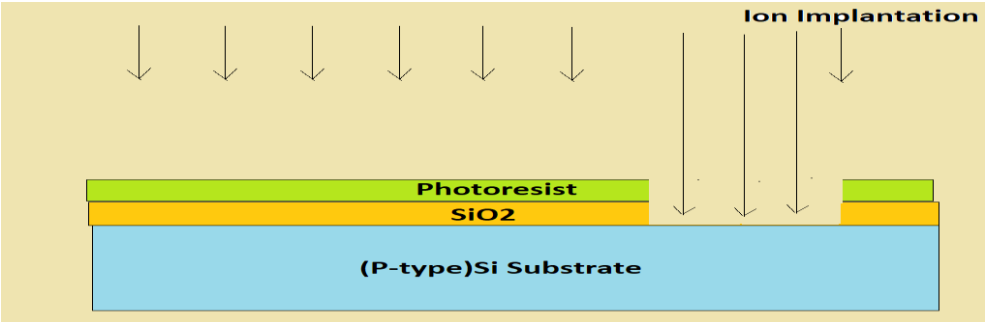


Step5 : **Etching** ➔ It removes material selectively from the surface of wafer to create patterns. The pattern is defined by etching mask. The parts of material are protected by this etching mask.

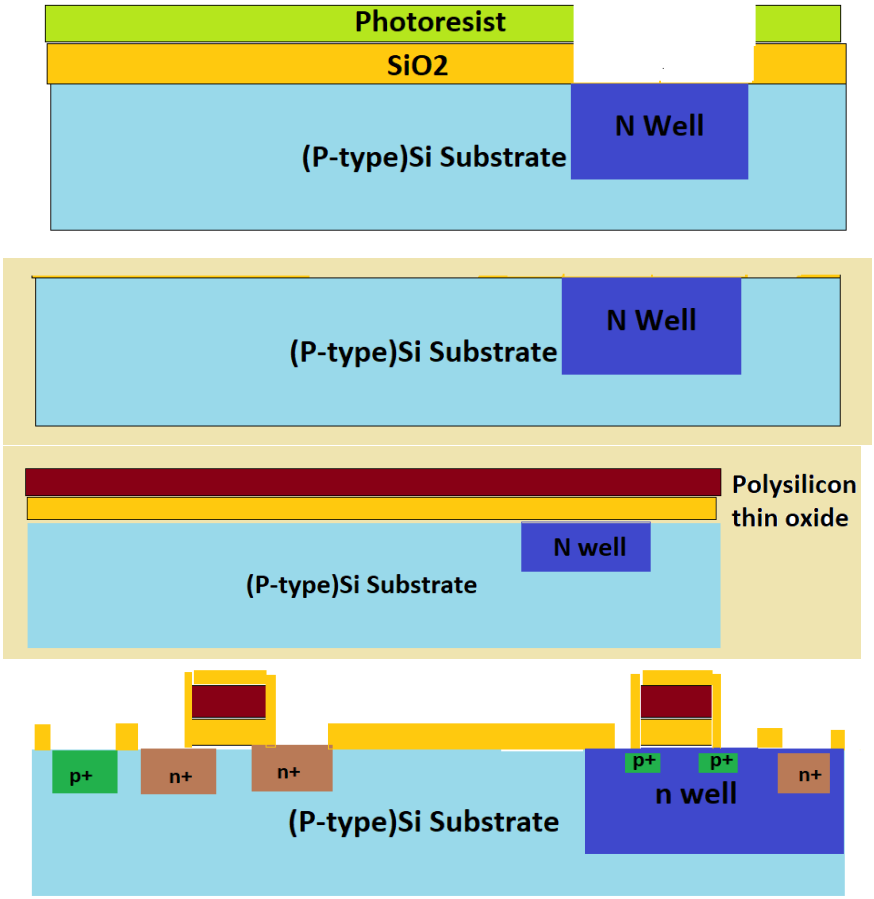


Step6: Doping➔

- To alter the electrical character of silicon, atom with one less electron than silicon such as boron and atom with one electron greater then silicon such as phosphorous are introduced into the area.
- Atomic diffusion
  In this method p and n regions are created by adding dopants into the wafer. The wafers are placed in an oven which is made up of quartz and it is surrounded with heating elements.
- Ion implantation: This is also a method used for adding dopants. In this method, dopant gas such as phosphine or boron trichloride will be ionized first. Then it provides a beam of high energy dopant ions to the specified regions of wafer

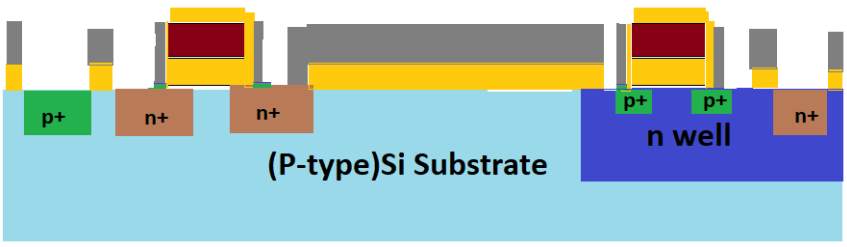


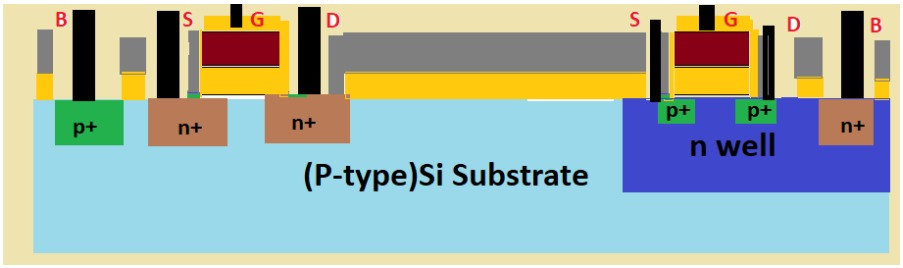
Formation of the N-well :By using ion implantation or diffusion process N-well is formed.



Step7 : **Metallization ➔**

- It is used to create contact with silicon and to make interconnections on chip. A thin layer of aluminium is deposited over the whole wafer. Aluminium is selected because it is a good conductor, has good mechanical bond with silicon, forms low resistance contact and it can be applied and patterned with single deposition and etching process.
- Assembly and packaging
  Each of the wafers contains hundreds of chips. These chips are separated and packaged by a method called scribing and cleaving. The wafer is similar to a piece of glass.





6. Derive the current equation for both the NMOS and PMOS in the linear region

⇨ For an NMOS: $V_{GS} \geq V_{th}$

$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

$V_{DS} < V_{GS} - V_{th}$

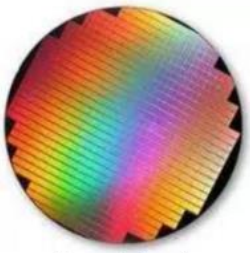
→ For an PMOS:

$$v_{GS} < V_T \qquad v_{DS} > v_{GS} - V_T \qquad i_D = K[2(v_{GS} - V_T)v_{DS} - v_{DS}^2]$$

7. Answer the following questions:

1. What is the difference between Wafer, Die and Package?

A wafer is a thin disc spun from a silicon crystal. A die is an individual circuit that is printed or chemically etched on a section of that wafer. A chip consists of an individual die cut from the wafer plus related circuitry (cache, memory controller, etc.). The chip can be mounted on a printed circuit board via wire bonding or solder balls. This is called a chip package



A complete wafer

2. **IC Component Types**
   - Input/Output (I/O) Cells: Implement the connection between IC inner circuitry and PCB.
   - Digital Standard Cells: Basic cells performing functions used as building blocks for large digital circuits.
   - Intellectual Property (IP) Blocks: Large blocks performing completed functions used in large designs.
   - Digital ICs: Large ICs (e.g. processor, GPU, etc.), distributed to end-users.

3. **What do we mean by Doping the Semiconductor? What is the difference between Ntype and Ptype materials?**

   A manufacturing procedure for increasing the conductivity of a pure semiconductor material by adding free charge carriers (free electrons or holes). There are two types: Ntype and Ptype. Ntype is achieved by adding (to silicon) a phosphorus atom with five valence electrons; this atom establishes covalent bonds with four nearby silicon atoms, while the fifth becomes a conduction electron because it is unattached. Unlike the Ntype, the Ptype creates a hole by adding an element with three valence electrons, such as boron or gallium. Unlike Ptype, electrons make up the majority of carriers in Ntype, whereas holes make up the minority.

4. **Explain how do we generate a depletion layer and how does that affect the capacitance?**

   When a positive voltage now is applied to the gate in Ntype, which is done by introducing positive charge Q to the gate, then some positively charged holes in the semiconductor nearest the gate are repelled by the positive charge on the gate, and exit the device through the bottom contact. They leave behind a depleted region that is insulating because no mobile holes remain; only the immobile, negatively charged acceptor impurities. The greater the positive charge placed on the gate, the more positive the applied gate voltage, and the more holes that leave the semiconductor surface, enlarging the depletion region. (In this device there is a limit to how wide the depletion width may become. It is set by the onset of an inversion layer of carriers in a thin layer, or channel, near the surface.