Faculty of Engineering and Technology

Department of Electrical and Computer Engineering

DIGITAL INTEGRATED CIRCUITS

Homework - 2

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Section: 3

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1. When is the channel said to be pinched –off?

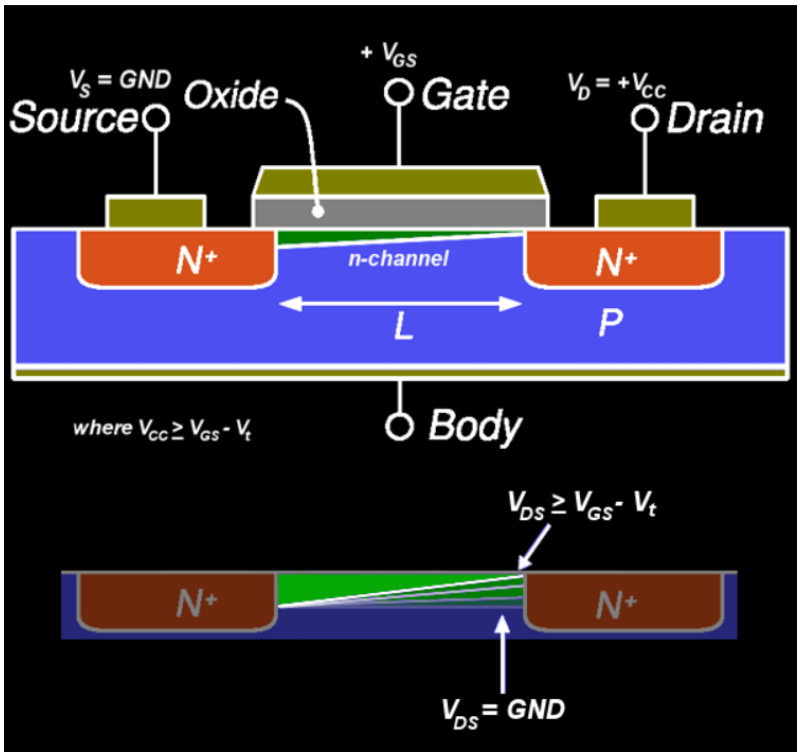
When the effective gate-to-channel voltage at the drain end becomes less than the threshold voltage and hence incomplete to maintain a layer of minority carriers across it, the channel of an enhancement-type MOSFET is said to be pinched off (needed for the channel to exist). As a result, near the drain end, the channel's effective width tends to zero.

Assume that V_{DS} is the applied drain-to-source voltage and V_{GS} is the applied gate-to-source voltage, with the source set to zero potential.

So, basically, the effective gate to channel voltage near the drain = $V_{GS} - V_{DS}$

At saturation condition, we have, $V_{DS} > V_{GS} - V_T$
So, the effective gate to channel voltage near the drain terminal < V_T

This basically implies that the channel is not formed near the drain, causing pinch-off



2. What is pull down device?

Pull the voltage down to more negative values. Because the Source pin on an NMOS part must be connected at a low level, the Drain pin can only "pull down" to the same low level when the part is turned on.

3. What is pull up device?

Pull the voltage up towards more positive values, for a PMOS part the Source pin must be connected at the high level, so when turned on the Drain pin can only "pull up" to that same high level.

4. Why NMOS technology is preferred more than PMOS technology?

Because n-channel MOSFET offer a lower Rdson*cost metric, they are favored over PMOS. This means that an n-channel device can provide the same Rdson for a lower price, and everyone wants to save money.

The manufacturing expenses of a PMOS wafer are nearly identical to those of a NMOS wafer. However, due to the poorer mobility of P-type silicon, PMOS requires a significantly larger die for the same Rdson as NMOS, as others have stated. Die per wafer will be lower and die cost (wafer cost/die per wafer) for a PMOS device of the same Rdson will be higher because the required die is larger.

5. What is Channel-length modulation?

Is an effect in field effect transistors, a shortening of the length of the inverted channel region with increase in drain bias for large drain biases, The result of CLM is an increase in current with drain bias and a reduction of output resistance. It is one of several short-channel effects in MOSFET scaling. It also causes distortion in JFET amplifiers.

6. Define Rise time

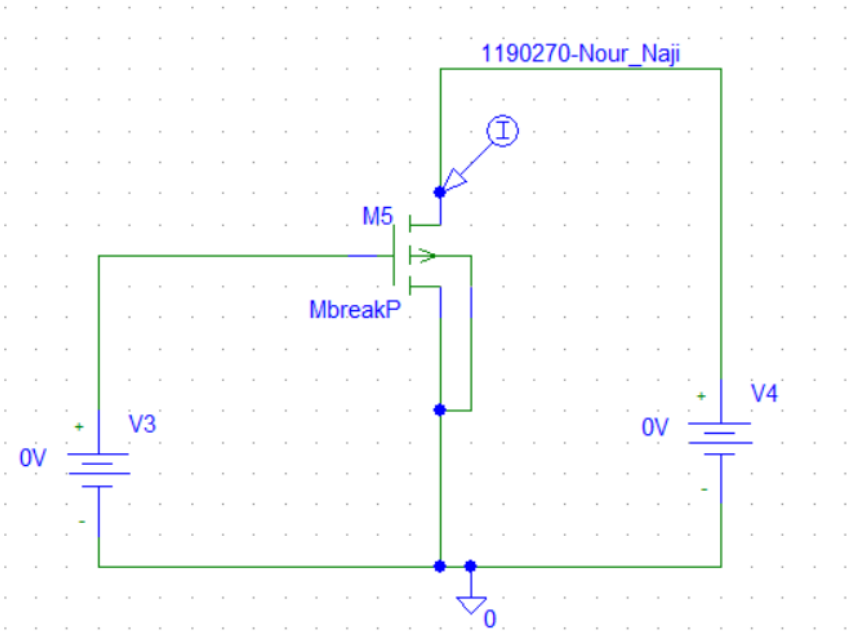
Rise time, tr is the time taken for a waveform to rise from 10% to 90% of its steady-state value.

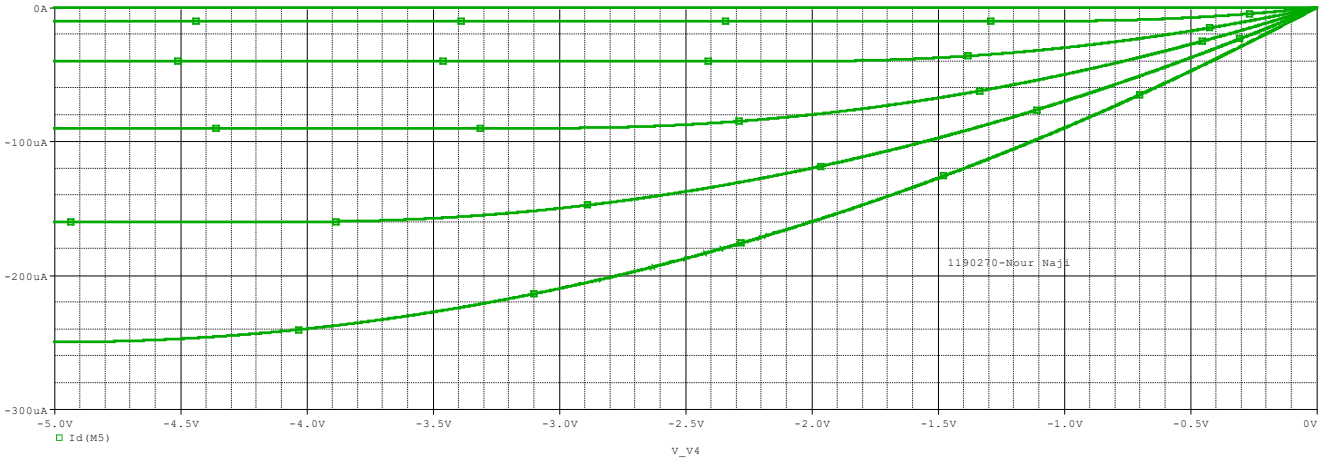
7. Define Fall time

Fall time, τf is the time taken for a waveform to fall from 90% to 10% of its steady-state value.

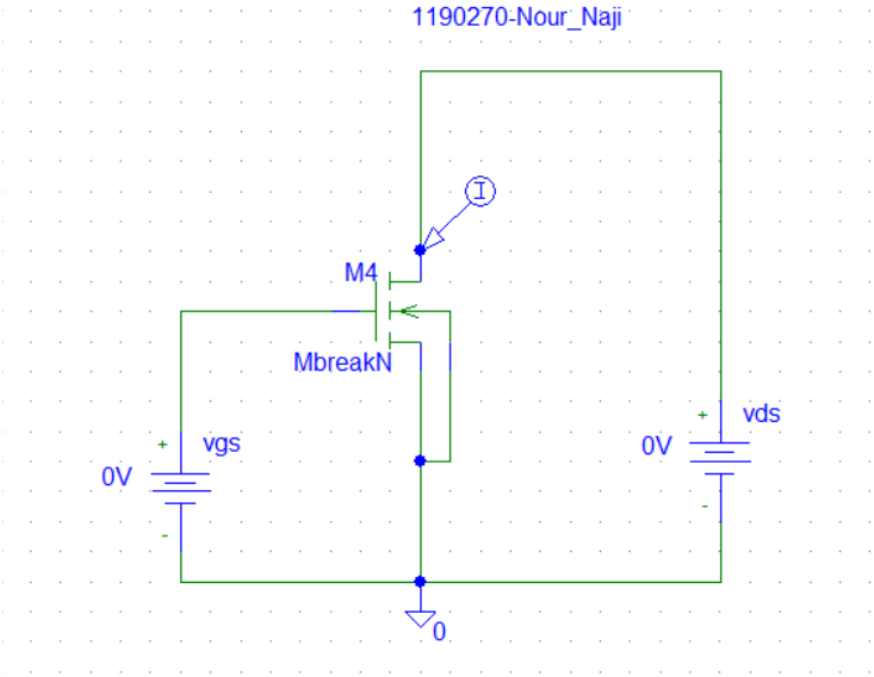
8. Using any spies tool (HSPICE, PSPICE …and any process node) simulate the following as explained in class AND SUBMIT THE SCHEMATIC AND WAVE FORS AS SNAPSHOT

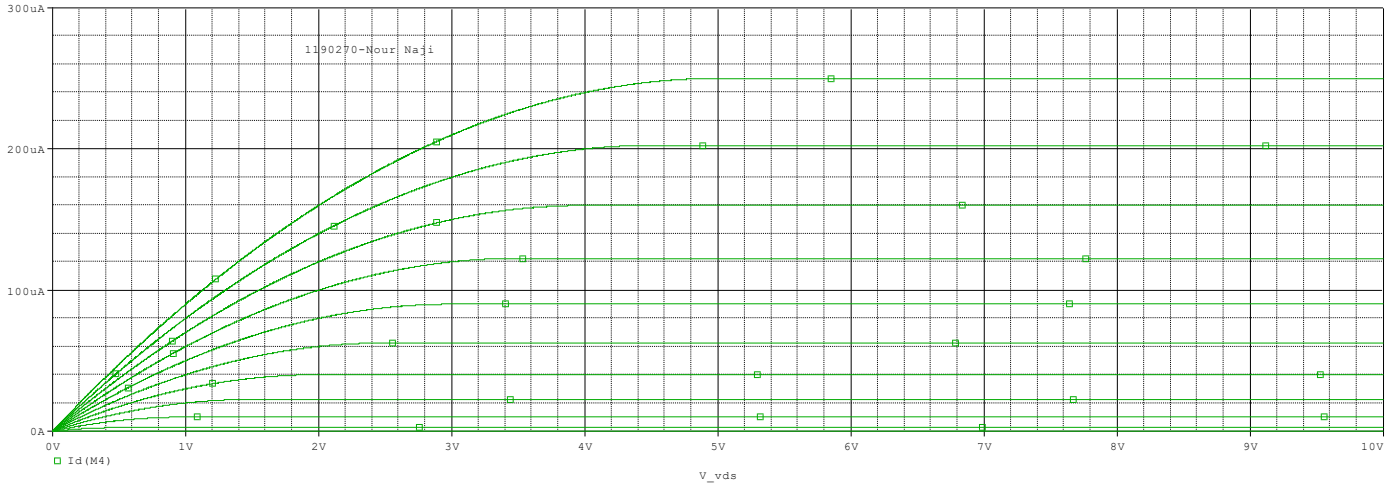
1- PMOS Device and show waveform for current and voltage (IV curve)



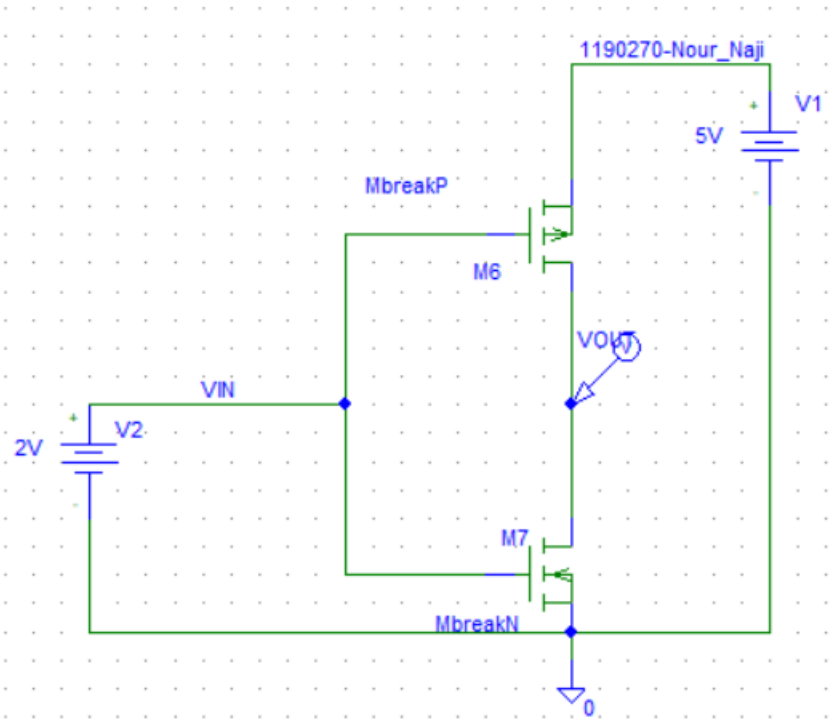


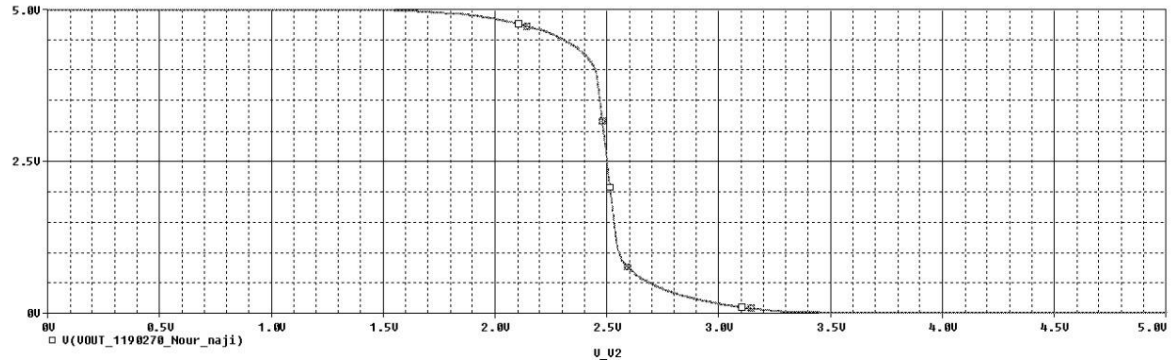
2- NMOS Device and show waveform for current and voltage (IV curve)



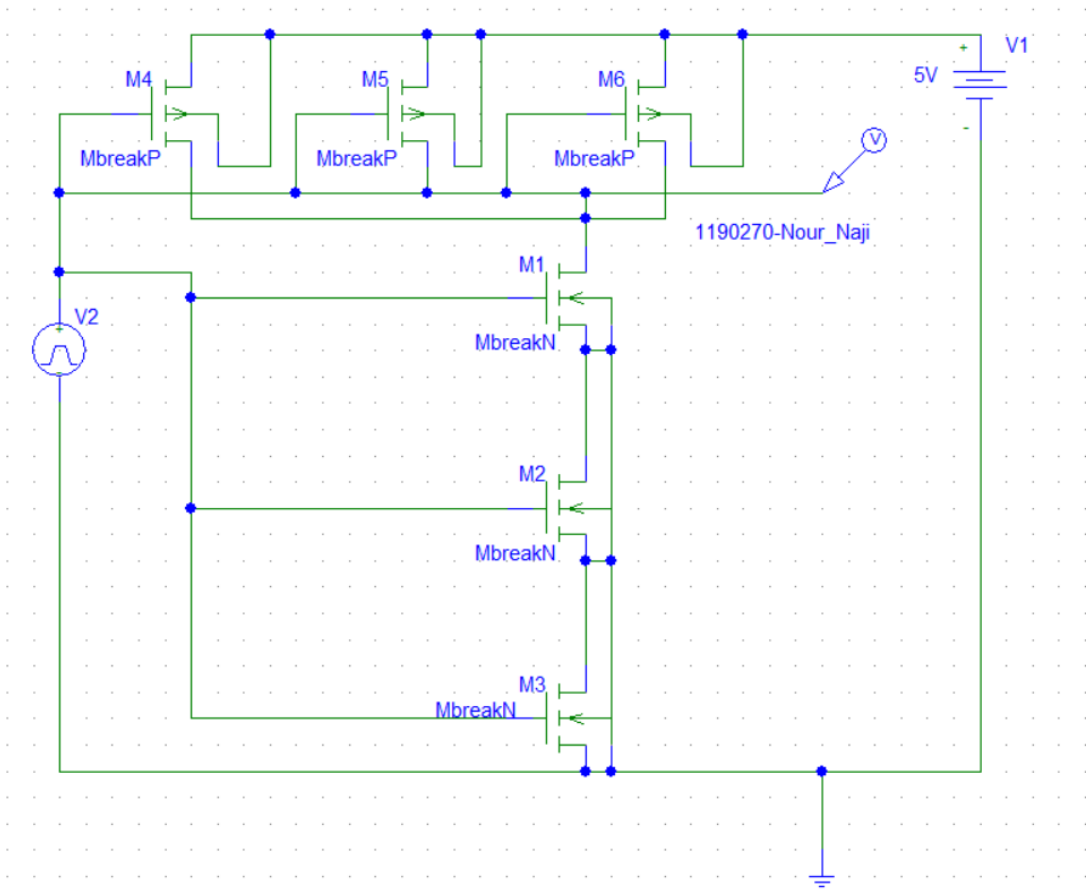


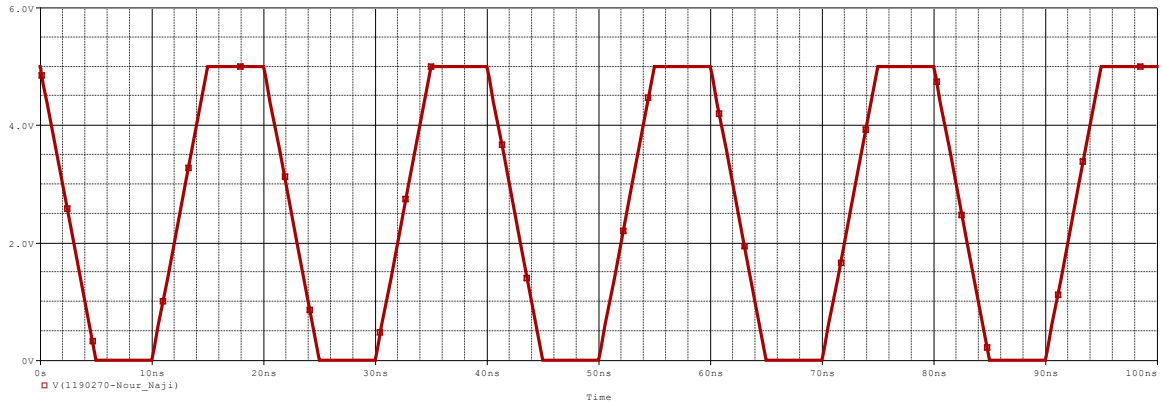
3- Inverter: size the inverter correctly to have equal rise and fall time



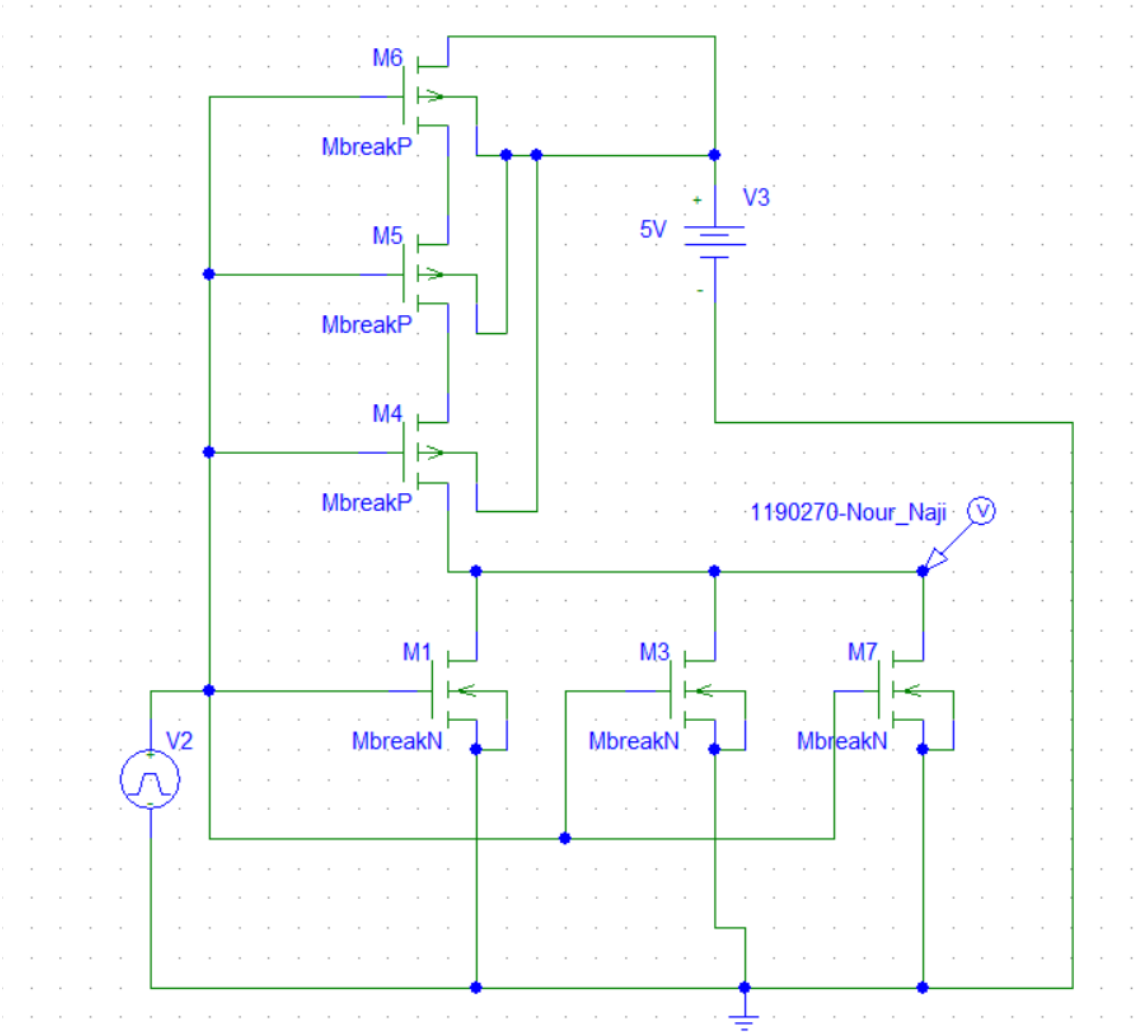


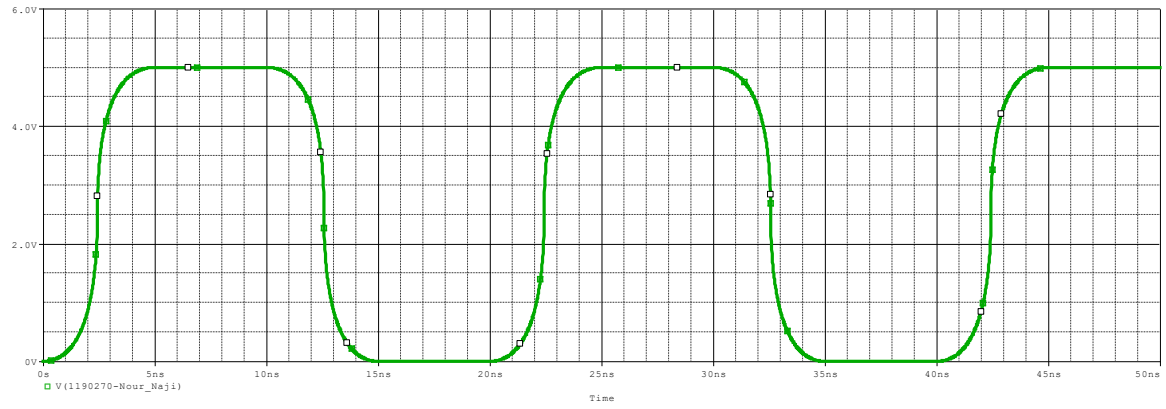
4. 3 INPUT NAND : size the inverter correctly to have equal rise and fall





5. 3 INPUT NOR : size the inverter correctly to have equal rise and fall time





6. Generate spice netlist for 3 INPUT NOR