Faculty of Engineering and Technology

Department of Electrical and Computer Engineering

DIGITAL INTEGRATED CIRCUITS

Homework - 3

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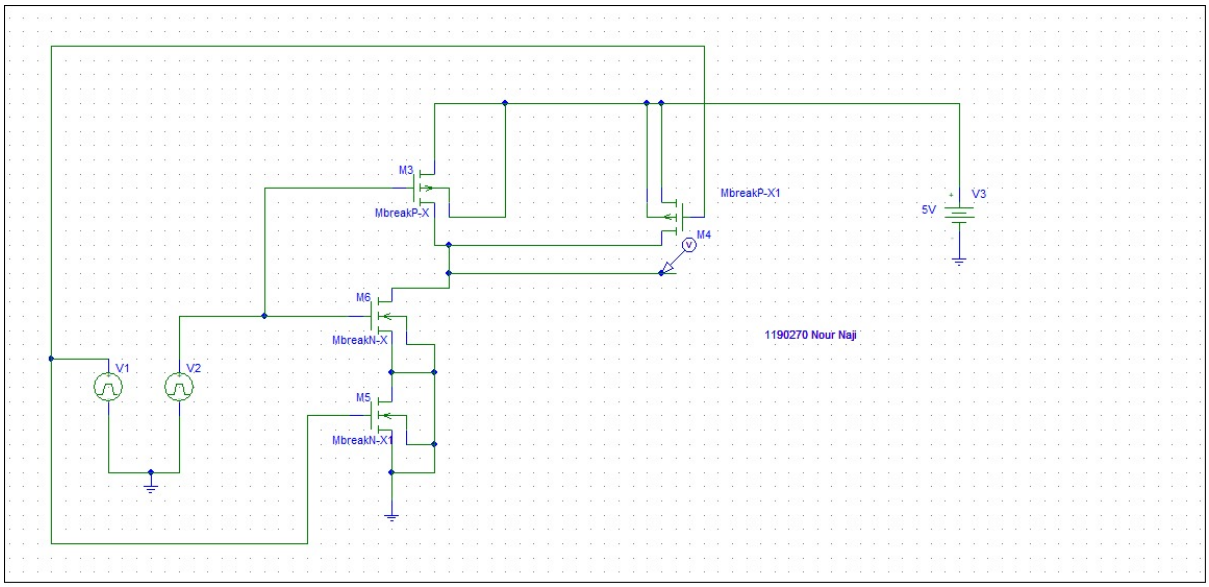
Section: 3

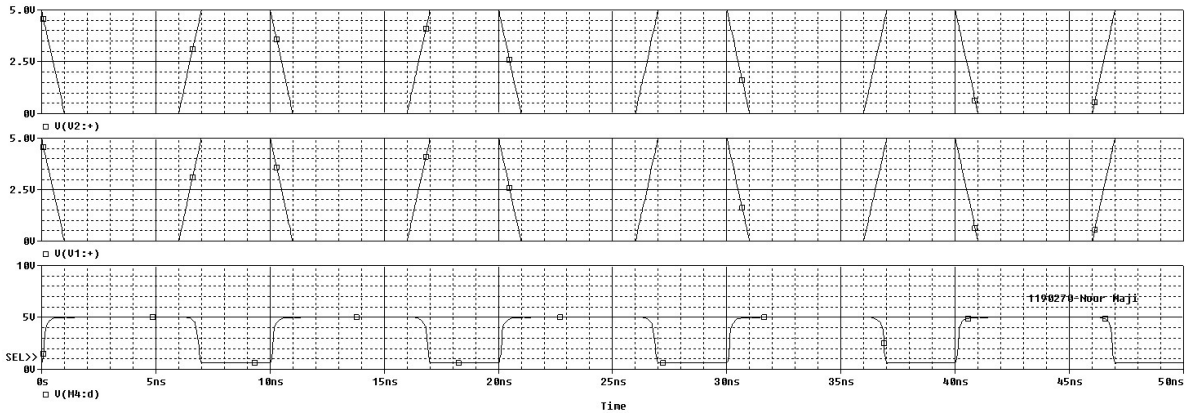
Date: 8/6/2022

Layout design of a CMOS Circuits
Part 1:

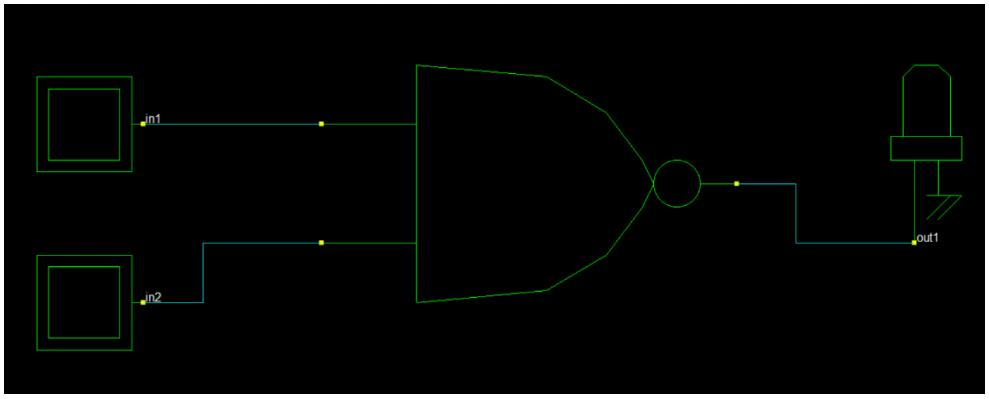
- **NAND gate in PSpise**

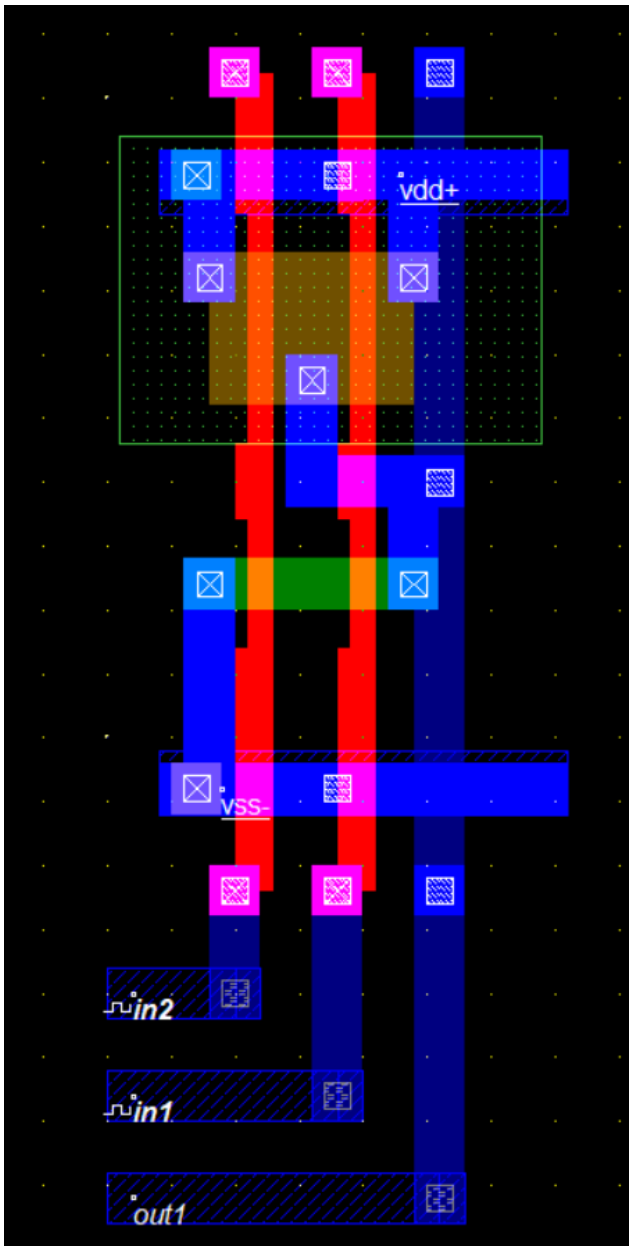


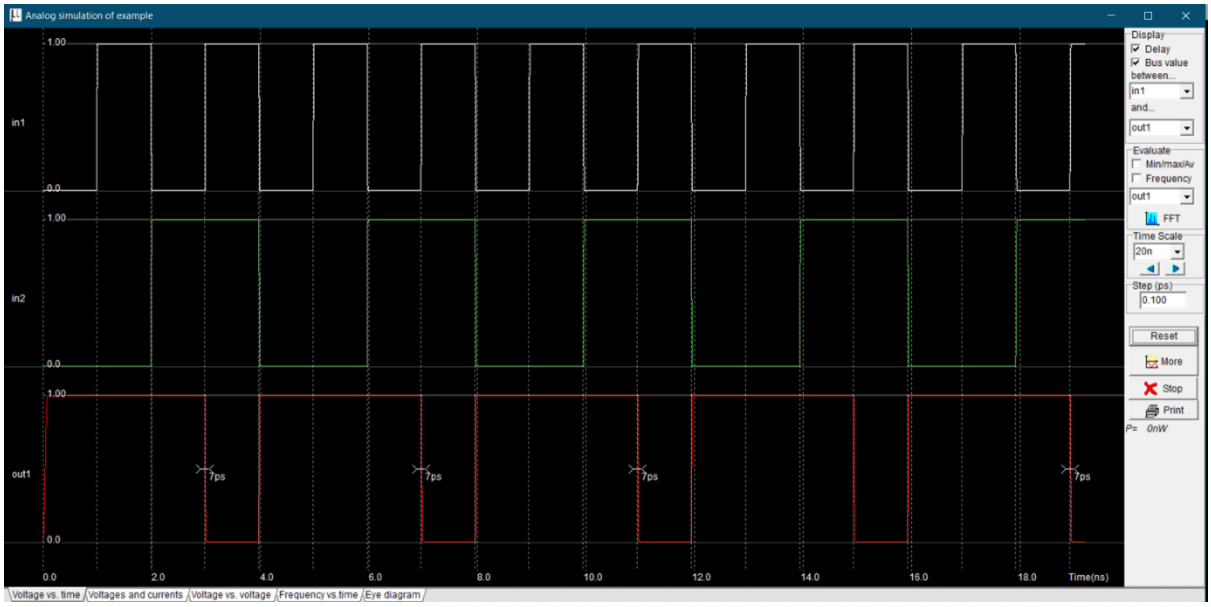
→ **Simulation:**



- **NAND gate and Layout:**







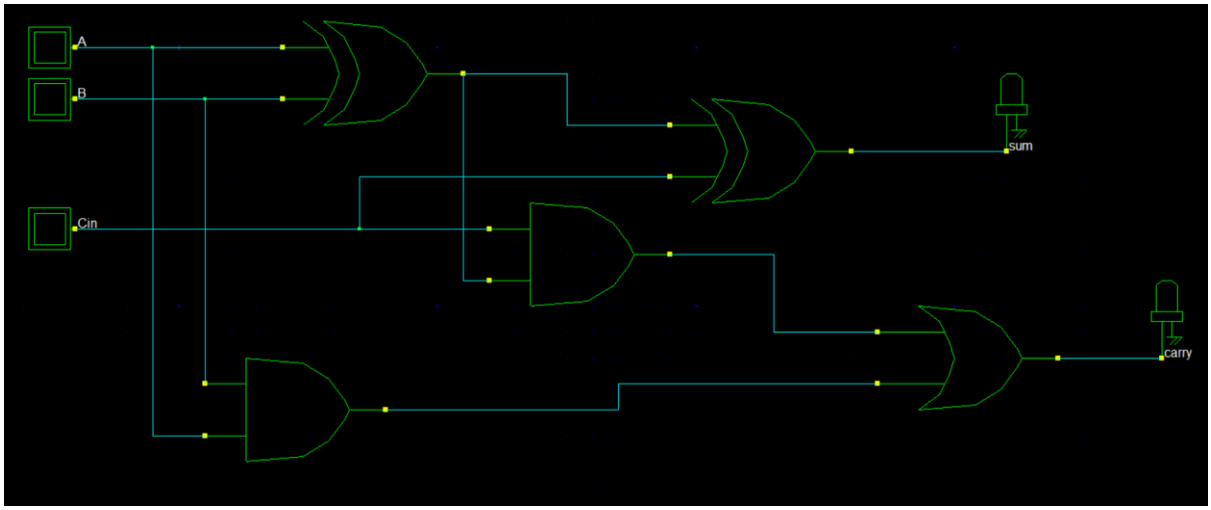
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

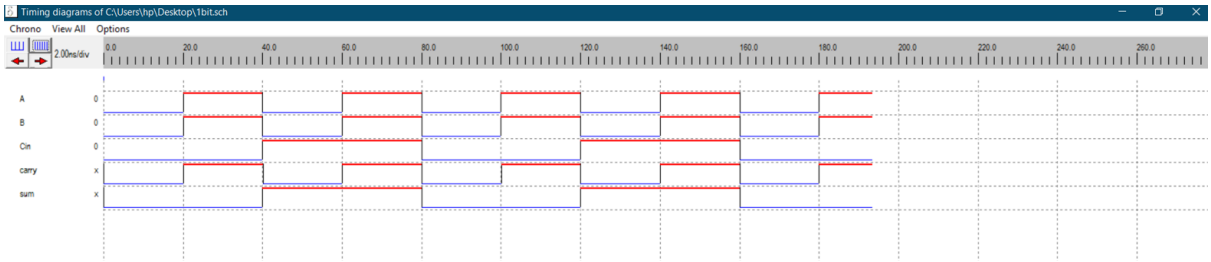
Part 2:

Two Bit Full Adders are the Logical Circuits that have two inputs for the input bits and one for the carry and as a result, Sum of the bits along with the carry are obtained at sum and carry Terminals respectively.

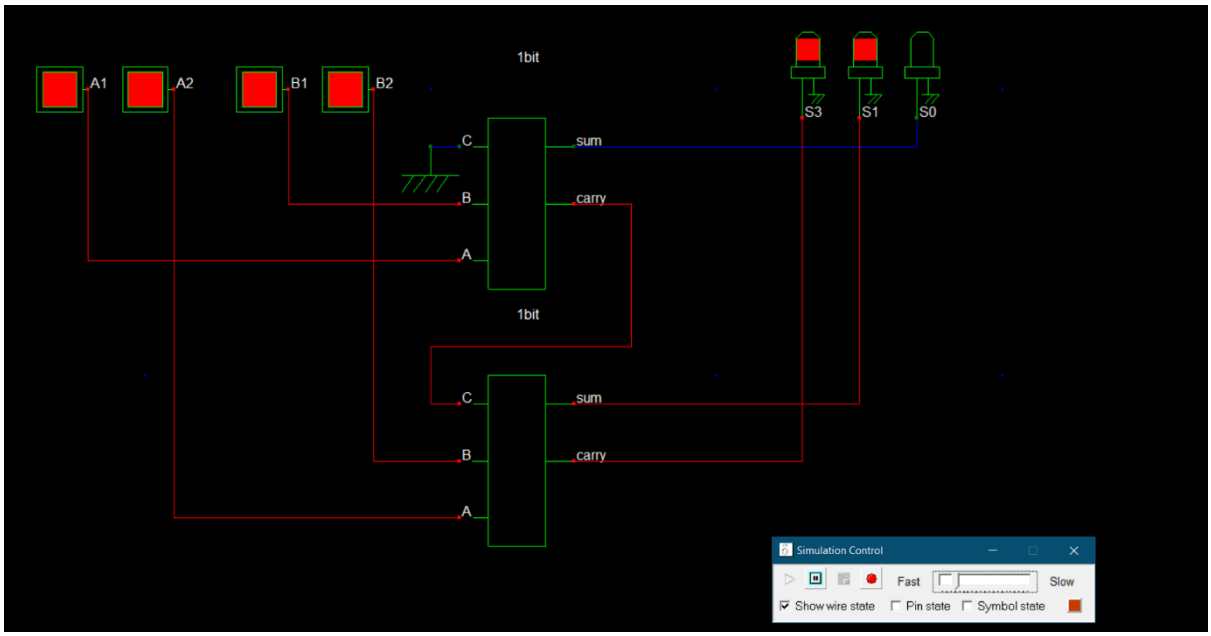
Let us consider first one-bit full-adder adds three one-bit numbers, often written as A, B, and Cin; A and B are the operands, and Cin is a bit carried in from the previous less-significant stage.

- 0+0+0 =0, 0 carry output
- 0+1+0 =1, 0 carry output
- 1+0+0 =1, 0 carry output
- 1+1+0 =0, 1 carry output
- 0+0+1 =1, 0 carry output
- 0+1+1 =0, 1 carry output
- 1+0+1 =0, 1 carry output
- 1+1+1 =1, 1 carry output





If you cascade 2 binary full adder blocks you will get a 2-bit full adder. The general block diagram is as below.



the truth table :

A0	B0	A1	B1	S3	S1	S0
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	0	0	1
0	0	1	1	0	1	1
0	1	0	0	0	1	0
0	1	0	1	1	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	0	1	1
1	1	0	1	1	0	1
1	1	1	0	1	0	0
1	1	1	1	1	1	0

;module example(B2,A2,A1,B1,S0,S1,S3)

;input B2,A2,A1,B1

;output S0,S1,S3

;wire w4,w10,w11,w12,w13,w14,w15

;xor xor2_1_1(w10,A1,B1)

;xor xor2_2_2(S0,w10,vss)

;and and2_3_3(w11,w10,vss)

;and and2_4_4(w12,A1,B1)

;or or2_5_5(w4,w11,w12)

;xor xor2_1_6(w13,A2,B2)

;xor xor2_2_7(S1,w13,w4)

;and and2_3_8(w14,w13,w4)

;and and2_4_9(w15,A2,B2)

;or or2_5_10(S3,w14,w15)

endmodule

Simulation parameters in Verilog Format //

always

;B2=~B2 #200

;A2=~A2 #400

;A1=~A1 #800

;B1=~B1 #1600

Simulation parameters //

B2 CLK 1 1 //

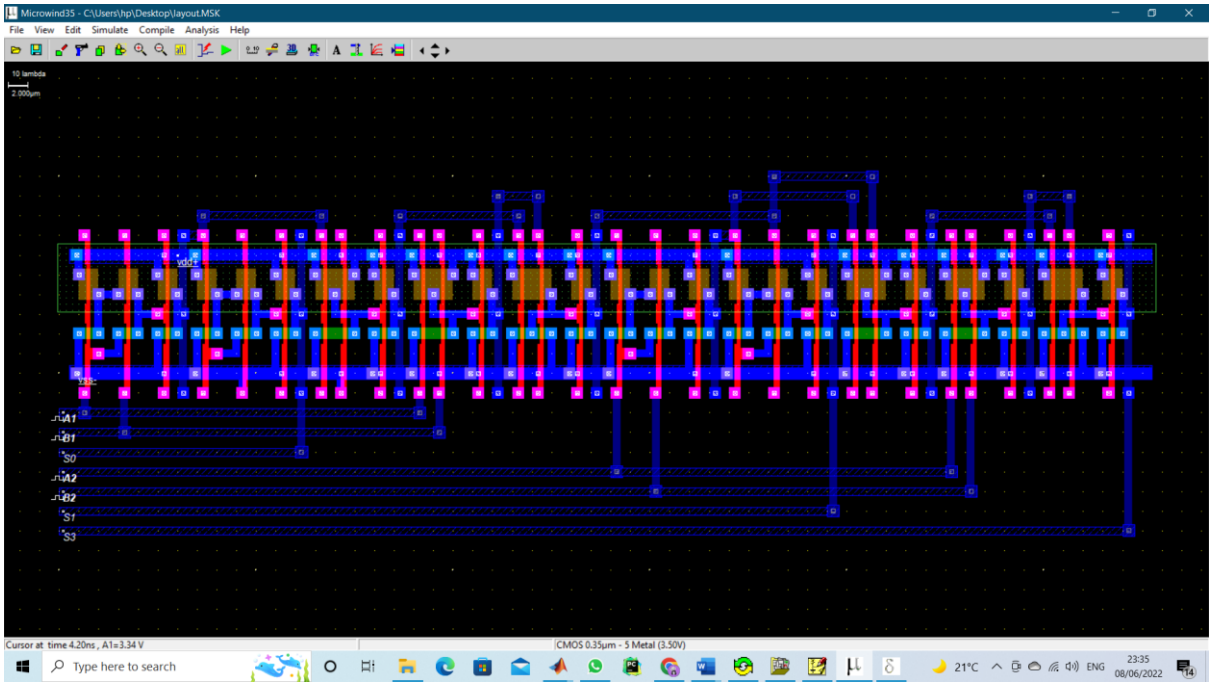
A2 CLK 2 2 //

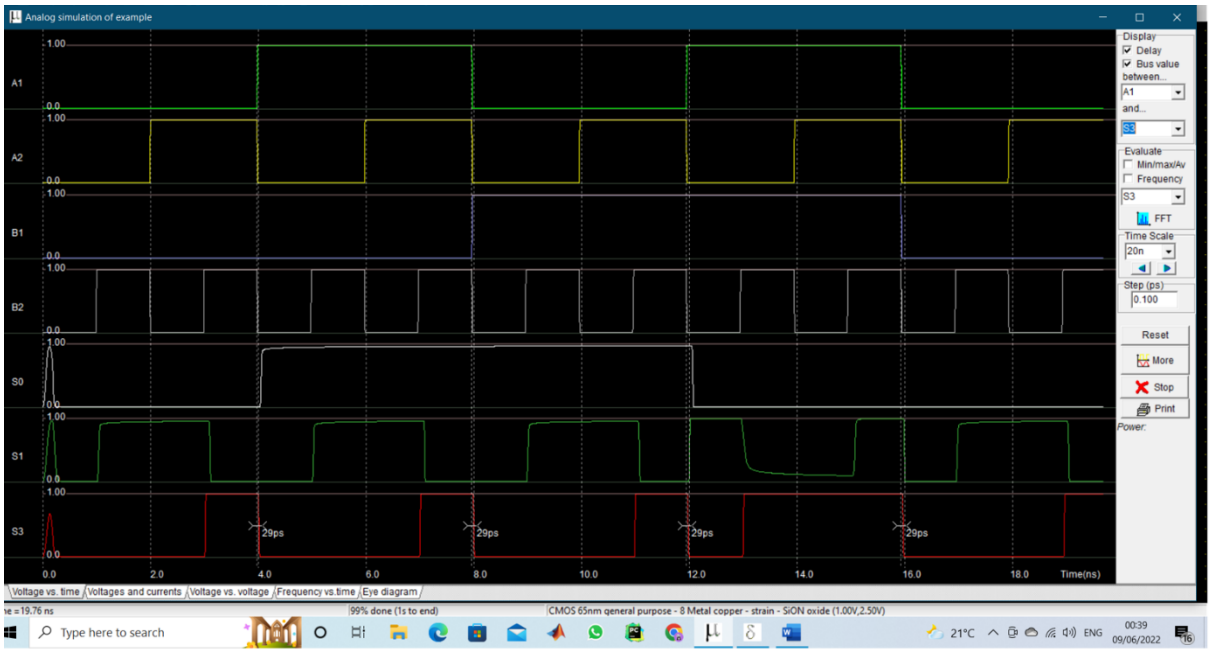
A1 CLK 4 4 //

B1 CLK 8 8 //

: Layout

: Layout





- ✓ We note that the results are identical to the Truth table