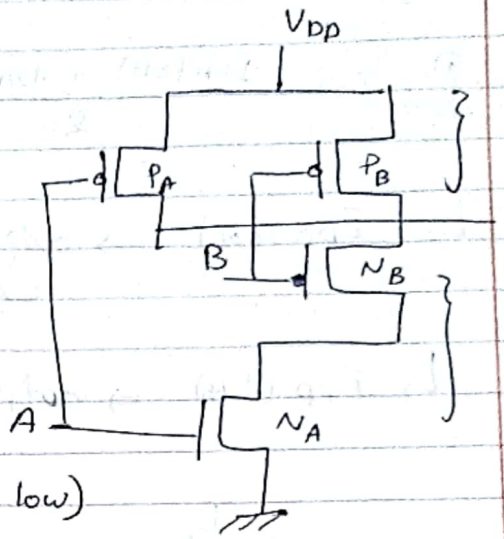
x W / ⇒

CMOS logic Gates [NAND, AND, OR, NOR, And-OR Inverter]

1) NAND ⇒

↳ NMOS → series
PMOS → parallel



$-V_{out} + V_{DS} + V_{DS} = 0$

If A = 0, B = 0 (logic low)
↳ NMOS → off
↳ pMOS → linear

P_A, P_B → linear ⇒ $I_D = 0$ ⇒ $I_{D,P\,B\,linear} = K_P\left[(V_{SG} + V_{T,P})V_{SD} - \frac{V_{SD}^2}{2}\right] = 0$

⇒ $V_{SD} = 0$

$V_{OH} = V_{DD}$ → logic high

A	B	Vout
0	0	1
0	1	1
1	0	1
1	1	0

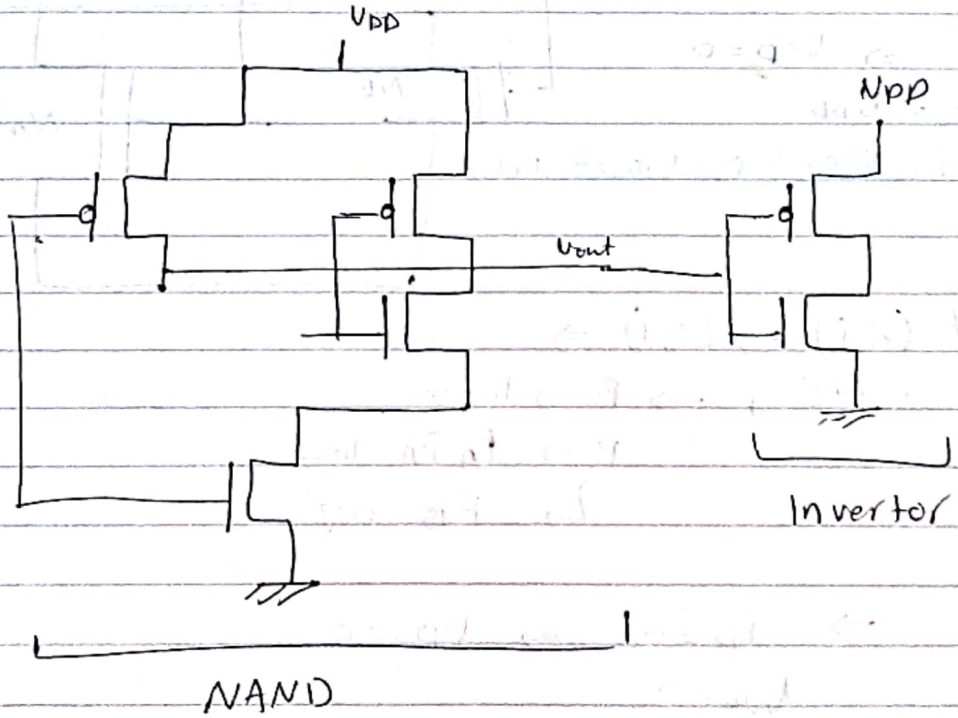
if (A, B = 1) ⇒ logic high → N → linear
P_A, P_B ⇒ off ⇒ $I_D = 0$ ⇒ output
I_D (linear) $= K_n\left[(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right] = 0$

→ $V_{DS} = 0$ ⇒ V_{OL} = Zero

For symmetry s=1

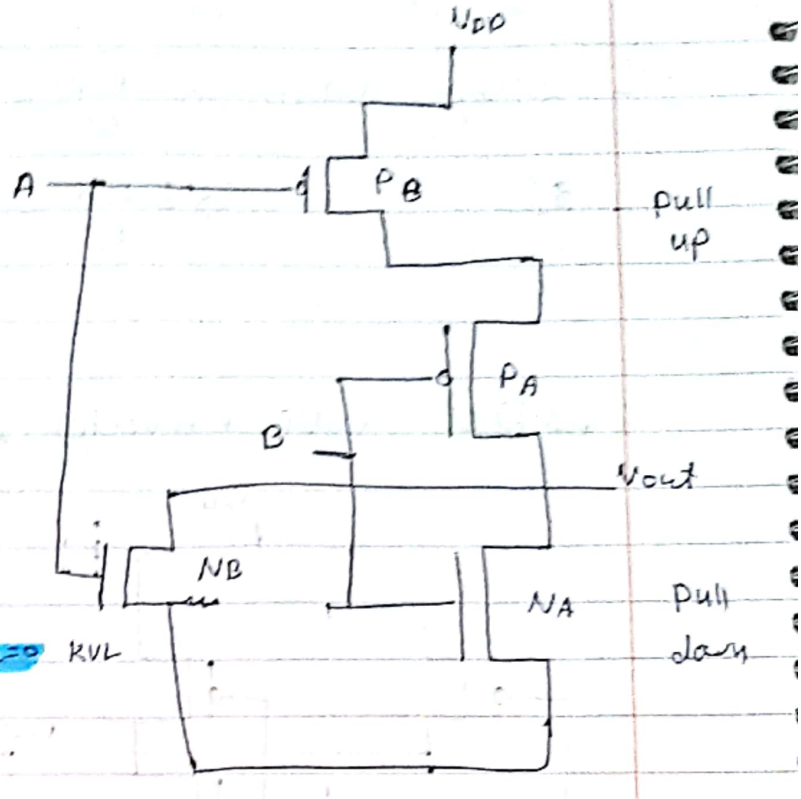
- single input $\Rightarrow \frac{W_P}{L_P} = 2.5 \frac{W_N}{L_N}$
- 2- Input NAND $\Rightarrow \frac{W_P}{L_P} = \frac{2.5}{2} \frac{W_N}{L_N}$
- 3 input : $\Rightarrow$ i $\frac{W_P}{L_P} = 2.5 \frac{W_N}{L_N}$

AND : NAND + Inverter



3 NOR gate

NMOS ⇒ parallel
pMOS ⇒ series



1) input low ⇒ (A, B = 0)
   ↳ N → off
   ↳ P → linear

يوخذ الـ output من الـ pull up

$I_D = 0 \Rightarrow V_{SD} = 0$

$V_{OH} = V_{DD}$

↳ $V_{out} = V_{DD} - V_{SD_1} - V_{SD_2} = 0$ KVL

2) input (A, B) → (0, 1) ⇒
   A → off , → B → linear
   P → P_A linear
   ↳ P_B off

⇒ $I_D = 0$ ⇒ $V_{DS} = 0$

$V_{OL} = 0$

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

* XNOR ⇒ $Z = \overline{A \oplus B} = \overline{A\bar{B} + \bar{A}B}$

XOR = $\bar{a}.b + a.\bar{b}$

For symmetric ⇒ 1)

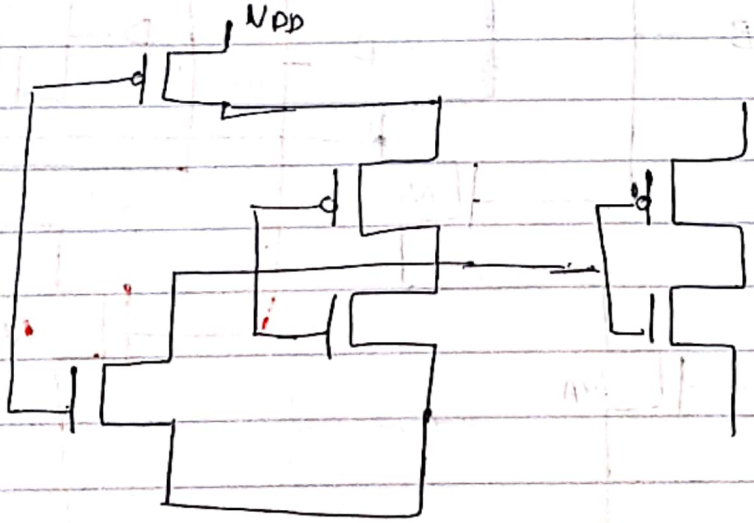
Single Input → $\frac{W_P}{L_P} = 2.5 \frac{W_N}{L_N}$

2-Input → $\frac{W_P}{L_P} = (2.5)(2) \frac{W_N}{L_N}$

3 input → $\frac{W_P}{L_P} = 2.5 (3) \frac{W_N}{L_N}$

(4) OR ⇒ 1)

NOR + Inverter



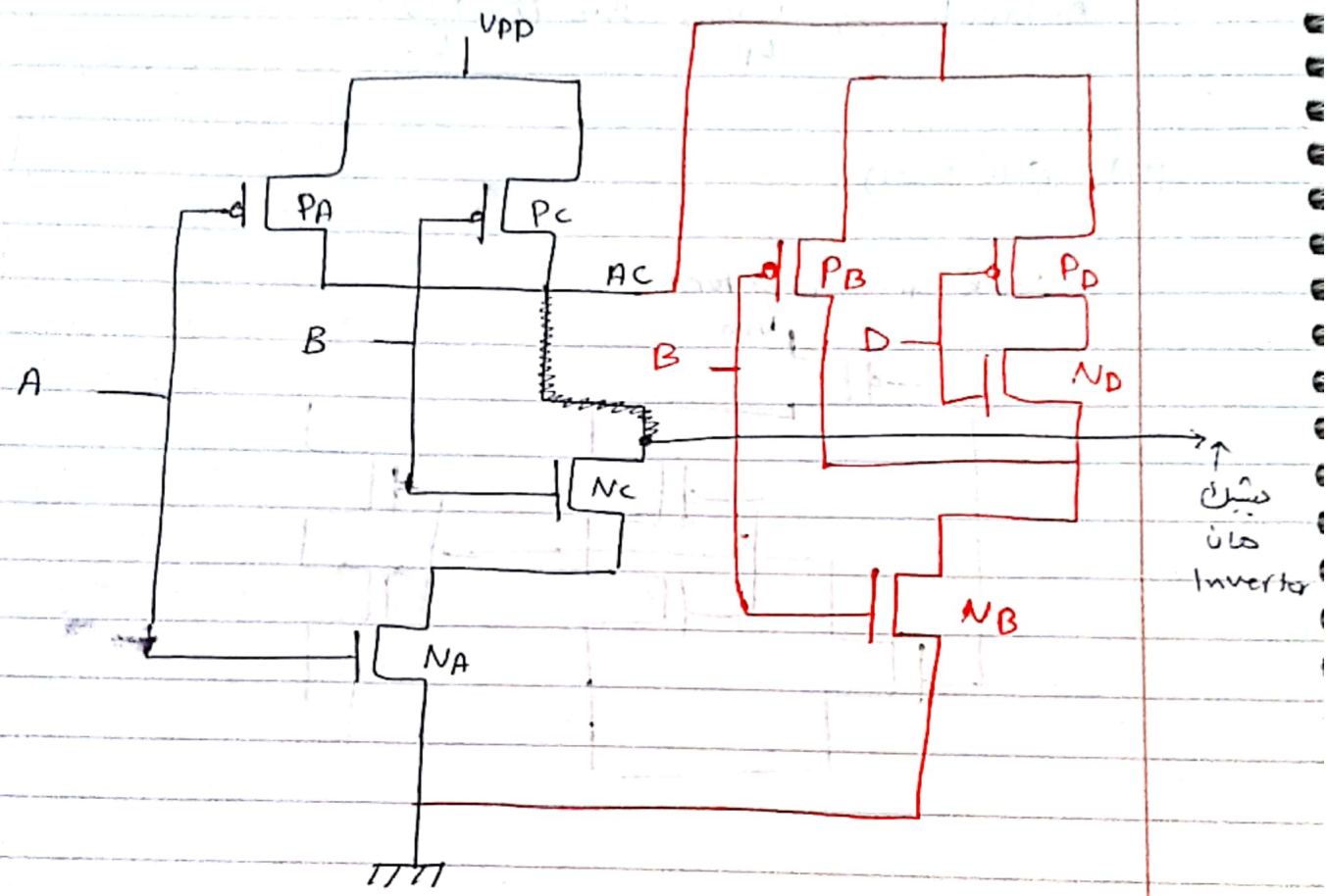
VI)

[5] AND- OR Inverter logic functions

examples =)) $F = \overbrace{A\,C} + B\,D$

N → ser

P → parallel



- Keep the Invertor Until the end.
- enough to look at NMOS OR PMOS

- For NMOS [A.C ⇒ series , BD ⇒ Series] ⇒ parallel

PMOS ⇒ بالعكس

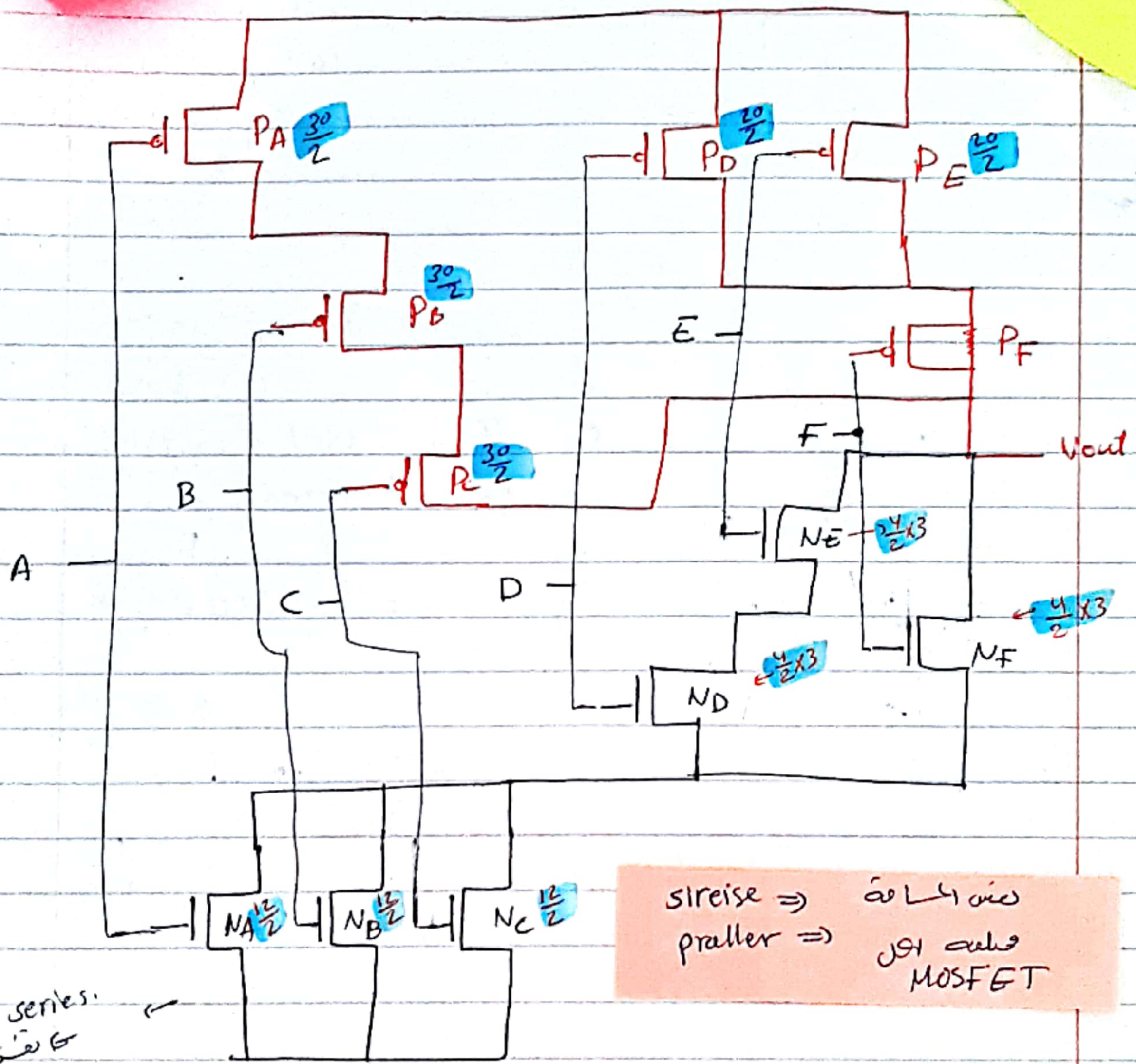
عشان أحدد المسافة بالنسبة لل NMOS : بشوف أطول path من ال Vout إلى ال ground
بشوف انو عندي طريق فيه 3MOS وطريق فيه 2MOS بوخذ ال 3MOS

$3 \times \frac{4}{2}$

عشان أحدد المسافة بالنسبة لل PMOS : ل path ⇐ من (VDD → Vout)
بالنسبة الجزء الأول ⇐ $\frac{10}{2} \cdot 2$
الجزء الثاني

$3 \times \frac{10}{2}$

$$F = \overline{(A+B+C)\cdot(DE+F)}$$



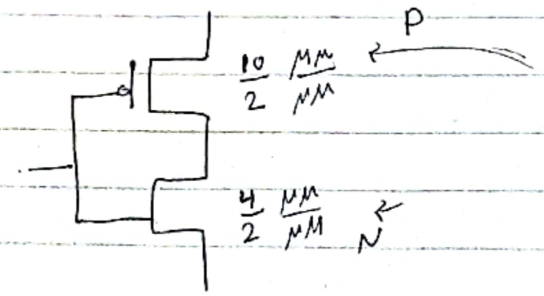
series: ← تقسم المسافة

sireise ⇒ نفس المسافة
praller ⇒ حطها اول MOSFET

If you know that the Inverter: (1) NMOS ⇒ $\frac{W_N}{L_N} = \frac{4}{2}\ \frac{\mu m}{\mu m}$

Find the Area.

Ans:



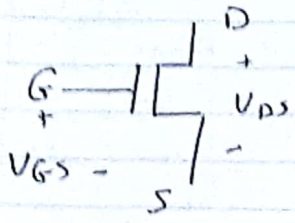
$\frac{W_P}{L_P} = 2.5\ \frac{W_N}{L_N}$

$2.5 \cdot \frac{4}{2}$

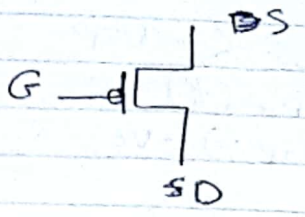
$\frac{5}{2} \cdot \frac{4}{2}$

MOSFET :=)

1) N-channel:



2) P- channel:



for n-channel: =)

1) cut-off.

$-V_{TN} > V_{GS}$, $I_D = 0$

↳ thershold voltage.

* $V_{DS(sat)} = V_{GS} - V_{TN}$

2) Sat mode:

- $V_{GS} > V_{TN}$
- $V_{DS(sat)} < V_{DS}$

* $I_{D(sat)} = \frac{K_n}{2}[V_{GS} - V_{TN}]^2$

3) Linear mode :

- $V_{GS} > V_{TN}$
- $V_{DS} < V_{DS(sat)}$

$$I_{D(linear)} = K_n\left[(V_{GS} - V_{TN}) \cdot V_{DS} - \frac{V_{DS}^2}{2}\right]$$

* $K_n = \mu_n C_{ox}' \frac{W}{L}$; $C_{ox}' = \frac{\epsilon_{ox}}{t_{ox}}$

(μ_n: mobility of e; W: width; L: length; C_{ox}': capacity for oxide; ϵ_{ox}: permittivity for oxide; t_{ox}: thickness for oxide layer.)

$K_n = K_n' \cdot \frac{W}{L}$

for p-channel:

1) cut-off:

* $-V_{SG} < -V_{TP}$
* $I_{D,P(off)} = 0$

عشان يشتغل ← $V_{TP} \Rightarrow -Ve$

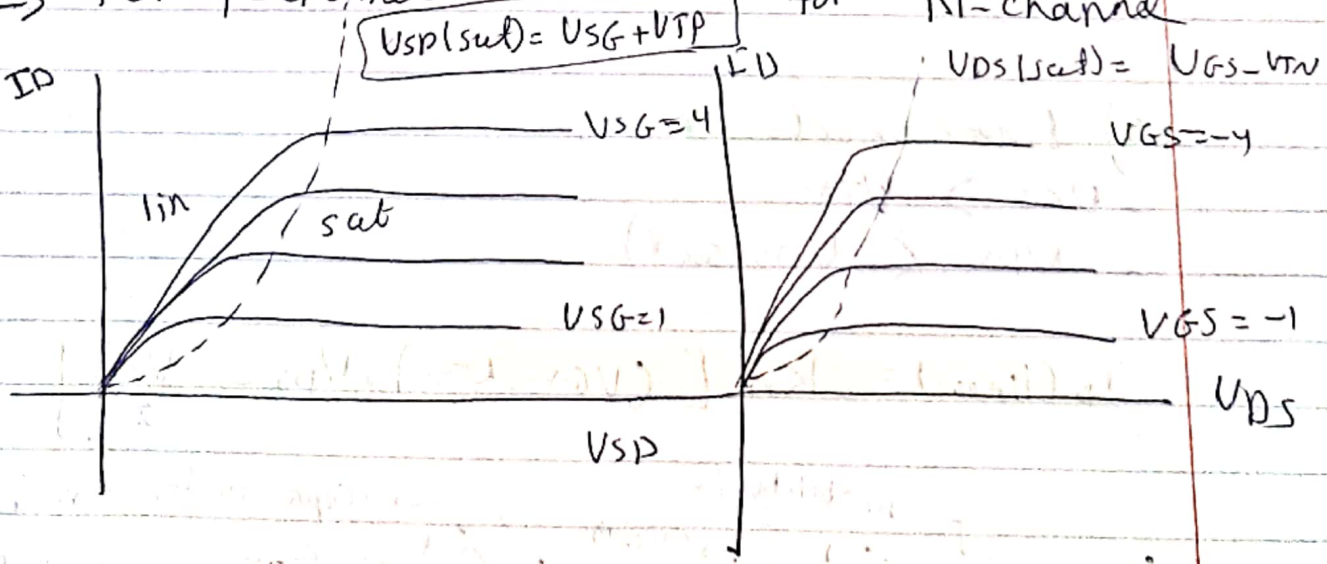
2) sat mode

- $V_{SG} > -V_{TP}$
- $V_{SD} > V_{SD(sat)}$
- $V_{SG} = V_{SG} + V_{T,P}$
- $I_D(sat) = \frac{K_P}{2}[V_{SG} + V_{TP}]^2$

3) linear mode:

- $V_{SG} > -V_{TP}$
- $V_{SD(sat)} > V_{SP}$
- $I_D(linear) = K_P[(V_{SG} + V_{TP})V_{SD} - \frac{V_{SD}^2}{2}]$

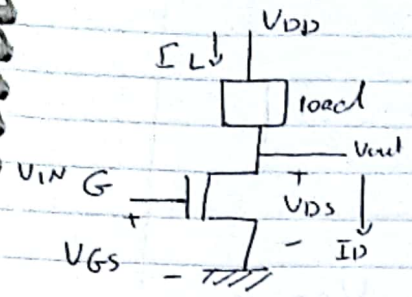
⇒ for p-channel:



for N-channel

$K_P = k_P' \frac{W_P}{L_P}$ ، $K_P = \frac{W_P}{L_P} = \frac{10\,\mu m}{2\,\mu m}$

general N-MOS Inverter.



$V_{IN} = V_{GS}$
$V_{out} = V_{DS}$
$I_D = I_L$

Inverter's

⇒ logic low ⇒ $V_{IN} = V_{GS} < V_{TN}$
Mosfet ⇒ off ⇒ $I_D = 0$ ⇒ $V_{out} = N_{OH} = V_{DD}$

⇒ logic high ⇒ V_{IN} = V_{GS} (high value) > V_{TN}

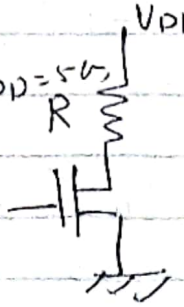
Mos ⇒ linear ⇒ I_D (linear) = ---
Vout = VoL (Inverter) = V_{DS}

⇒ Zero drain Current active mosfet
How? ⇒ load = R_L = ∞ ⇒ [O.C]
In this case,
by Increasing the value of R_L, I_D ⇒ 0, and transistor is in active mode iff (VGS lang enough] VGS > VIN

$$I_D(lin) = K_n\left((V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

if $V_{DS} = 0$ ⇒ $I_D = 0$

example: $K_n = 80\,\mu A/V^2$, $V_{TN} = 2V$, $V_{DD} = 5V$,
when $V_{in} = 5V$ (H), $V_{out} = 0.1V$
also low input $V_{in,L} = V_{GS} = 0$



high, out ⇒
low Input ⇒ zero < VTn(2V) ⇒ MOS off → no current

1) $I_{DD}(OH) = 0V$.

out ⇒ low

2) $I_{DD}(OL) =$

Input ⇒ high (5V)

(linear)

$$I_{DD}(lin) = K_n \left[(V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

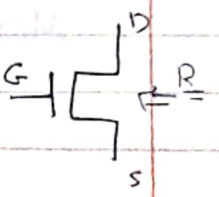
$V_{IN(H)} = 5$, $2V$, 0.6

$$3)\ P_{cc(avg)} = \frac{I_{DD(OL)} + I_{DD(OH)}}{2} \cdot V_{DD}$$

(0)

example

Find the resistance of D-S chamel R_{DS}, for
$V_{GS} = 5V$, $V_{TN} = 1V$, $K_n = 40\mu A/V^2$
when 1) $V_{DS} = 3V$ 2) $V_{DS} = Zero$



Solution $V_{DS(sat)} = V_{GS} - V_{TN}$

$= 5 - 1 = 4$

$4 > 3V \Rightarrow$ linear

since $V_{DS(sat)} > V_{DS}$

$V = IR \Rightarrow$

$$I_D(linear) = K_n \left[(V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

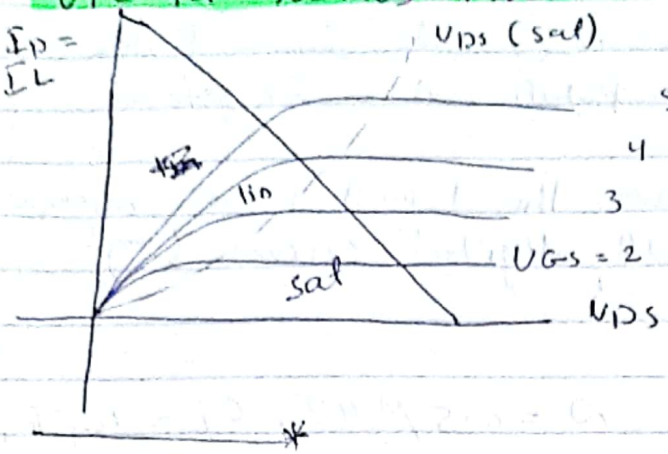
$$R_{DS} = \left. \frac{dV_{DS}}{dI_D} \right|_{V_{DS}} \Rightarrow \frac{1}{R_{ds}} = \left. \frac{dI_D}{dV_{DS}} \right|_{V_{DS}}$$

$$\Rightarrow R_{DS} = \frac{1}{K_n \left[(V_{GS} - V_{TN}) - V_{DS} \right]}$$

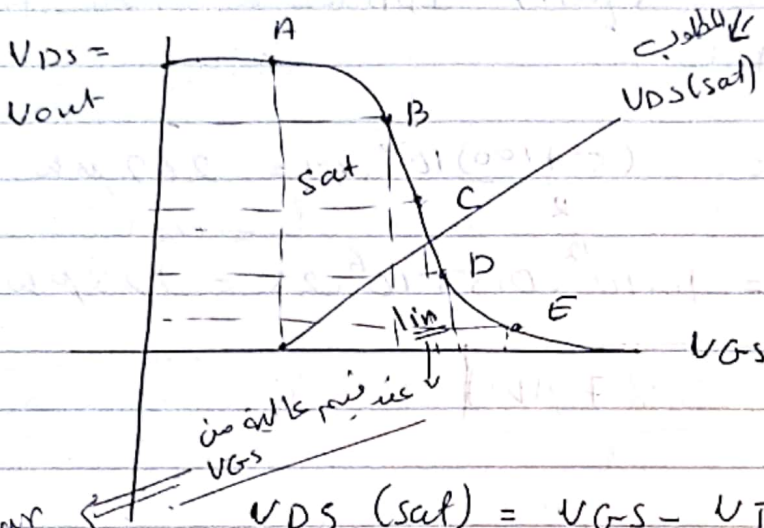
when $V_{DS} = 3V \Rightarrow R_{DS} = 25\ K$

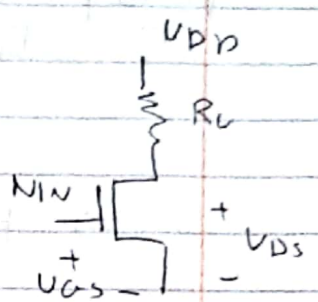
$\quad\quad = 0 \Rightarrow R = 6.25\ K$] → جدول يربط بين $[V_{DS}, R_{DS}]$

VTC for N-MOS Inverter



كلما زادت الـ VGS ← ID بتزيد ← وال MOS بيدخل حالة الـ linear





$V_{DS(sat)} = V_{GS} - V_{TN}$ ∴ $V_{TN} = 1V$

Power dissipation

- static power = $\frac{I_{DD(0H)} + I_{DD(0L)}}{2} \cdot V_{DD}$
- dynamic power = $C_L \cdot \omega \cdot V_{DD}^2$
  - C_L: total load capacitance (F)
  - ω: the switching frequency (Hz)

$P_{total} = P_{static} + P_{dynamic}$

* Mosfet circuit have the lowest power dissipation compared with all digital circuit (T)

ex: $V_{DD} = 5V$, $f = 0.5MHz$, $C_L = 10pF$, $I_{DD}(OH) = 5\mu A$, $I_{DD}(OL) = 100\mu A$, find PT.

$$\Rightarrow P_{static} = \frac{(5+100)10^{-6}}{2} .5 = 262\mu W$$

$$\Rightarrow P_{dyn} = 10.10^{-12}.0.5.10^{6}.25 = 125\mu W$$

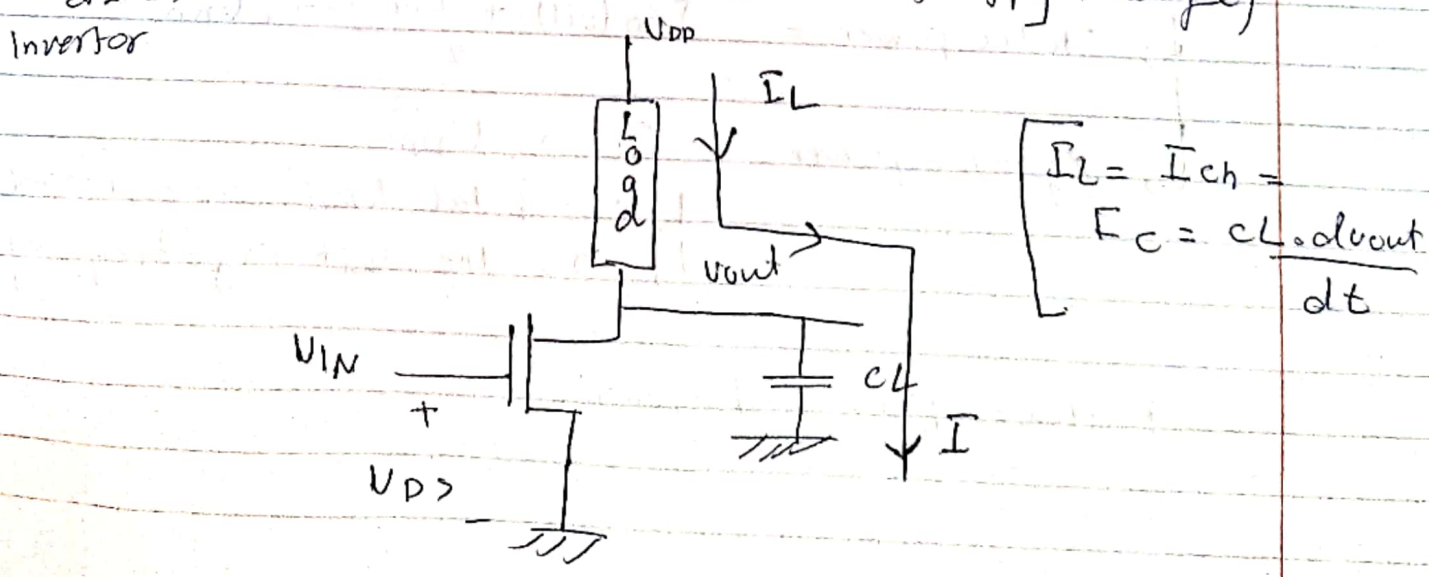
$$P_T = 387\mu W$$

Fan_Out => ↙ capacitance.

L_1 is measured by C_L.

* during charge load (O/P L → H)

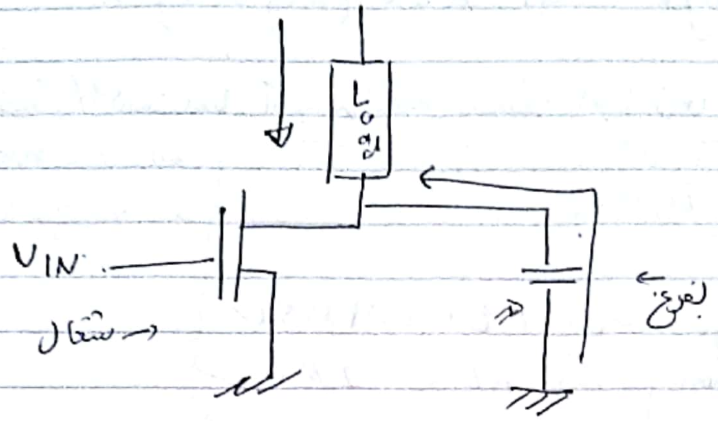
i/P => (H → L) => [linear => off] (charge)



$$I_L = I_{ch} = I_C = C_L \frac{dv_{out}}{dt}$$

[2] during discharging of CL (o/p → (H → L)) i/p → (L → H)

⇒ [off → linear] discharge



$$I_{Dis} = I_{CL} = -C_L \frac{dv_{out}}{dt}$$

Example :=) Find Max (c) , if $I_{CRG} = 50\mu A$,

$I_{Dis} = -20\mu A$, $\Delta t = 2\mu s$, $V_{OL} = 0.5$, $V_{OH} = 5$

$$I = C_L \cdot \frac{dv_{out}}{dt} \Rightarrow$$

$$\int_{t_1}^{t_2} I\, dt = \int_{v_1}^{v_2} C_L\, dv_{out}$$

$$I(\Delta t) = C_L(\Delta v)$$

$$C_L = \frac{I \Delta t}{\Delta v}$$

$$= 50\mu A \cdot \frac{50\,2\mu s}{5 - 0.5} \Leftarrow \text{for charging } V(H-L)$$

$$= \underline{11.1\ pF}$$

بوخذ الأصغر الأقل

$$= \underline{4.44} \Leftarrow \text{for discharge}$$

$I = -20$

$\Delta v = v(L-H)$

check:

if $C = 11.1$

for charging $\Rightarrow \Delta t = \frac{C_L \Delta V}{I_{ch}} = 2\mu s$ ✓

for discharge $\Rightarrow \Delta t = 2.5\mu s$ ✗

فشل الاختبار / احنا بدنا اكبر مواسعة بدهيا ان زمن الشحن والتفريغ:

if $C = 4.44$

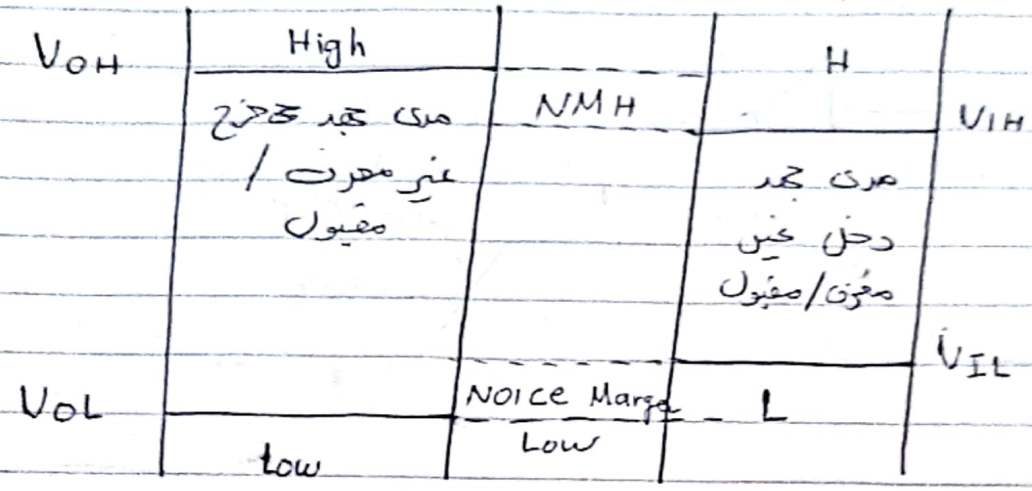
for charge $\Rightarrow \Delta t = 0.4\mu s$ ✓

for discharge $\Rightarrow \Delta t = 2\mu s$ ✓

او $C_L = 4.44pF$

Noice Margain:

هو مقدار الجهد الأقصى الذي يمكن إضافته إلى مدخلات البوابة
والذي لا يؤثر على استقرار الخرج



* توجد مثالان لـ (NM)

(١ NML

لـ هو الفرق بين أقصى
جهد دخل منخفض في الدخل
وأقصى جهد منخفض في
الخرج.

↳ NML = VIL - VOL

(٢ NMH

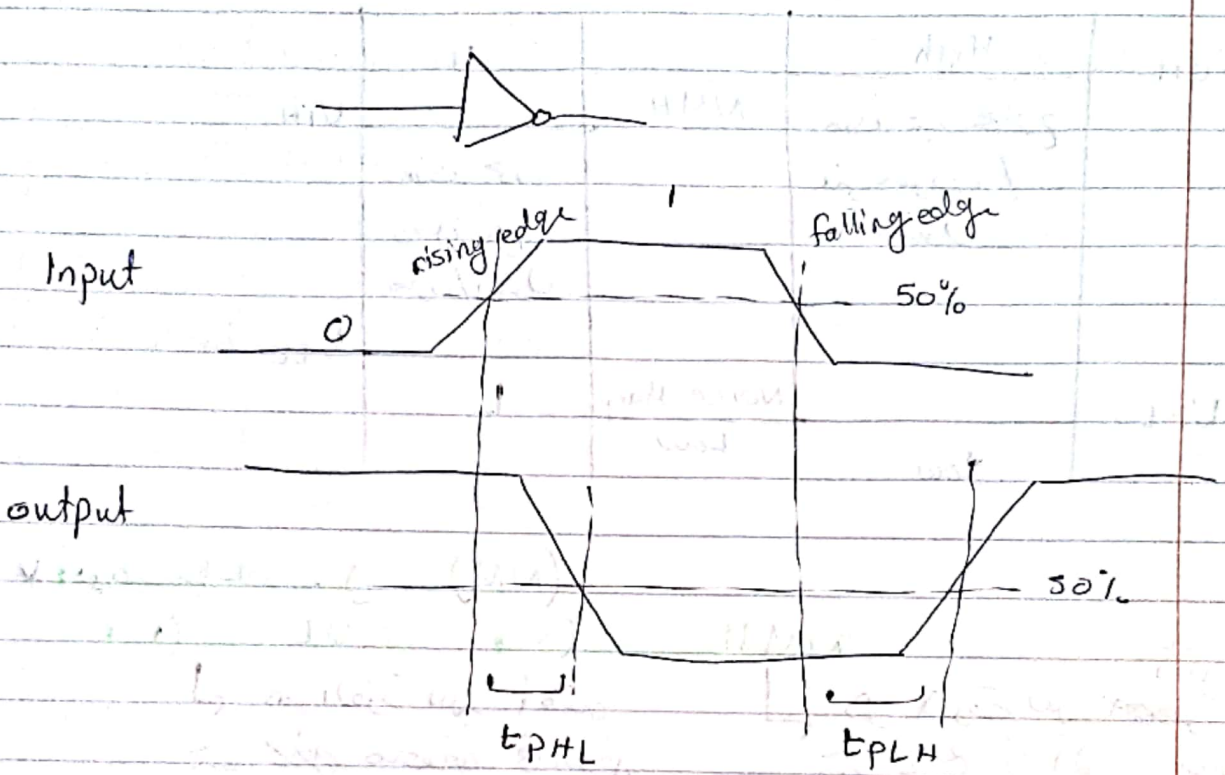
لـ هو الفرق بين أقل
جهد عالي في الخرج وأقل
جهد عالي في الدخل

↳ NMH = VOH - VIH

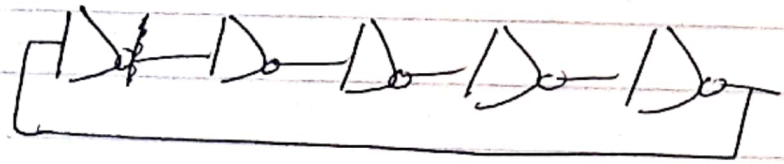
propagation delay :=) p.d

T_{PLH} ⇒ time requiered from output to go from 0 → 1

T_{PHL} ⇒ " " " " " " " 1 → H



$$t_p = \frac{t_{PLH} + t_{PHL}}{2}$$



p.d of each invertor is 100 p s., what ~~is the fundamental frequency~~

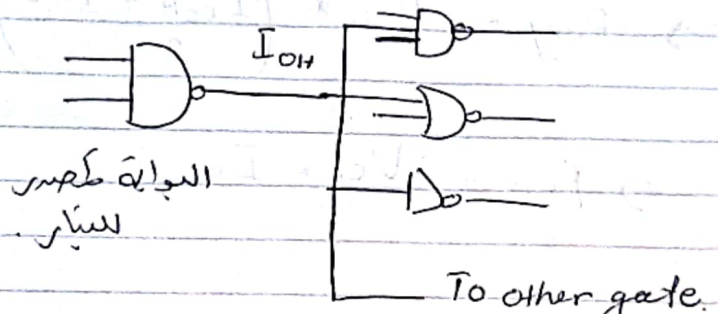
Fan IN and Fan Out

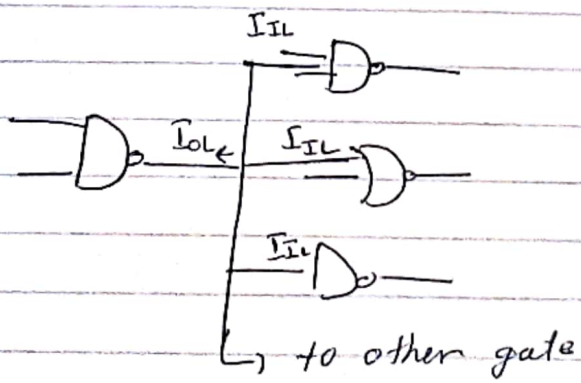
* **Fan-out :** هو أقصى عدد من البوابات المنطقية التي يمكنه توصيلها إلى خرج بوابة منطقية بدون أن تتأثر أداء هذه البوابة.

- يتم حساب الـ Fan-out كالتالي :

$$F_{OH} = \left(\frac{I_{OH}}{I_{IH}}\right)_{max}$$

$$F_{OL} = \left(\frac{I_{OL}}{I_{IL}}\right)_{max}$$

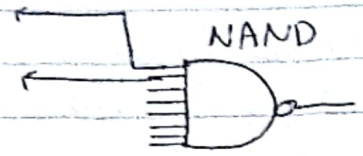




Fan-IN :=)

هو أقصى عدد من البوابات المنطقية التي يمكنه توصيلها إلى دخل بوابة منطقية بدون أن تتأثر أداء هذه البوابة.

كل نوع بوابة له مواصفات



زمن الانتقال من H ← L

$$t_p = \frac{t_{PHL} + t_{PLH}}{2}$$

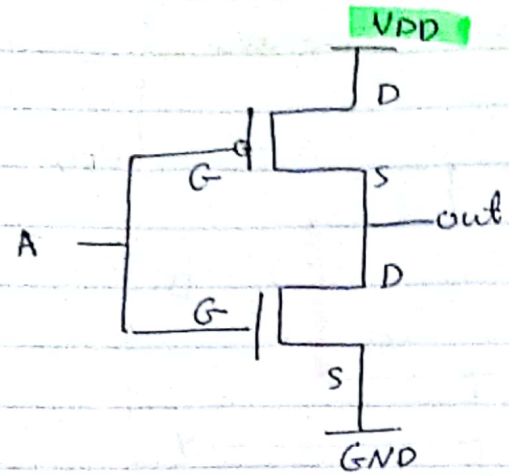
$$F_{OH} = \left(\frac{I_{OH}}{I_{IH}}\right)_{max} \quad ; \quad F_{OL} = \left(\frac{I_{\alpha}}{I_{IL}}\right)_{max}$$

$$TTL \Rightarrow P_{avg} = V_{cc} * \left(\frac{I_{CCH} + I_{CCL}}{2}\right)$$

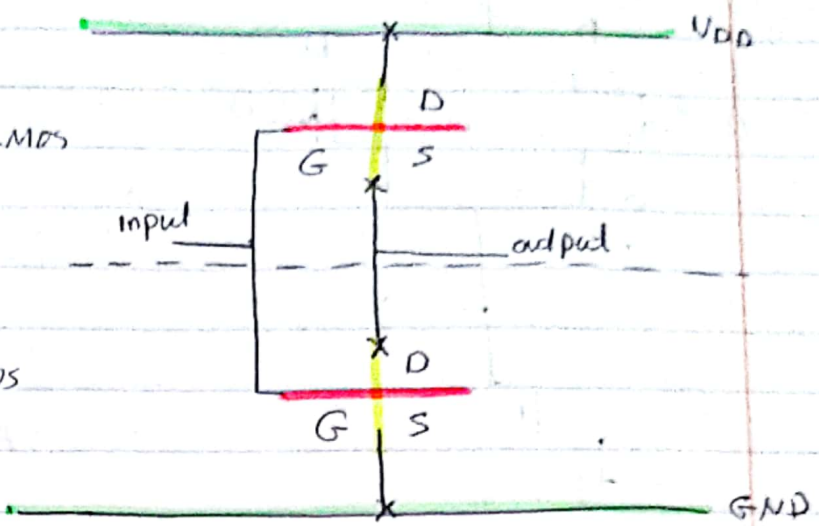
$$CMOS \Rightarrow P_{avg} = V_{cc} \cdot I_{cc}$$

Inverter :

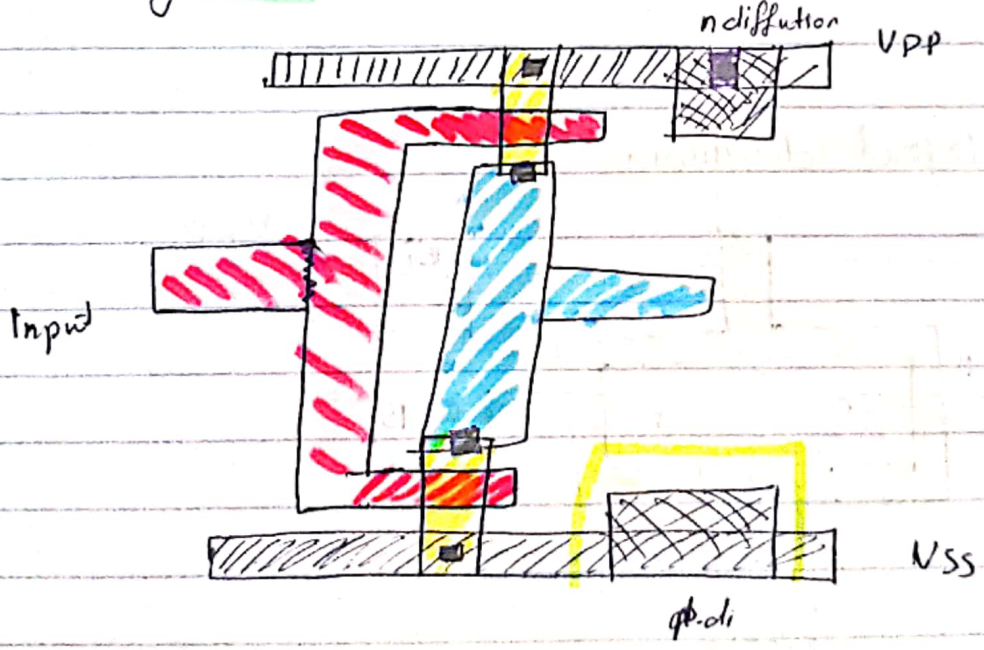
schematic diagram



static diagram

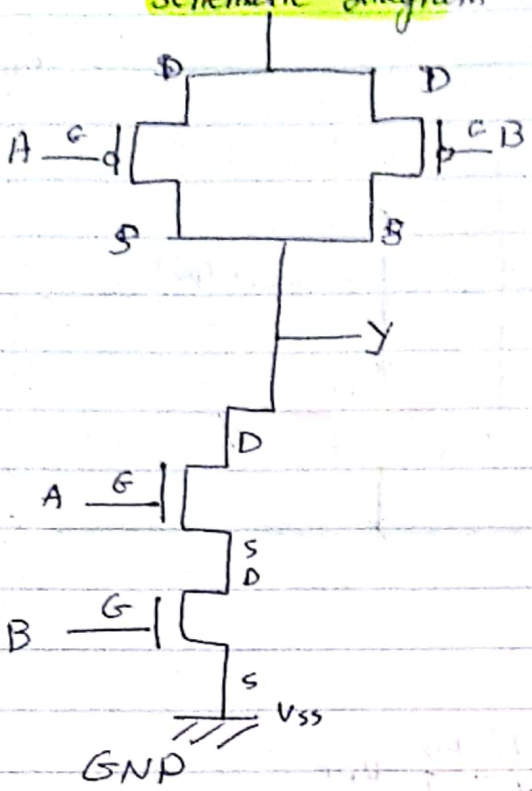


Layout :

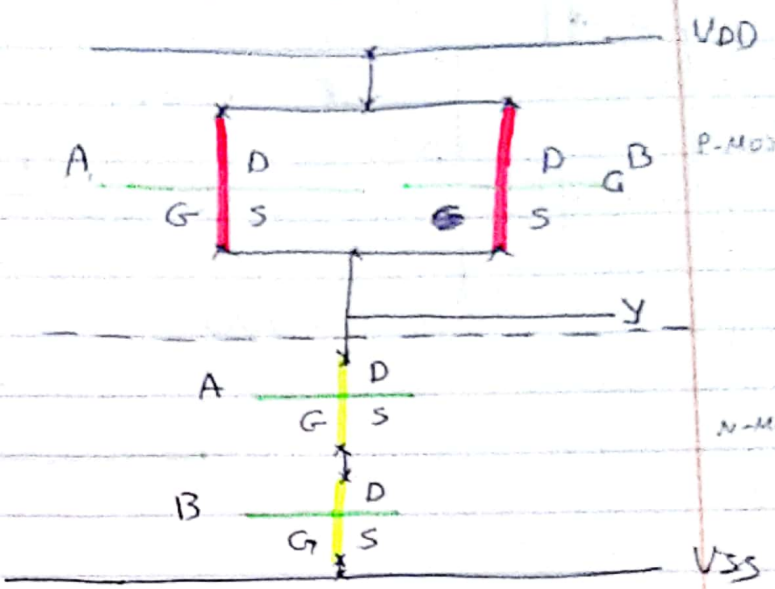


NAND :- $\overline{A \cdot B}$

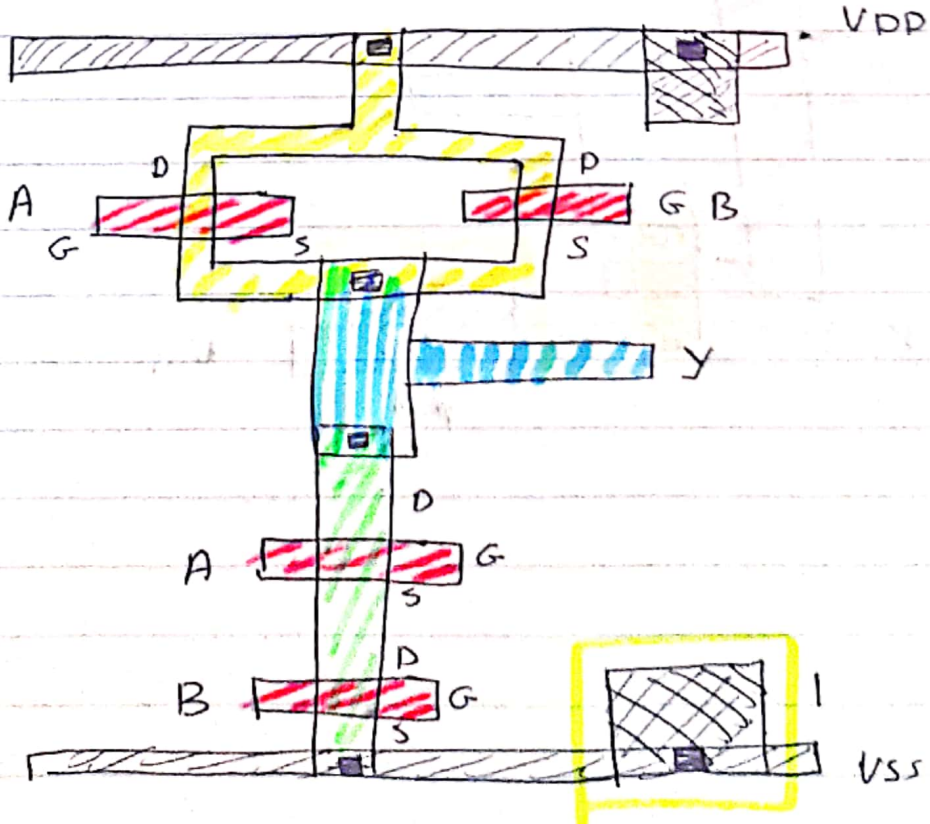
Schematic diagram



static diagram

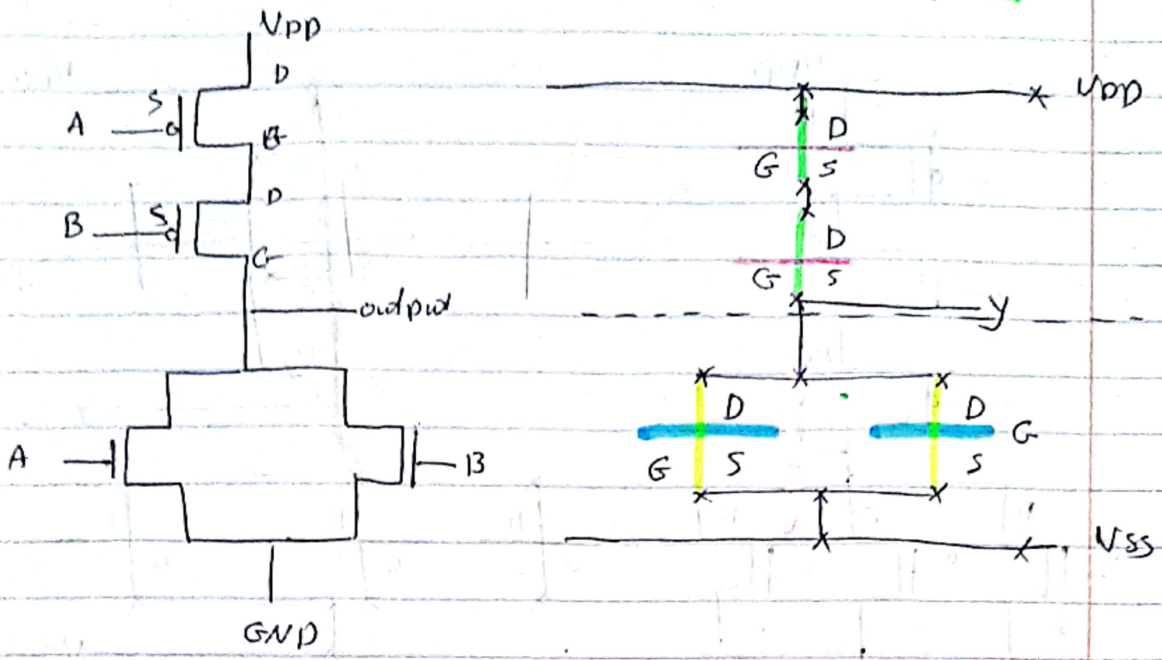


Layout diagram :

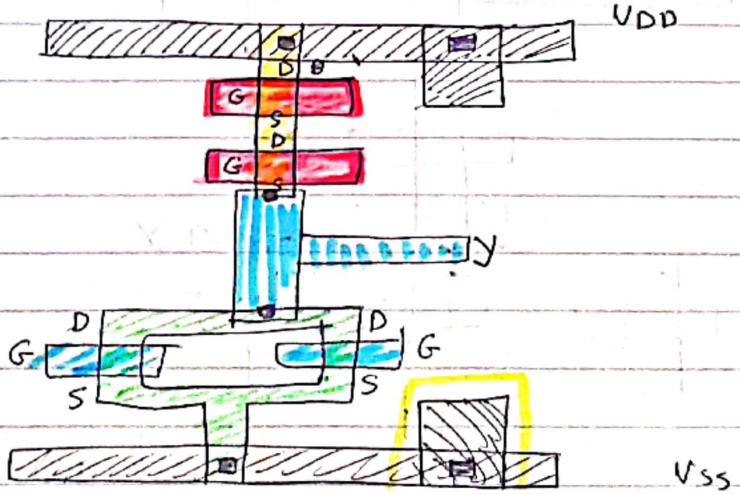


NOR $\overline{A+B}$

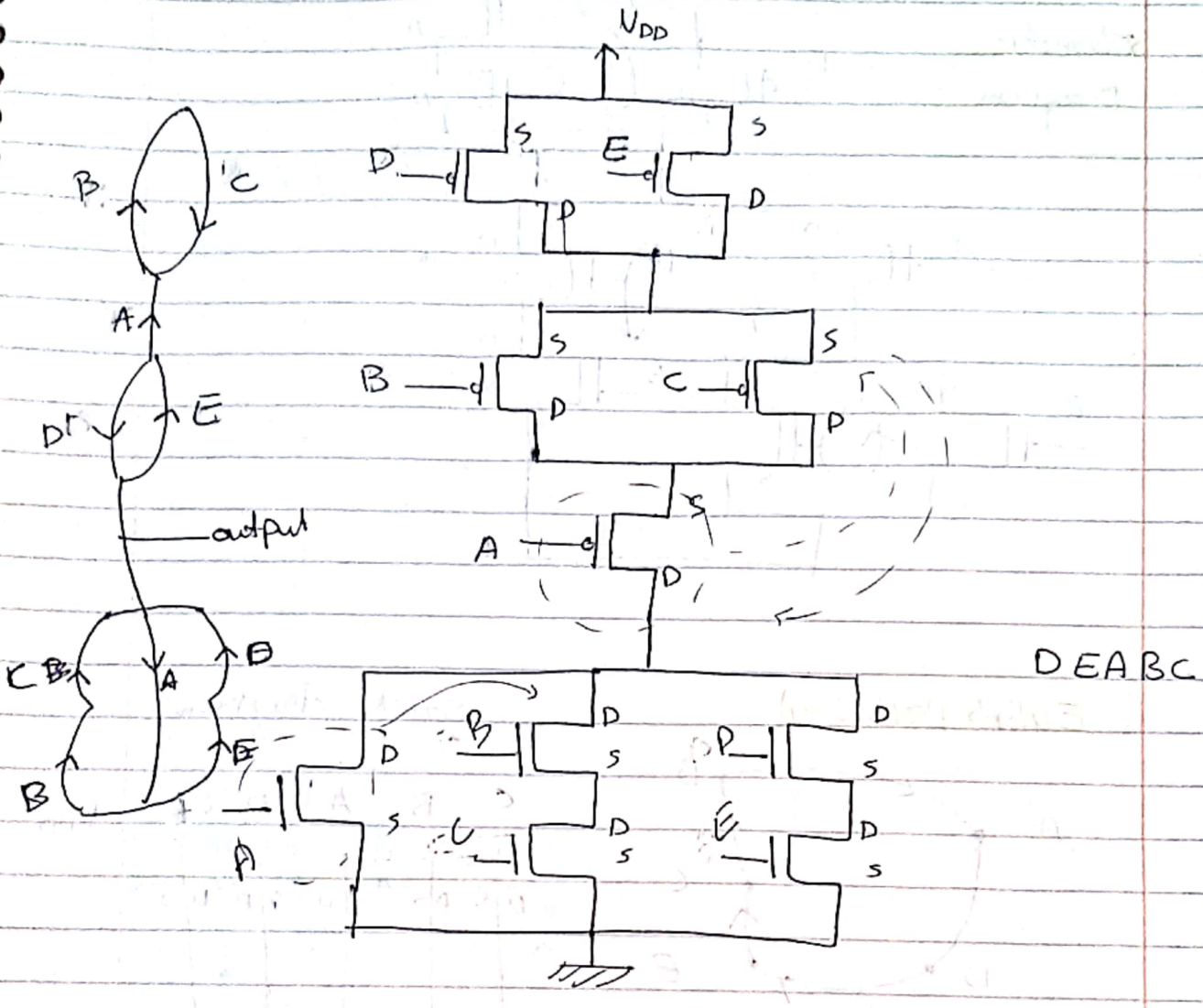
Static diagram

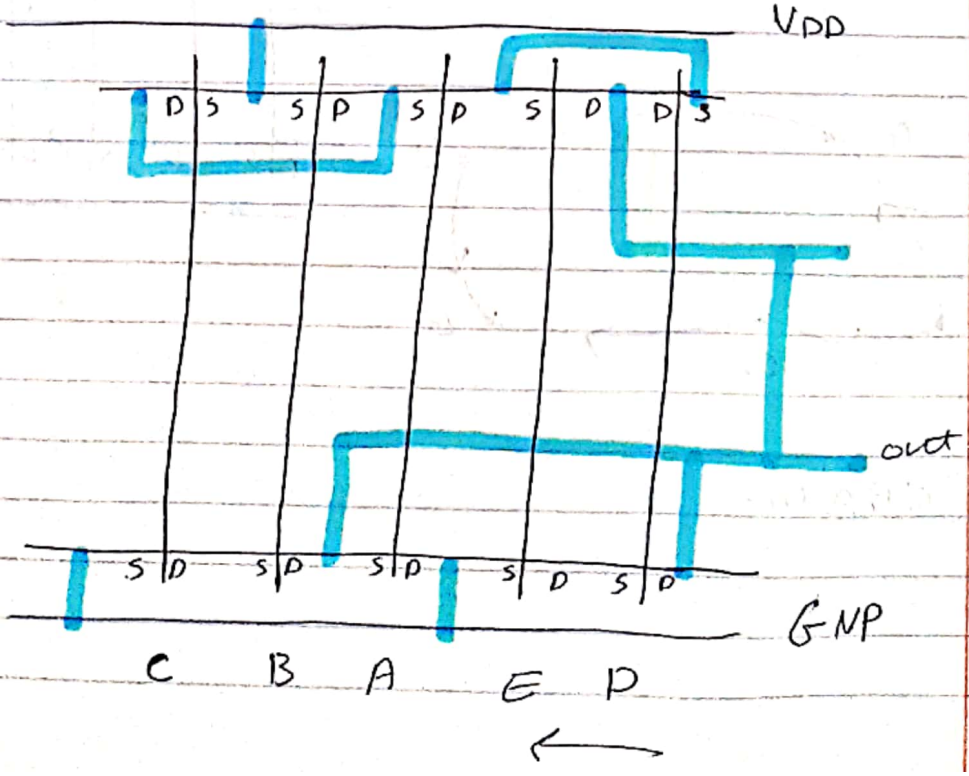


Layout diagram



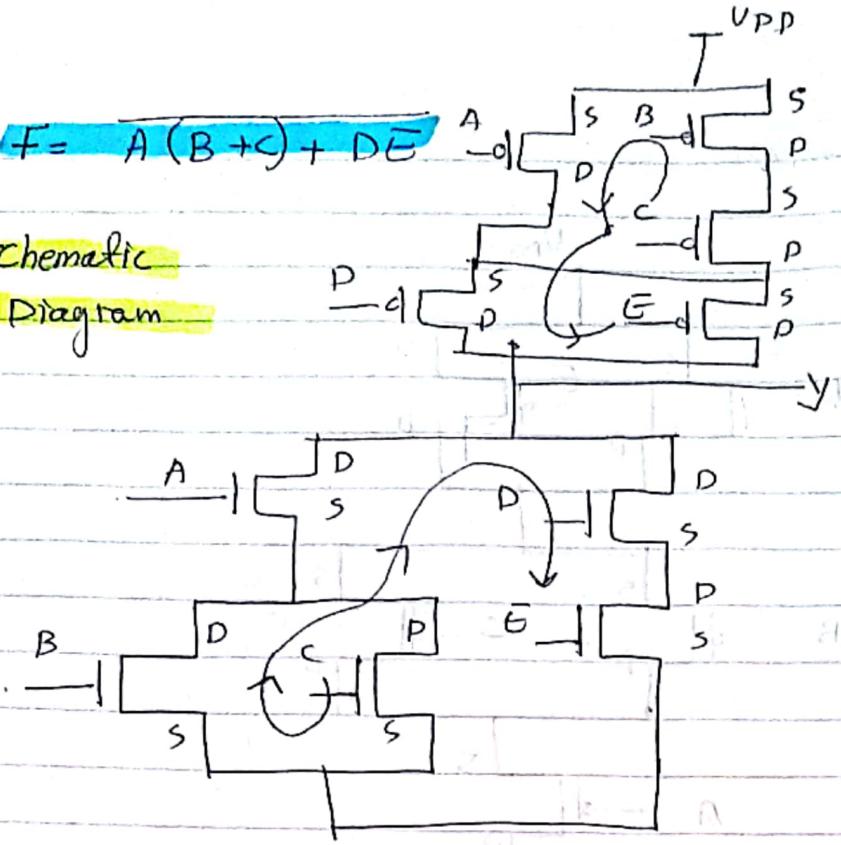
$$F = \overline{A + BC + DE}$$



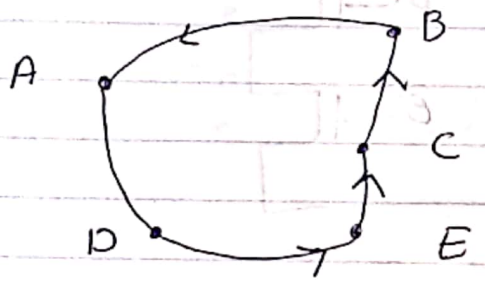


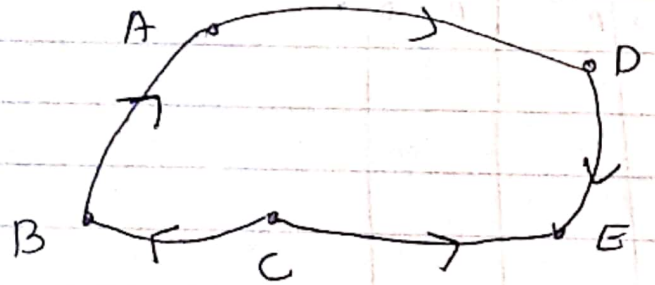
$F = \overline{A(B+C) + DE}$

Schematic Diagram



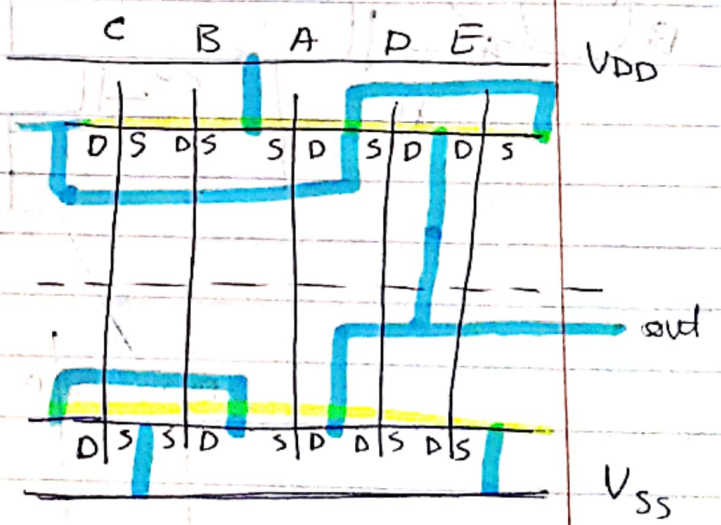
Euler's path :=))





CBA DE

stick diagram



$$I_{DS} = Q/T \quad -(1)$$

$$C = \frac{\varepsilon_o A}{t_{ox}} \;,\; C_{ox} = \frac{C}{A} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$Q = C\,V$$
$$= \frac{\varepsilon_{ox} A}{t_{ox}} \left[(V_{GS} - V_T) - V \right]$$

$$Q = C_{ox}\, WL \left[(V_{GS} - V_T) - V \right]$$

sub in (1)

$$I_{DS} = C_{ox}\, W \frac{L}{T} \left[(V_{GS} - V_T) - V \right]$$

$V_d = \mu E$

$$I_{DS} = C_{ox}\, W\, (V_d) \left[(V_{GS} - V_T) - V \right]$$

$$I_{DS} = C_{ox}\, W (\mu E) \left[(V_{GS} - V_T) - V \right]$$

$$I_{DS} = \mu C_{ox}\, W \left[(V_{GS} - V_T) - V \right] \frac{dV}{dx}$$

$$\int_0^L I_{DS}\, x\, dx = \int_0^{V_{DS}} \mu C_{ox}\, W \left[(V_{GS} - V_T) - V \right] dV$$

$$I_{DS}(L - 0) = \mu C_{ox}\, W \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

for small $V_{DS} \Rightarrow$

$$I_{DS} = \mu C_{ox} \left(\frac{W}{L} \right) \left((V_{GS} - V_T) V_{DS} \right)$$

$V_{DS} = V_{GS} - V_T \Rightarrow$ saturation

$$\Rightarrow I_{DS} = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2$$