$$I_D = \frac{\mu_n \varepsilon_{ox}}{2T_{ox}} \frac{W}{L} \left(V_{GS} - V_{tn} \right)^2 \qquad \text{(Saturated State)}$$

$$I_D = \frac{\mu_n \varepsilon_{ox}}{2T_{ox}} \frac{W}{L} \left[2\left(V_{GS} - V_{tn}\right)V_{DS} - V_{DS}^2 \right] \qquad \text{(Non-Saturated State)}$$

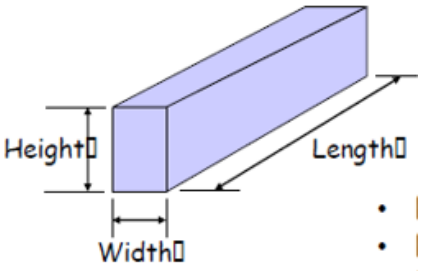
$$K = \frac{\mu \varepsilon_{ox}}{2T_{ox}} \qquad V_t = V_{to} \pm \gamma \left(\sqrt{\left|2\phi_F\right| + V_{SB}} - \sqrt{\left|2\phi_F\right|} \right)$$

Q1: 25 points

1. What are the two types of CMOS transistor? Explain the Working Region of both devices , are they sized the same to have equal rise and fall time , if not why ? (6 points)
   - P channel and N channel semiconductor devices OR PMOS or NMOS, For CMOS technology
   - N works when we have positive voltage on the gate, N mos when we have zero voltage on the gate
   - No, N faster than P so p has bigger size
2. How does the Current flow in CMOS? From where to where? (2 points)
   - Nmos d→s
3. What are the basic design matrixes? (6 points)
   - Area/cost, Power, speed
4. What or how does the temperature affect CMOS devices? (2 points)
   - As temperature increased, the Speed will be go low as temp increased because Vt will increase
5. Explain What do we mean by process node? And how does that affect IC characteristics ? (3 points)
   - The technology node (also process node, process technology or simply node) refers to a specific semiconductor manufacturing process and its design rules.
   - Different nodes often imply different circuit generations and architectures. Generally, the smaller the technology node means the smaller the feature size, producing smaller transistors which are both faster and more power-efficient. Historically, the process node name refered to a number of different features of a transistor including the gate length as well as M1 half-pitch
6. What is drive strength? (2 points)

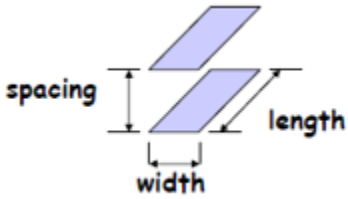
- Driver has raise/fall time proportional to the load

7. If you have wire as in the figure below, How do you calculate its resistance? What can I do toreduce the resistance by almost half ? (2 points)



- R= rL/A = r.Length /(width*length)
- Use different r, reduce length or increase width

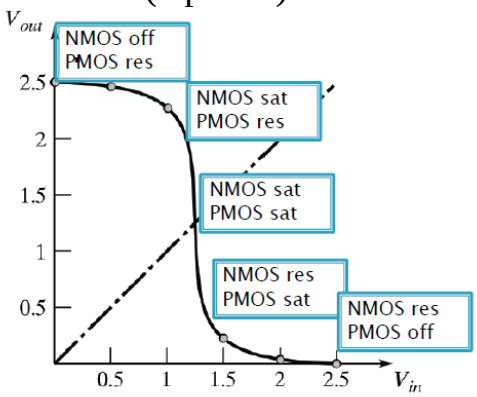
8. If we have 2 wires (plates as in figure below, how do you calculate the capacitance between them ? (2 points)



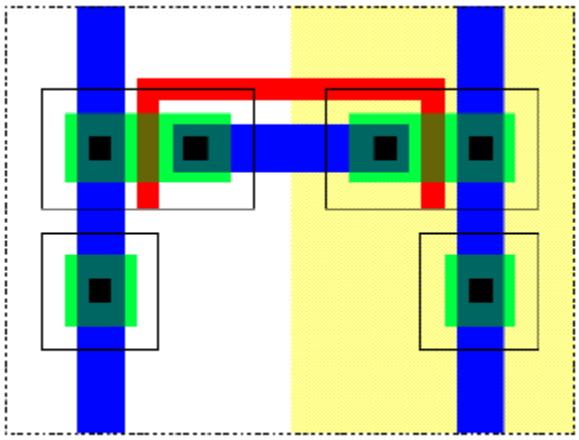
9. C=eps*A/d

Q2: 25 points

1. Draw a VTC curve for a CMOS invertor and SHOW regions of operation for each device (3 points)

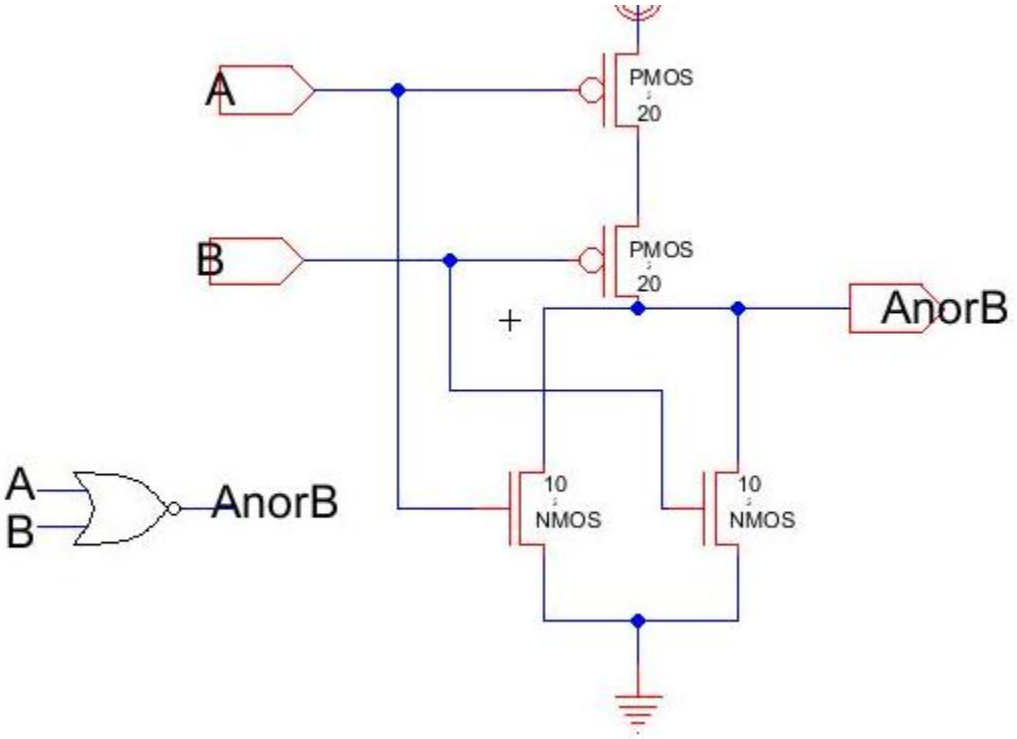


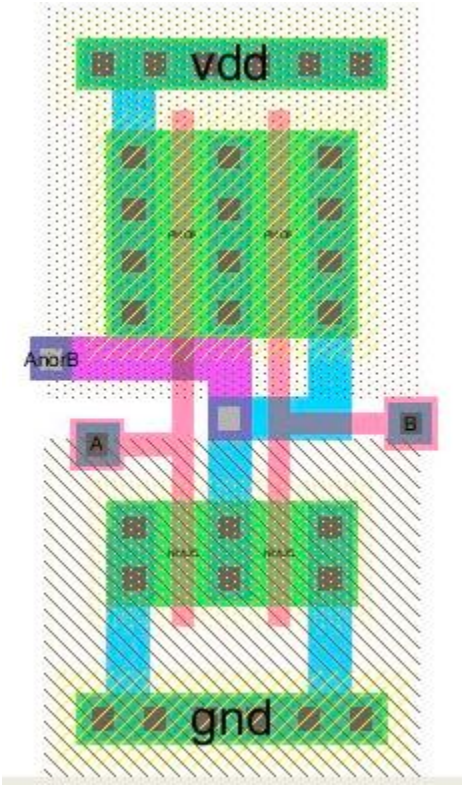
2. What will happen to the rise and fall slopes if we double both the NMOS and PMOS width? (2 points) lower
3. Draw A detail layout showing all materials and estimate dimension for inverter with p device size of 3u and n device of 1 u using 25nm process (5 points)



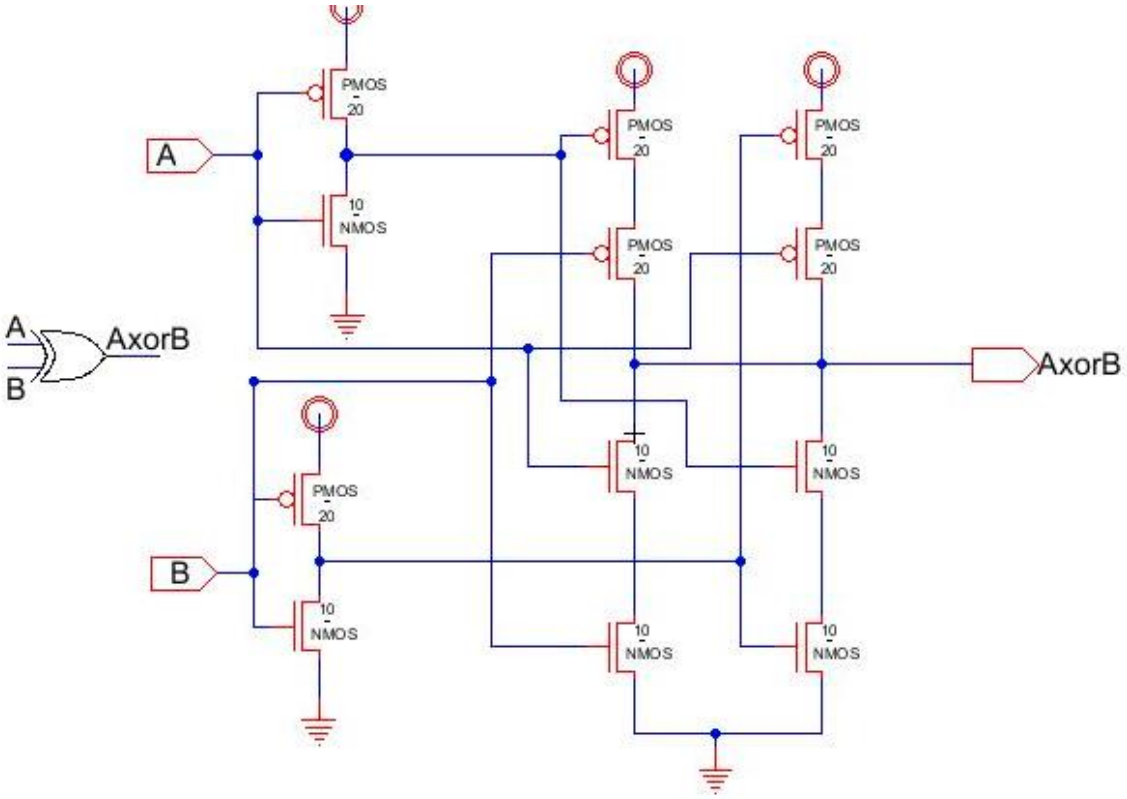
4. Why do VLSI chips have multiple metal layers? What are these used for? Why so many? (2 points)
   - Used for routing, the device become smaller, so we can have many devices so we can add more function in the same chip which required lot of routing, so we need more layers

5. Draw schematic and layout for a CMOS 2 input NOR gate which will have equal rise and fall time as an inverter which has N to P ration 2 using 90nm process and N device width for regular inverter is =10u? Note mark all layers used in layout (8 points).


A
B
PMOS
20
PMOS
20
AnorB
10
NMOS
10
NMOS
A
B
AnorB


vdd
AnorB
A
B
gnd

1. Draw schematic for 2 input XOR gate (transistor level only, (no layout is required and size them correctly assuming ratio of n/p ratio of 2 ? (5 points)



Q3: 25 points

1. How do you measure wire delay ? SLOPES? (4 points)
   a. 50% OF THE SIGNAL , 20/80% for slopes
2. What is the impact of technology scaling on Resistance, Capacitance and RC (3 points)

SEE NOTES LOWER PROCESS WILL HAVE LESS CAP AND LESS R IN GENRAL, BUT WIDTH of wires can't be lower since it is small so it will have larger cap so it does not scal as devices width and length so wire rc will be dominant in low process

3. If you want to reduce the leakage, will you use the high threshold or the low threshold devices and why ? . (3 points)

4. Construct the CMOS logic circuit that implements= Y= a + (a' + b)' +cb' using the fewest possible transistors and size them to have equal rise and fall time with ration of n/p OF 2. You are allowed to use inverted inputs (e.g., a') rather than adding inverters to create these signals. (15 points)

solution

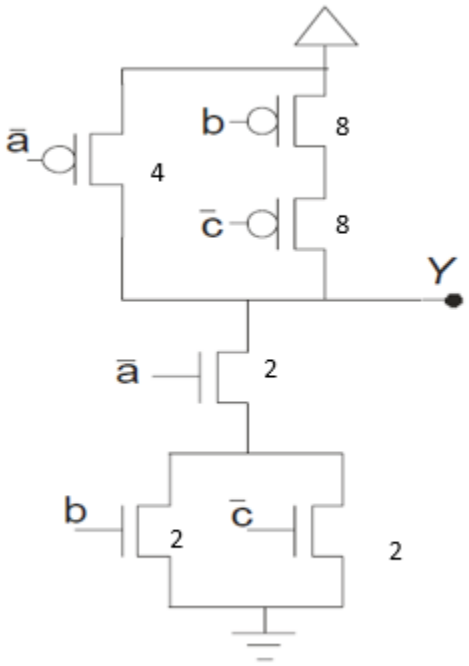
First let's simply the function to remove all inverted operations

$Y = a + (a\bar{b}) + c\bar{b}$

$Y = a + c\bar{b}$ (because A+AX = A)

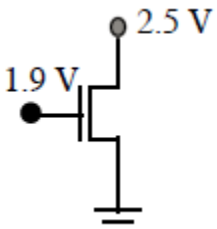
Thus

$Y_p = \bar{a} + \bar{c}b$, and $Y_n = \bar{a} \cdot \overline{c\bar{b}} = \bar{a} \cdot (\bar{c} + b)$, which looks correct because all AND/OR operations are complemented between Yp and Yn, and both have the same inputs. Substituting parallel connections for OR operations and series connections for ANDs, we get:

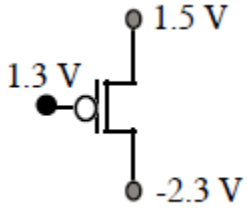


Q4: 25 points

1. Determine the bias state for the two circuit conditions if Vtn = 0.4 V. where Vtp = -0.4 V (10 points)

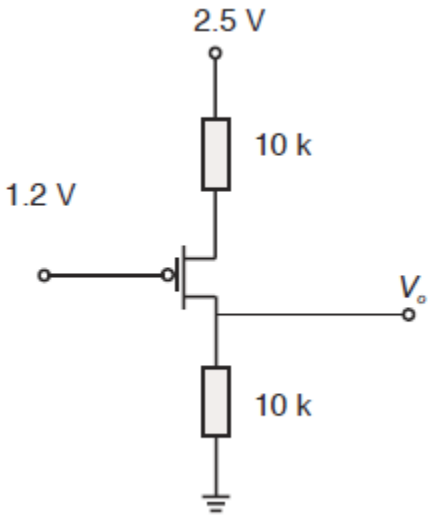


V_{GS} = 1.9 V, V_{DS} = 2.5 V, V_{tn} = 0.4 V, therefore V_{GS} = 1.9 V < 2.5 V + 0.4 V = 2.9 V. Eq. (3-7) is satisfied, and the transistor is in the saturated state described by



b) The gate voltage is not sufficiently more negative than either drain or source terminal to invert holes at the oxide interface, so that the transistor is in the offstate.

2. Calculate ID, VDS , and verify the assumed bias state of transistor M1 for Vtp = –0.4 V, Kp = 60 μA/V2, and W/L = 2. (15 points)



Assume a saturated bias state and

$$I_D = \frac{\mu\varepsilon_{ox}}{2T_{ox}}\frac{W}{L}(V_{GS} - V_{tp})^2$$

Since V_{GS} is not known, we must search for another expression to supplement this equation.

We can use the KVL statement

$$\begin{aligned} V_{GS} &= 1.2 - (V_{DD} - (I_D R_S)) \\ &= 1.2 - 2.5 + I_D R_S \\ &= -1.3 + (10\ \text{k}\Omega) I_D \end{aligned}$$

We substitute this into the saturated current expression to get

$$\begin{aligned} I_D &= 60\ \mu\text{A}(2)\left[-1.3 + (10\ \text{k}\Omega) I_D + 0.4\right]^2 \\ &= 120\ \mu\text{A}\left[-0.9 + (10\ \text{k}\Omega) I_D\right]^2 \end{aligned}$$

This quadratic equation in I_D gives solutions

$$I_D = 35.56\ \mu\text{A},\ 227.8\ \mu\text{A}$$

The valid solution is $I_D = 35.66\ \mu$A, since the other solution for I_D when multiplied by the sum of the two resistors gives a voltage greater than the power supply. V_{DS} is then

$$\begin{aligned} V_{DS} &= I_D (20\ \text{k}\Omega) - V_{DD} \\ &= (35.56\ \mu\text{A})\ (20\ \text{k}\Omega) - 2.5\ \text{V} \\ &= -1.789\ \text{V} \end{aligned}$$

and

$$\begin{aligned} V_S &= V_{DD} - I_D R_S = 2.5 - (35.56\mu A)\ (10k\Omega) \\ &= 2.144\ V \end{aligned}$$

Verify the bias state

$$V_{GS} = V_G - V_S = 1.2 - 2.144 = -0.944\ \text{V}$$

Transistor M1 is in saturation since

$$\begin{aligned} V_{GS} &> V_{DS} + V_{tp} \\ -0.944\,\text{V} &> -1.789\,\text{V} - 0.4\,\text{V} \end{aligned}$$