Student Name =
Student ID =
Student Grade =

Question	Full Grade	Student Grade	ABET OUTCOME
1	10		a
2	10		c
3	10		k
4	10		c
	40		

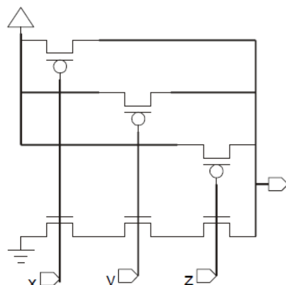
Question 1 (10 pts)

1	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*Total*
F	*T*	*F*	*T*	*T*	*F*	*T*	*F*	*T*	*T*	

1. To set the switching threshold (midpoint) voltage, Vm, to VDD/2 in a CMOS inverter, the nMOS transistor must be wider than the pMOS.
2. Increasing power supply voltage, VDD, will increase the speed performance of CMOS gates.
3. The best way to improve the speed performance of a CMOS circuit is to decrease the channel
4. CMOS = Complementary MOS use of both nMOS and pMOS to form a circuit with lowest power consumption.
5. Electric Fields: vertical field through gate oxide determines charge induced in channel while horizontal field across channel determines source-to-drain current flow
6. pMOS switching behavior device will be on = closed, when Vin > VDD - |Vtp| and will be off = open, when Vin < VDD - |Vtp|
7. 'source' is at lowest potential for nMOS and highest potential for pMOS
8. Logic gates are created by using sets of controlled switches. nMOS acts like an assert-low switch and pMOS acts like an assert-high switch
9. CMOS is inherently Inverting logic,
10. CMOS Transmission Gates , capable of passing both '1' and '0'

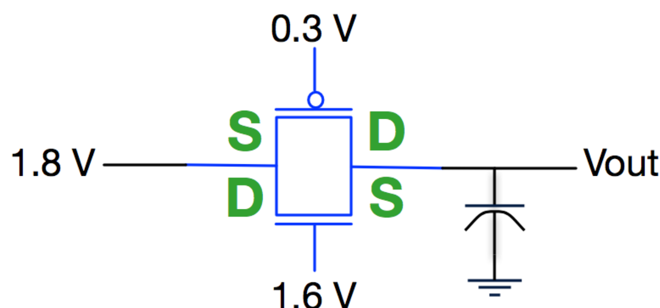
Question 2 (10 pts)

A. what function does this below circuit represent? **(2 pts)**



ANSWER: **3-INPUT -NAND**

B. In this transmission gate, Vout is initially discharged to 0 Volts. Given: V_{tN} = 0.5V, V_{tP} = -0.6V. Mark in the designated boxes the source and drain for each device **(2 pts)**



C. arrange the terms VOHmin, VIHmin, VILmax and VOLmax, and arrange them from lowest value to highest value. **(2 pts)**

$$V_{OLmax} \leq V_{ILmax} \leq V_{IHmin} \leq V_{OHmin}$$

D. Answer the following questions based on the circuit shown . **(4 pts)**

a) If Vx = 0V, what logic function is implemented?

ANSWER: **INV**

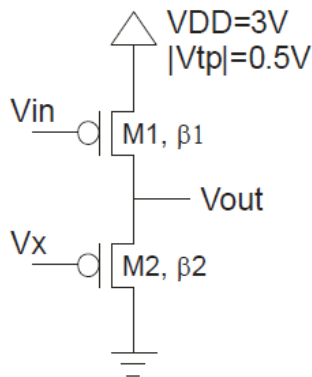
b) What is V_{OL} if Vx = 0V?

ANSWER: V_{OL} = **0.5** V

C) How can this circuit be modified to maximize the output voltage swing (i.e., get V_{OH} close to 3V and V_{OL} close to ground)? Explain briefly
i) in terms of size parameter (W, L) for transistors M1 and/or M2?
V_{OL} = |Vtp|, can not be changed
V_{OH} can be raised by decreasing the W/L ratio of M2 or increasing W/L of M1

ii) Are there any other circuit parameters that can be modified to improve output voltage swing?

Increasing Vx (> 0V) will make current in M2 weaker and allow V_{OH} to go higher.



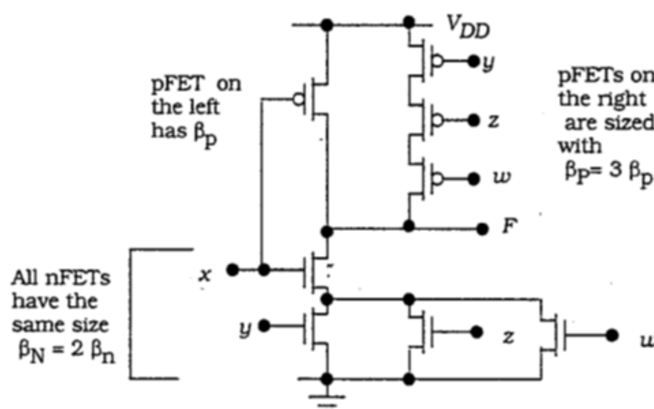
Question 3 (10 pts)

Transmission gates circuits used extensively in CMOS, good switch, can pass full range of voltage (VDD-ground)

A. How does the Pass gate Formed ? how do you connect the nMOS and pMOS to form a pass gate ? ***(1 pts)***

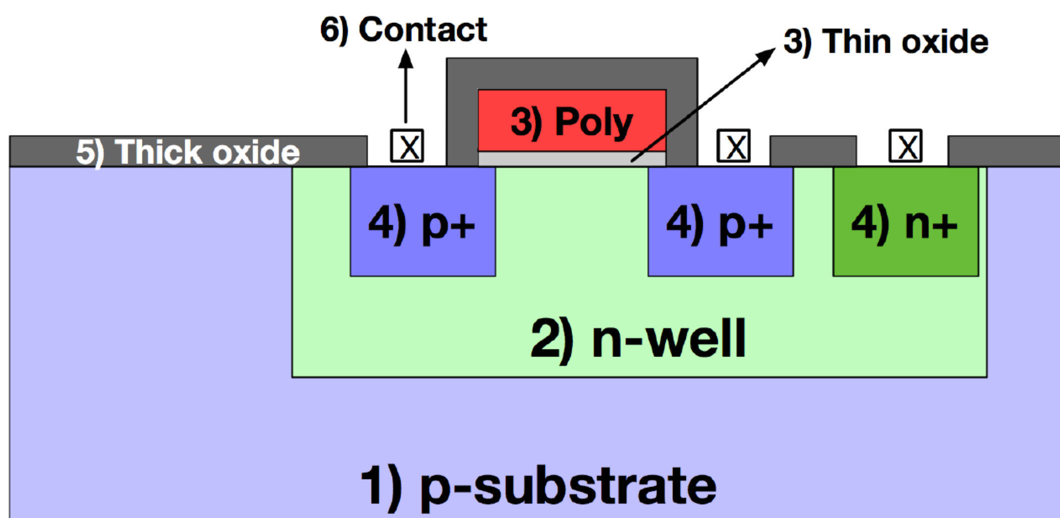
by a parallel nMOS and pMOS

B. Given the circuit as shown below, size the device assuming an inverter sizes are Bn for NMOS device size and Bp for PMOS size. ***(4 pts)***



C. List the steps required for creating a PMOS transistor, and draw a cross-section of the PMOS transistor, labeling each layer/feature in the order fabricated. **(5 pts)**

The steps below assume that a p-type substrate and positive photoresist is used.
1. Expose the substrate to oxygen (and hydrogen) at very high temperatures to form silicon dioxide
(SiO_2) layer. This is thick oxide.
2. Deposit photoresist.
3. Cover the photoresist with a mask which exposes those areas where n-well is to be created.
4. Expose to UV light.
5. Remove the exposed photoresist by dissolving.
6. Etch the surface to remove the portions of SiO_2 not covered by photoresist.
7. Strip off remaining photoresist.
8. Use *n* ion implantation to form n-wells in the areas without SiO_2.
9. Cover the whole surface with thin oxide and polysilicon.
10. Selectively remove thin oxide and poly from everywhere except for transistor gates.
11. Use *p+* ion implantation to form sources and drains of PMOS transistors.
12. Use *n+* ion implantation to form ntaps.
13. Cover the whole surface with thick oxide.
14. Selectively remove thick oxide from the source, drain and body (n-tap). This forms contact cuts.



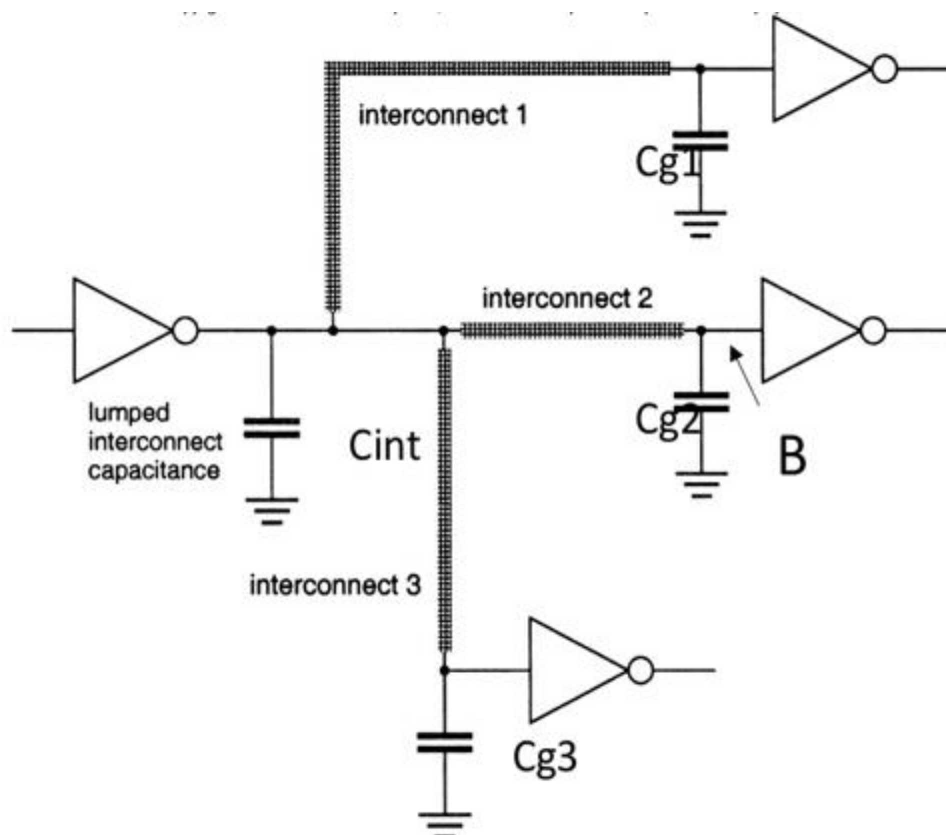
Question 4: *(10 pts)*

A) Where do we find thin oxide in a CMOS circuit? Why don't we use thick oxide? *(3 pts)*

Thin oxide is found under the polysilicon gate regions of any transistor.
Since its thickness is small, gate capacitance is higher. This allows better charge attraction to quickly form the inversion channel between source and drain.

B) Compute the worst-case rising and falling RC time constants at point B of the circuit below using the Elmore delay method. Assume all transistors **are unit sized** and wire **capacitance is lumped**. *(7 pts)*

Assume **Rchn** = 2000 ohms. **Rchp** = 8604 ohms, Cg(n+p) = 20 ff, Cd(n+p) = 20ff, and Cint = 10 ff.
Rint for interconnect1 is 10 ohms, interconnect2 is 5 ohms, and interconnect3 is 7 ohms.
Hint: Note that interconnect **capacitance is lumped at the beginning**, so we don't need to consider it separately for the 3 wires



Recall that channel resistance is inversely proportional to beta. So:

$$\frac{R_{chp}}{R_{chn}} = \frac{\beta_n}{\beta_p}$$

Note that interconnect **capacitance is lumped at the beginning**, so we don't need to consider it separately for the 3 wires.
Following is the circuit for falling delay at B:
Falling Elmore delay at B = $2000 \times 20 + 10 + 20 + 20 + 20 + 5 \times 20 = \mathbf{0.1801}\ \boldsymbol{ns}$
For rising delay at B, the circuit is the same except that Rchn is replaced with Rchp and the leftmost Gnd
symbol is replaced with Vdd.
Rising Elmore delay at B = $8604 \times 20 + 10 + 20 + 20 + 20 + 5 \times 20 = \mathbf{0.77446}\ \boldsymbol{ns}$