Final Project Grading Sheet 100

**Project:**

Design of a cutting-edge chip. Teams of 3 students undertake a large circuit design problem, going from specification to VLSI implementation while optimizing for speed, area, and/or power. Group collaboration and engineering design

**GRADES:** Grading is based upon the following factors

* In-class presentations
* final project report
* Technical competency in pursuing project goals
* Proficiency in collaboration, as measured by overall project integration and success.

**Designers:**

**Checkoff:**

* Project Meets Specifications \_\_\_\_ / 5
* Schematic Quality \_\_\_\_ / 5
* Layout Quality \_\_\_\_ / 5
* Implementation
  + DRC \_\_\_\_ / 5
  + Test Cases \_\_\_\_ / 5
  + Simulation \_\_\_\_ / 5
* **Total \_\_\_\_ / 30**
* **Presentation -------/20**

**Final Report -IEEE format**

Functional Overview \_\_\_\_ / 3

clear to other engineers

design Pinout \_\_\_\_ / 1

labeled with pin names, input/output/bidir

Floorplan \_\_\_\_ / 5

captions and dimensions of final

design, relation to original floorplan,

explanation of discrepancies

Area and Design Time Data \_\_\_\_ / 5

table listing area and design time for each cell in the design

Simulation Results \_\_\_\_ / 5

description of simulations performed

include a few pages of key waveforms

convince reader design works

estimate maximum operating speed

Verification Results \_\_\_\_ / 2

Schematics / Verilog \_\_\_\_ / 2

complete set of drawn schematics

and Verilog for synthesized blocks

legible and well-commented

Layout \_\_\_\_ / 2

complete set of color layout

clean and efficient

Writing quality \_\_\_\_ / 6

Clarity, organization, grammar, brevity

report submitted in WORD/IEE form \_\_\_\_ / 5

area optimization \_\_\_\_ / 3

Timing/speed \_\_\_\_ / 3

collaboration (if applicable) \_\_\_\_ / *3*

Conclusion -------/3

References ------/3

**Total \_\_\_\_ / 50**