A
Minor Project Report
On

"HIGH SPEED COMPARATOR FOR ADC USING MICROWIND SOFTWARE IN VLSI"

Submitted to

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI

In partial fulfillment of requirement for the award of degree

of

Bachelor of Engineering [VII semester]

In

Electronics and Telecommunication Engineering

By

Miss. ISHITA MISHRA

Mr. VICKY SHARMA

Miss. JYOTI BAGHEL

Under the Guidance of

Prof. ANANT G. KULKARNI
Reader

Department of Electronics and Telecommunication Engineering
RUNGTA ENGINEERING COLLEGE,
Near Nandanvan, Raipur (CG)- 492099

www.rungta.ac.in

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Department of Electronics and Telecommunication Engineering
RUNGTA ENGINEERING COLLEGE,
Near Nandanvan, Raipur (CG)- 492099
www.rungta.ac.in

D E C L A R A T I O N

I the undersigned solemnly declare that, the report of the project work entitled "**HIGH SPEED COMPARATOR FOR ADC USING MICROWIND SOFTWARE IN VLSI**." is based on my own work carried out during the course of my study under the supervision of **Prof. Anant G. Kulkarni**.

I assert that, the statement made and conclusions drawn are an outcome of the project work. I further declare that to the best of my knowledge and belief that the report does not contain any part of any work which has been submitted for the award of any other degree/diploma/certificate in this university or any other university.

_____

(Signature of the candidate)
Name :
Miss ISHITA MISHRA
Roll No.-3972811019
Enrollment No.- AJ3090

_____

(Signature of the candidate)
Name :
Mr.VICKY SHARMA
Roll No.-3972811041
Enrollment No.-AJ3253

_____

(Signature of the candidate)
Name :
Miss JYOTI BAGHEL
Roll No.-3972811023
Enrollment No.-AJ3152

Department of Electronics and. Telecommunication Engineering
RUNGTA ENGINEERING COLLEGE,
Near Nandanvan, Raipur (CG)- 492099
www.rungta.ac.in

C E R T I F I C A T E

This is to certify that, the report of the minor project submitted is an outcome of the project work entitled "**HIGH SPEED COMPARATOR FOR ADC USING MICROWIND SOFTWARE IN VLSI** " Carried out by **Miss ISHITA MISHRA bearing Roll No 3972811019 and Enrollment No AJ3090 , Mr VICKY SHARMA bearing Roll No 3972811041 and Enrollment No AJ3253, Miss JYOTI BAGHEL bearing Roll No 3972811023 and Enrollment No AJ3152** under my guidance and supervision for the award of B. E. VIII Semester in Electronics and Telecommunication Engineering of Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.), India.

To the best of my knowledge the report,

1. Embodies the work of the candidate him/herself.
2. Has duly been completed.
3. Fulfils the requirement of the ordinance relating to the B.E. degree of University and,
4. Is up to the desired standard for the purpose of which is submitted.

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(Signature of the Project Coordinator)	(Signature of the Guide)
Prof. Sandeep D. Bhad	Prof. Anant G. Kulkarni
Asst. Professor, ET&T	Reader

The project work as mentioned above is hereby being recommended and forwarded for examination and evaluation.

Prof. Sanjeev M. Ranjan

Head, ET&T

(Signature of head of the department with seal.)

epartment of Electronics and Telecommunication Engineering
RUNGTA ENGINEERING COLLEGE
Near Nandanvan, Raipur (CG)- 492099
www.rungta.ac

CERTIFICATE BY THE EXAMINERS

This is to certify that the project work entitled "HIGH SPEED COMPARATOR FOR ADC USING MICROWIND SOFTWARE IN VLSI " Submitted by:

Sr. No	Name of the Student	Roll No.	Enrollment No.
1	Ms. ISHITA MISHRA	3972811019	AJ3090
2	Mr.VICKY SHARMA	3972811041	AJ3253
3	Ms.JYOTI BAGHEL	3972811023	AJ3152

Has been examined by the undersigned as a part of the examination for the award of Engineering degree in Electronics and Telecommunication Engineering of Chhattisgarh Swami Vivekanand Technical University, Bhilai (C.G.), India.

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Internal Examiner External Examiner

Date: Date:

..

A C K N O W L E D G E M E N T

This Project work has been carried out to meet the academic requirements Of Chhattisgarh Swami Vivekanand Technical University Bhilai, for the completion of Bachelor of Engineering in Electronics and Telecommunication Engineering. I would like to put on record, my appreciation and gratitude to all who have rendered their support and input. Without them, it would not have been possible for me to shape this study.

I have received immense guidance from my guide **Prof. Anant G. Kulkarni, Reader, ET&T**. I would therefore like to convey my sincere gratitude to him.

Besides, I would like to extend my gratitude and appreciation to Prof.Anant.G.Kulkarni for all their support and guidance. I would like to thank them immensely for providing me the conceptual and theoretical concept. I would like to mention another person who has always showed great zeal in helping me. I thank **Prof. Anant G. Kulkarni** for all his willingness to help me. I thank him for and finding time to share his ideas, while I was busy putting up my project into its final shape.

I wish to express my sincere gratitude to **Dr. Saurabh Rungta**, Director (Technical), and **Prof. (Dr.) Pankaj Kumar,** Principal and **Prof. Sanjeev M.Ranjan** , Head, ET&T, REC, Raipur .

I also wish to express my gratitude to all the faculties & staff members of Electronics & Telecommunication department who rendered their help during the period of my project. Last but not least I wish to avail myself of this opportunity, express a sense of gratitude and love to my friends and my beloved parents for their manual support, strength, and help and for everything.

ABSTRACT

A novel design of CMOS dynamic latch comparator with dual input single output with the differential amplifier stage is presented. The designed dynamic latch comparator is required for high-speed analog-to-digital converters to get faster signal conversion and to reduce the power dissipation, which is immune to noise than the previous works. The design and analysis of a latch comparator using charge sharing circuit topology is illustrated to achieve low power and high-speed operation. The proposed circuit is designed using 0.18μm CMOS process. The simulated results shows that 100 MHz clock frequency with the power supply voltage (VDD) 3.3V and input range 3.3V produce the desired output signal. The topology of the proposed design is able to minimize the propagation delay and power consumption with the improved performances than other research works.

Moreover, the different capacitor value and the transistor lengths produced the faster output, which is suitable for the successful operation of the ADC.

List Of Abbreviations

VLSI	Very Large Scale Integrated
PMOS	P-Type Mosfet
NMOS	N-Type Mosfet
CMOS	Complementry Mosfet
ADC	Analog to Digital Convertor
MOS	Mosfet
Vin	Input Voltage
Vout	Output Voltage
Vref	Reference Voltage
Vdd	Power Supply Voltage

List Of Symbols

μ	MICRO
m	METRES
v	VOLT
pF	PICO FARAD
mhz	MEGAHERTZ
n	NANO
α	ALPHA
β	BETA
λ	LEMBDA
ϒ	GAMA

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CHAPTER – I

INTRODUCTION

A comparator becomes the great electronic device, which widely used in the analog to digital converters and plays important role in high speed ADC. An important circuit that is used for transition the analog to digital signal is the comparator. In general, a comparator is a device, which compares two currents or voltages and produces the digital output based on the comparison. Many applications, such as analog to digital converters (ADCs), memory sensing circuits and recently also on chip transceivers are widely using comparators . In the last years, most of the researches focus on the comparator with low power consumption,simple thermal management and high efficiency. The growth of the portable electronic devices makes the power consumption is critical issue to circuit designers because the low power and high speed comparators are the main building block in the front end of the radio frequency receiver in the most of the modern telecommunications system .

Recently, most of the researchers have proposed the dynamic latch comparators based on the cross coupled inverters to provide the latching in order to force a fast decision due to the positive feedback commonly used in flash analog digital converters (ADCs) due to their high decision Speed.

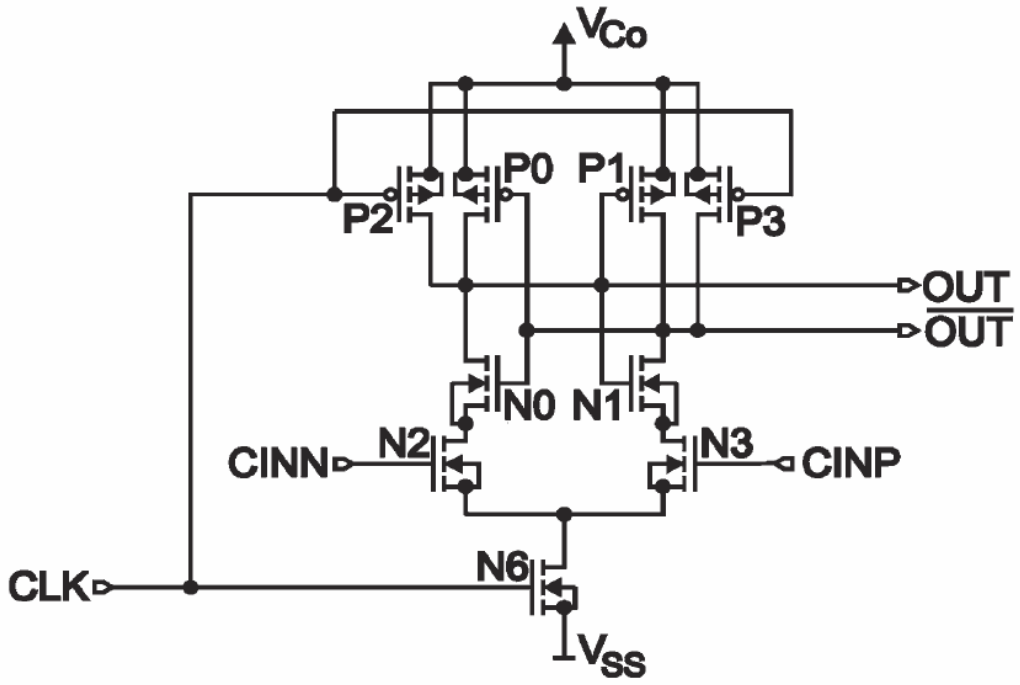

Fig.1.1 Conventional latch-type comparator.

Fig. 1.1 shows a widely used standard conventional latch type comparator circuit with the high impedance input, rail to rail output swing and no static power consumption .Robustness against noise and mismatch are the main advantages of the conventional latch type comparator .

However,it suffers from high sufficient power supply, which is caused by many stacked transistors in circuit design.

Goll and Zimmermann proposed a comparator with reduced delay time in 65nm CMOS using 0.65 V as the supply voltages as shown in Fig. 2 [1]. The proposed design is different from the conventional circuit by replacing a new latch for low power supply voltage operation, which offersthe great advantages of high impedance input, a rail to rail output swing, no static power dissipation and indirect influence of the parasitic capacitances of the input transistors to the output nodes.

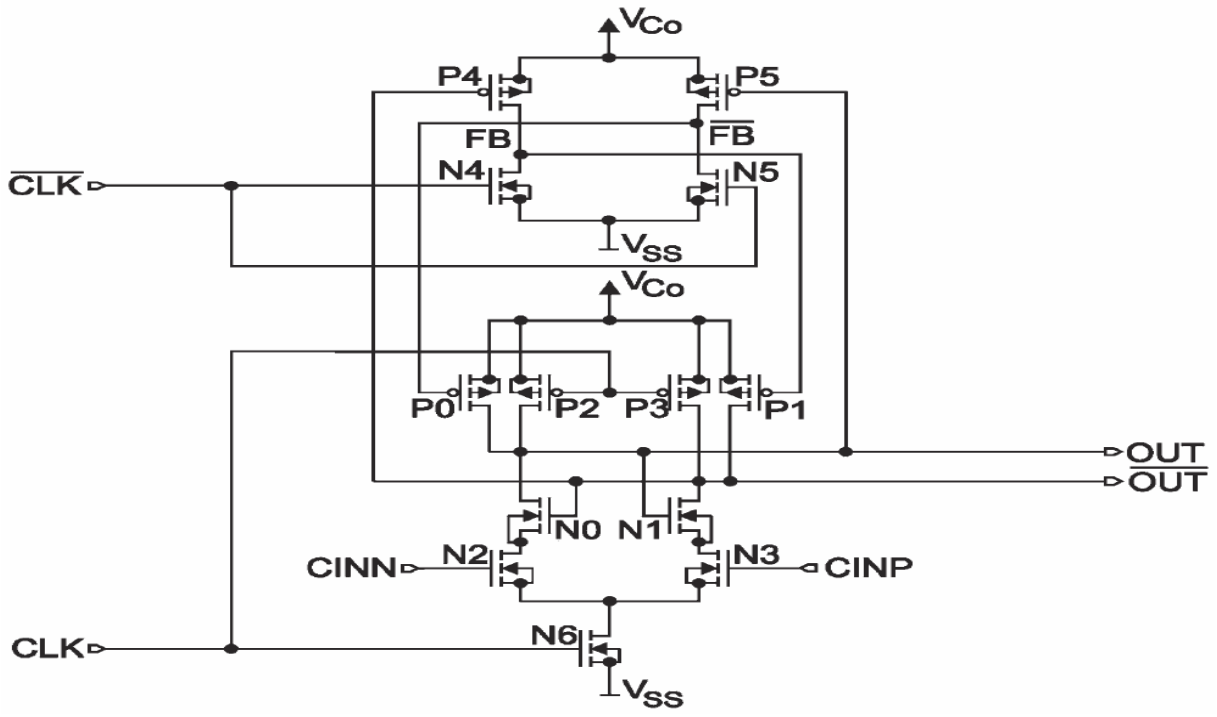

Fig.1.2. Comparator with modified latch.

A new CMOS dynamic latch comparator is presented. The fully dynamic charge sharing topology employed latch circuit with high input impedance. Moreover, a rail to rail output swing is produced with no static power dissipation. In addition, the proposed designed comparator is free from indirect influence of the parasitic capacitances of the input transistors to the output nodes. The design is optimized by choosing the right W/L ratio of the transistors in the circuit. The new design exhibits latched MOS transistors with faster output.

CHAPTER – II

LITERATURE REVIEW

S.NO.	TITLE	PUBLISED BY	YEAR
1.	Design and Analysis of Low Power and High Speed Dynamic Latch Comparator in 0.18 μm CMOS Process	Raja Mohd. Noor Hafizi Raja Daud, Mamun Bin Ibne Reaz, and Labonnah Farzana Rahman	November 2012
2.	Low Power CMOS Charge Sharing Dynamic Latch Comparator using 0.18μm Technology	Ili Shairah Abdul Halim Nurul Aisyah Nadiah Binti Zainal Abidin, A'zraa Afhzan Ab Rahim.	2011
3.	High-Speed And Low-Power Dynamic Latch Comparator	D. lackuline Moni and P. Jisha	2008
4.	Analysis of Power in Dynamic Comparators	Samaneh Babayan-Mashhadi, Mojtaba Daliri Reza Lotfi	2013
5.	High Resolution Low Power 0.6μm CMOS 40MHz Dynamic Latch Comparator	Carlos J Solis and Gladys O. Ducoudray	2010
6.	Design and Simulation of a High Speed CMOS Comparator	Smriti Shubhanand*, Dr. H.P. Shukla, and A.G. Rao	2013
7.	An Ultra-high-speed Comparator for ADC in 90nm CMOS Technology	Song Ye and Jie Wu	2009
8.	A Cmos Low-Power Low-Offset And High-Speed Fully Dynamic Latched Comparator	HeungJun Jeo and Yong-Bin Kim	2010
9.	Design of Low Power and High Speed CMOS Comparator for A/D Converter Application	Shubhara Yewale and Radheshyam Gamad	April 2012

CHAPTER – III

PROBLEM IDENTIFICATION

The problem is identified by this papers which are arranged in chapter 2 and the problem is given below:

PROBLEM:

The growth of the portable electronic devices makes the power consumption is critical issue to circuit designers because the low power and high speed comparators are the main building block in the front end of the radio frequency receiver in the most of the modern telecommunications system .

CHAPTER – IV

METHODOLOGY

The technology of scaling of MOS transistors improves the high speed and low power operation, the offset of the comparator in increased owing to transistor mismatch. Jungetal. proposed the low power and low offset comparator using latch load as shown in Fig.4.1, which using the dynamic offset cancellation and latch load is to reduce the power consumption and offset voltage of the comparator [1]-[3].

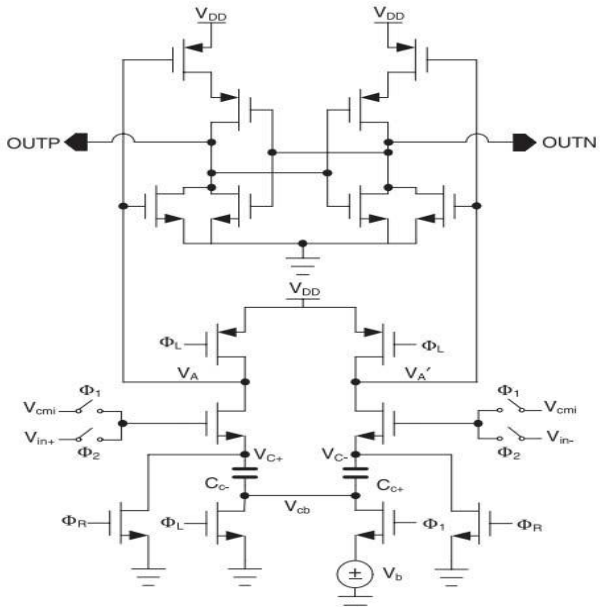

Fig.4.1. Low power and low offset comparator using latch load

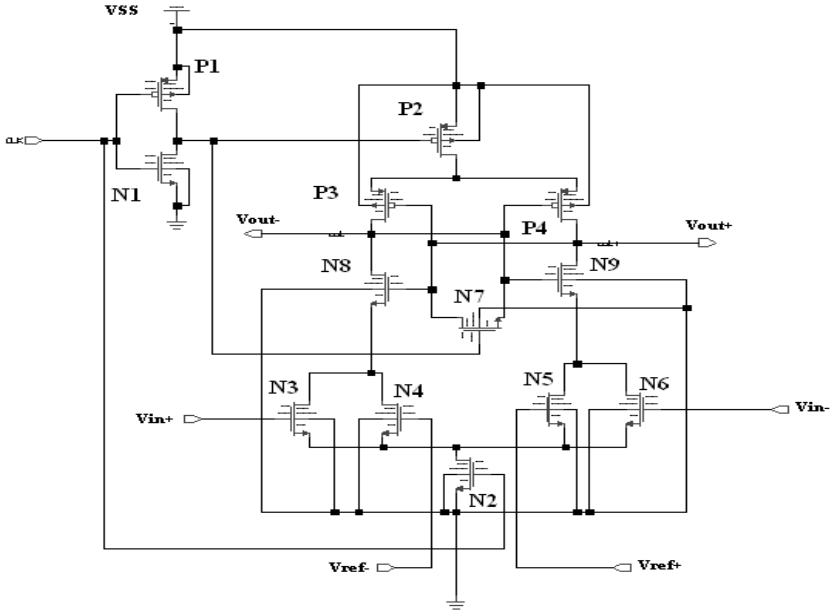

Fig. 4.2. Proposed design of comparator circuit.

The topology of the proposed comparator circuit as shown in Fig.4.2 describes about the charge sharing comparator combines the positive features of the previously designed dynamic latch comparator, which can be used in pipeline A/D converter. The proposed designed dynamic latch comparator is the combination of resistive dividing comparator and differential current sensing comparator. The complete layout of proposed designed comparator circuit is shown in Fig.4.3 using the CEDEC 0.18 um CMOS process. The layout area of the circuit is minimized by sharing the drain and source connection between the MOSFETs. The capacitors are not located in layout because to reduce the cost of the whole chip. Moreover, the capacitor is put in the test bench of the circuit.

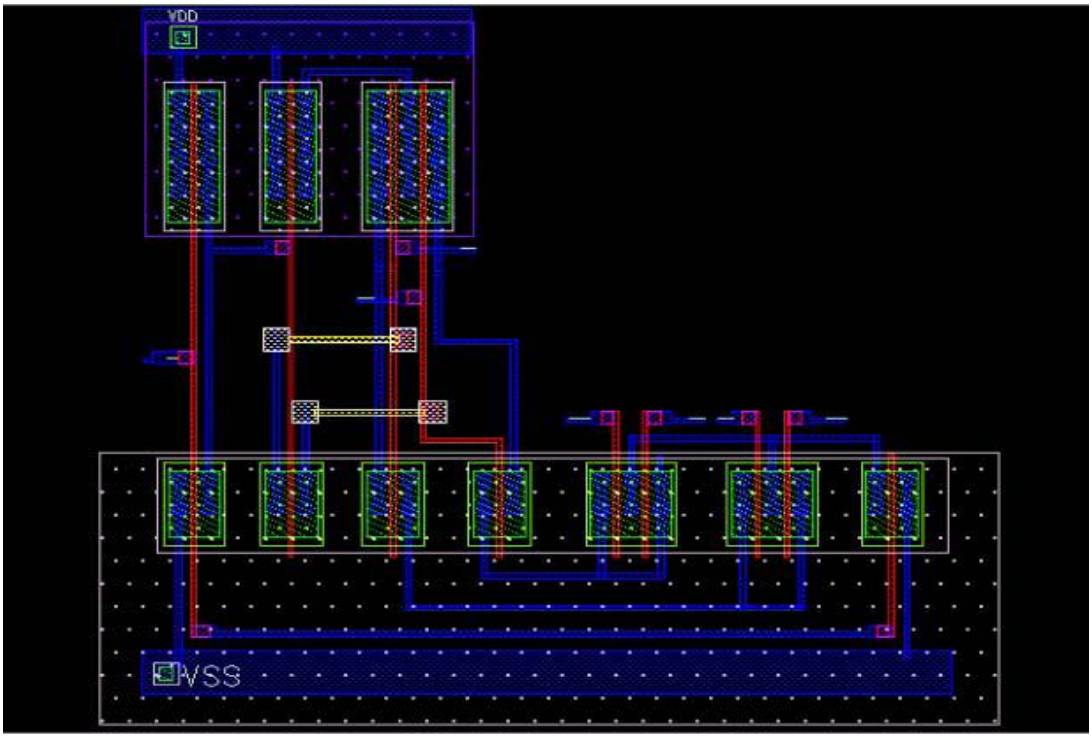

Fig.4.3. Layout of the proposed design.

CHAPTER – V

SIMULATION RESULTS AND DISCUSSION

CEDEC 0.18-μm CMOS process is used to measure the output results of the proposed dynamic latch comparator circuit with the ELDONET simulator. The input voltage Vin is set to 3.3 V and the reference voltage Vref is set to 1.65 V for simulating the outputs. 27oC operating condition is used for the proposed dynamic latch comparator circuit. The critical design parameters for designing the proposed CP circuit are listed in Table 5.1.

TABLE 5.1: MAIN DESIGN PARAMETERS

Parameters	Value
Voltage input (Vin)	3.3 V
Voltage reference (Vref)	1.65 V
All MOS Transistor length	0.18 μm
PMOS width	6 μm
NMOS width	3 μm

The basic comparison between the comparator waveforms should be functional. If the input of the comparator is greater than the reference voltage, Vref, then the output results will be a "1" and if the input voltage is less than reference voltage then the output voltage of the comparators produces output of "0." The waveform as shown at Figure 5.1 is the required function, which is efficiently be produced by the comparator. The most important dynamic parameters that determine the speed of a comparator are the propagation delay and the settling time.

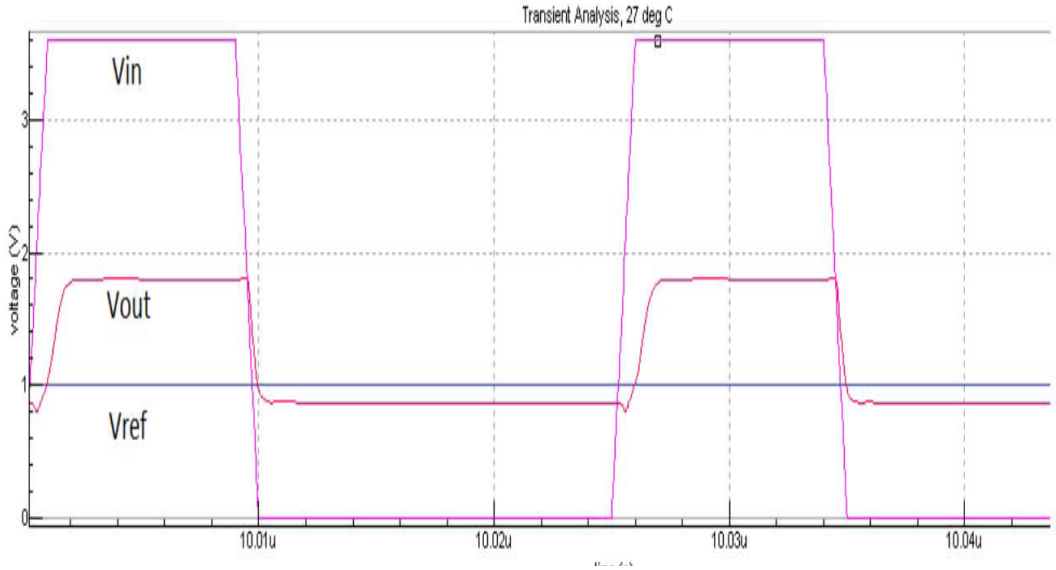

Fig.5.1.Comparator waveform in vin,vout and vref.

The simulated waveform, which is produced by the proposed dynamic latch comparator, is shown in Fig.5.2 and the width and the length of the transistor used in the design process of the comparator circuit is shown in Table II.

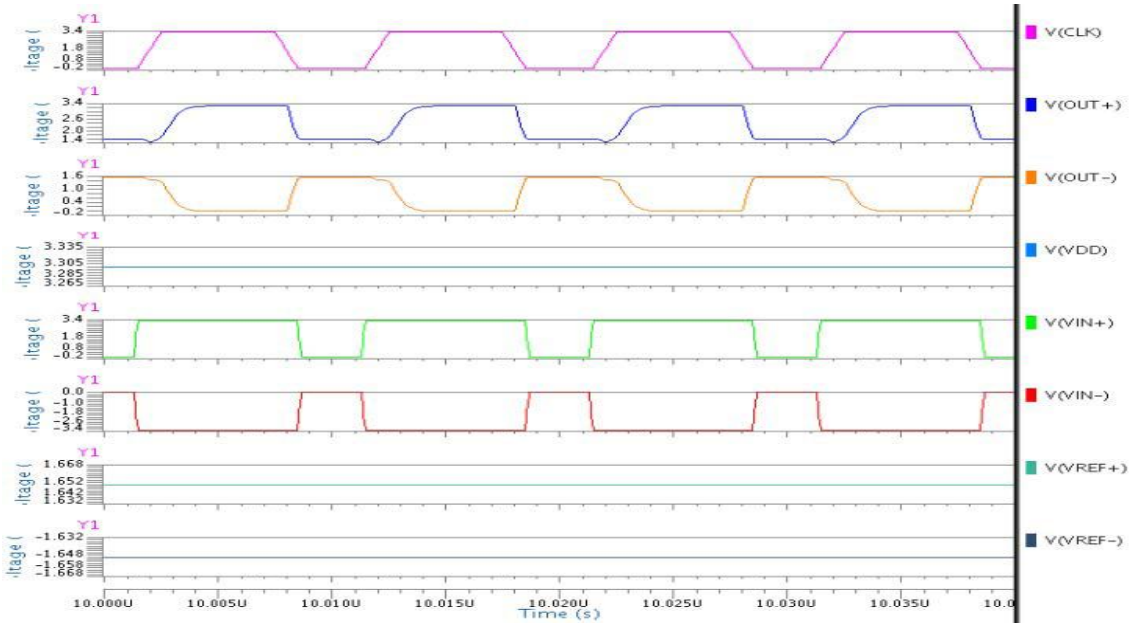

Fig.5.2. Simulation results of proposed design comparator.

TABLE 5.2. TRANSISTORS PARAMETERS FOR PMOS AND NMOS

Transistors	Length	Width
PMOS	**0.18 µm**	**6 µm**
NMOS	**0.18 µm**	**3 µm**

The operation process of the dynamic latch comparator to produce the output waveform is shown in Fig.5.3. The output voltage is changing from logic '0' to logic '1' when the input voltage Vin+ larger than reference voltage *Vref*+.

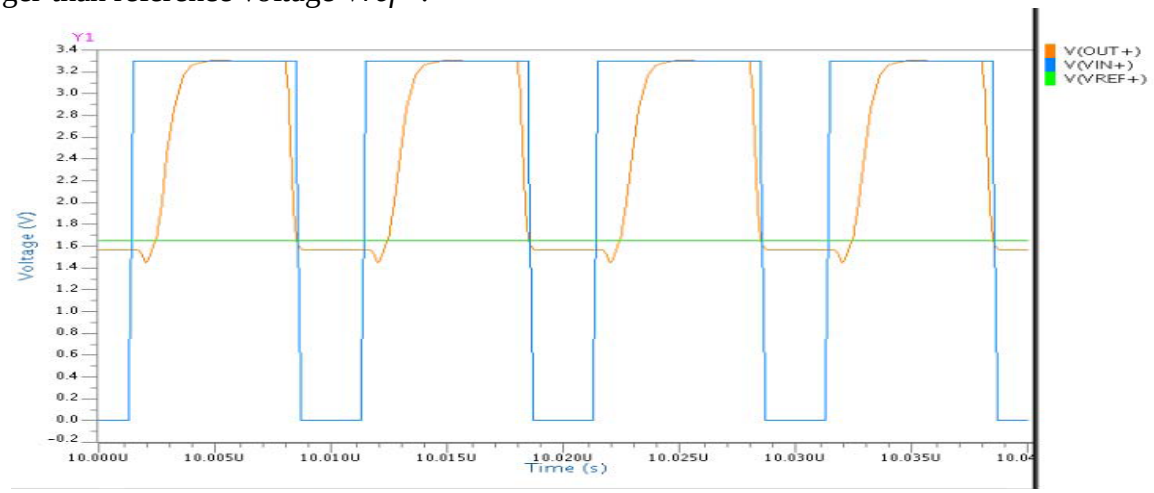

Fig. 5.3. The waveform of vout+ based on vin+ and vref+

On the other hand, when *Vref*+=*Vref*-=1.65V and *Vin*+=*Vin*-=3.3V are twice the *Vref* produced the waveform of the *Vout*+ along with the *Vout*- in square waveform is shown in Fig.5.4.

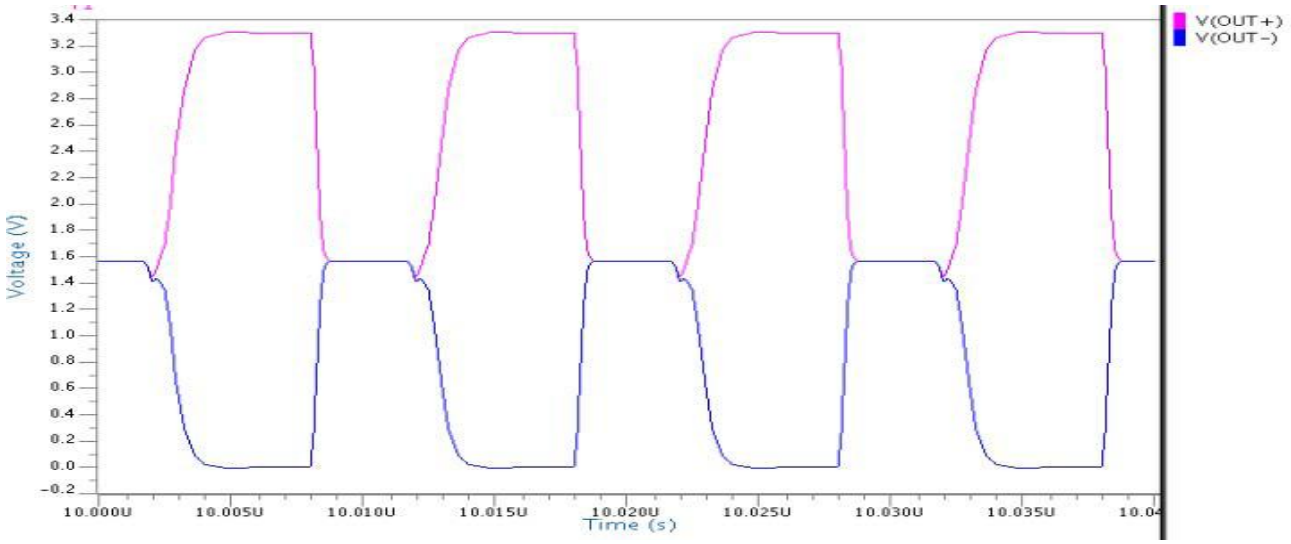

Fig.5.4. The waveform of dynamic latch comparator

The load capacitor significantly reduces the noise at the output voltage because it acts to remove the ripple from the power supplies and to store energy or electrical charge. Moreover, capacitor is used to resist any change of voltage across due to capability to store a charge and gives the output voltages waveform smoother. Fig.5.5. shows the faster output waveform with small value of the capacitor, which is produced when the value of the capacitor is decreased. Hence, the proposed designed dynamic latch comparator uses 0.5pF capacitor as load.

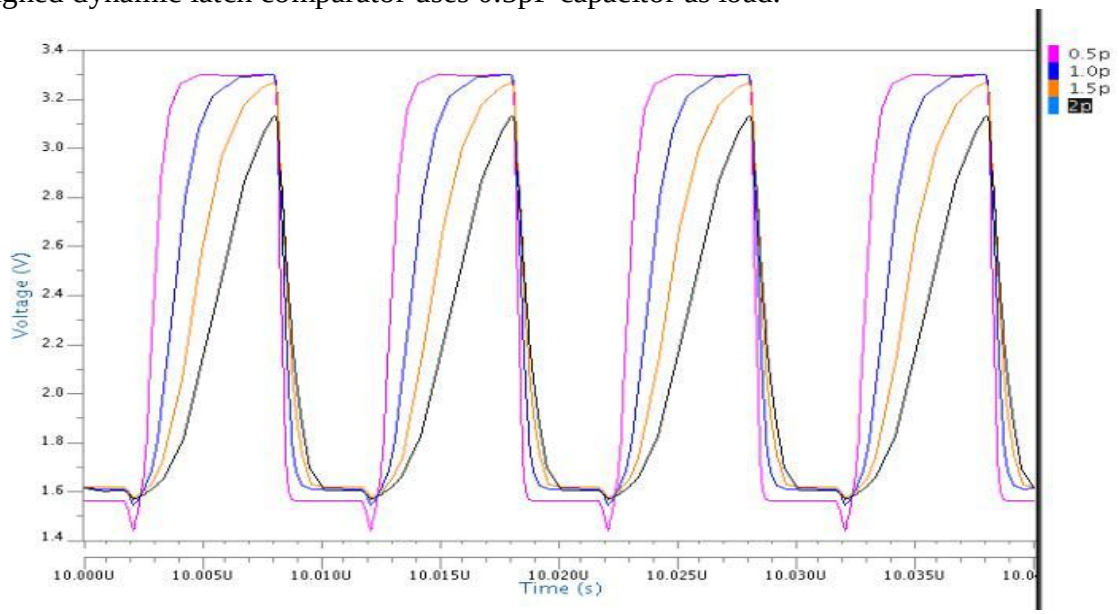

Fig.5.5.1. Output waveform with different capacitor value.

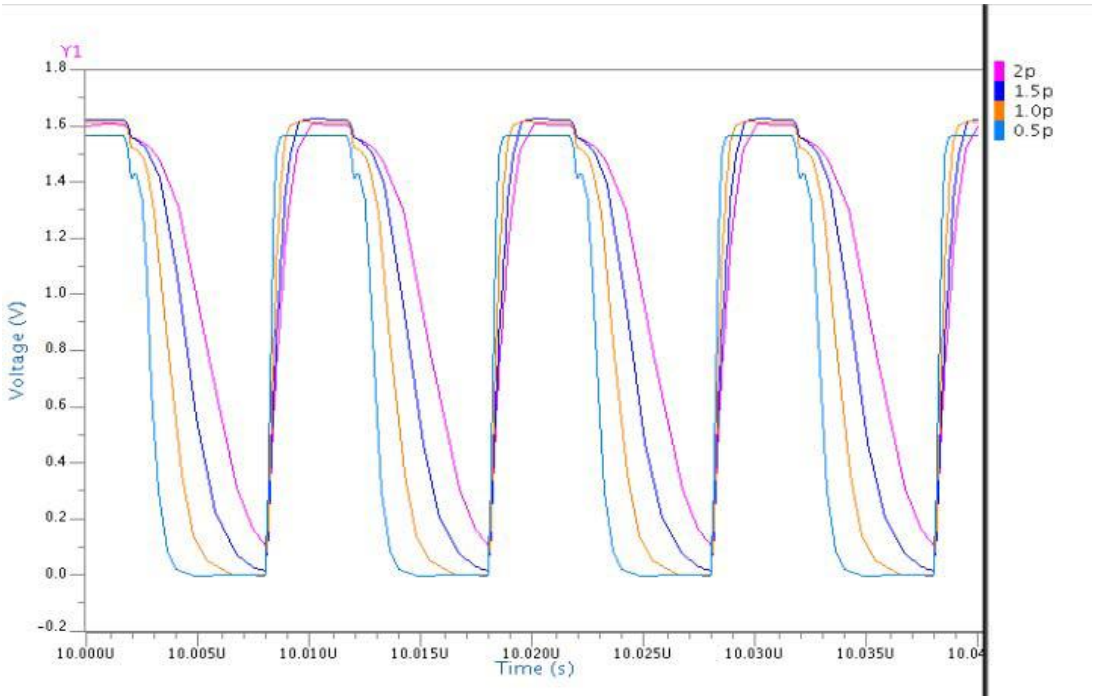

Fig.5.5.2. Output waveform with different capacitor value.

The length of the MOS transistors also influences the capability of the comparator to generate the faster output. The waveform output with different length of transistors is shown in Fig.5.6. The smaller length 0.18 um will produces the faster output with higher speed due to less propagation delay compared to the 0.20 um, 0.22 um and 0.24 um. All the PMOS and NMOS transistors used in the proposed designed is 0.18um. Although the smaller width of transistors will reduce comparator operation speed but the area can be reduced to more compact and low cost.

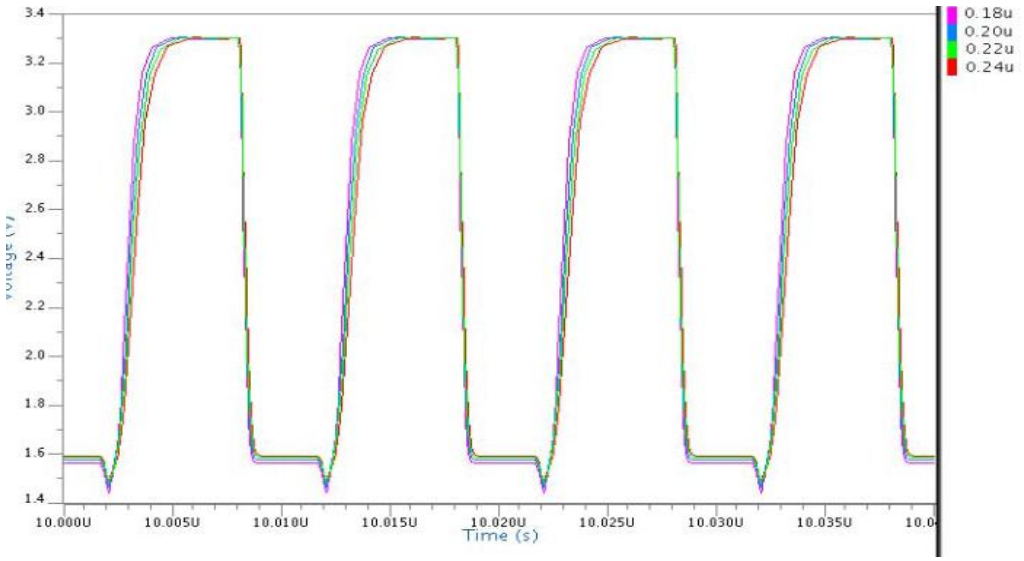

Fig.5.6.1. Simulated output waveform with different length transistors

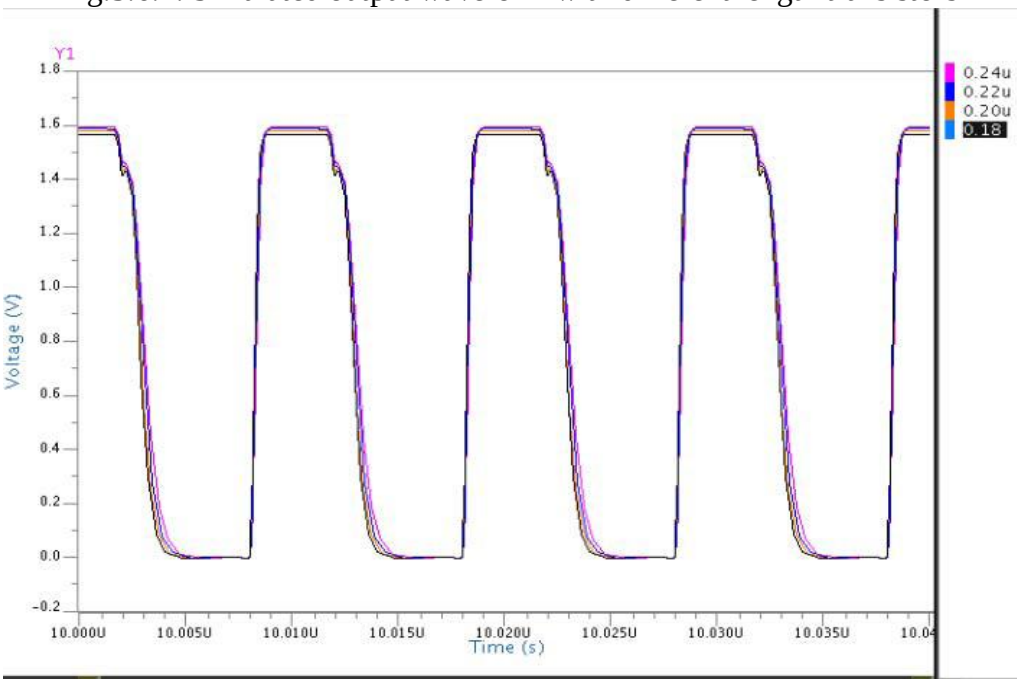

Fig.5.6.2. Simulated output waveform with different length transistors

CHAPTER – VI

CONCLUSION AND SCOPE OF FURTHER WORK

A new dynamic charge sharing topology is used to optimize the parameters for high speed applications.Designing dynamic latch comparator has its own pros and cons where optimization of one or more parameters may easily result in degradation of others. The main challenge lies on the constant speed, which makes more critical. In this paper the faster speed has been gained by the proposed designed dynamic latch comparator with the combination of resistive dividing comparator and differential current sensing comparator. The simulated output showed that the proposed designed dynamic latch comparator is able to produce higher speed with the power supply voltage 3.3 V. The proper scaling of MOS transistors provides the high speed and low power dissipation. Moreover, the smaller value of the capacitors and length of MOS transistors makes the novel designed dynamic latch comparator compatible for higher speed ADC applications.

In future , the scope of this comparator is that in this we add the ADC(analog to digital convertor) for betterment in this high speed comparator.

REFERENCES

[1] Book: VLSI design by V.S.BAGAD

[2] B. Goll and H. Zimmmermann, "A Comparator with Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65V," IEEE Transactions on Circuits and System II: Express Brief, vol. 56, no. 11, pp. 810-814, Nov 2009.

[3] Y. Guo, W. Cai, and T. Lu, "A Novel 1GSPS Low offset Comparator for high speed ADC," *in Proc. Fifth International Joint Conference on INC,IMS and IDC*, Seoul, Korea, Aug. 25 -27, 2009, pp. 1251–1254.

[4] Y. Jung, S. Lee, J. Chae, and G. C. Temes, "Low-power and low-offset comparator using latch load," *Electronics Letters*, vol. 47, no. 3, pp. 167-168, Feb. 2011.

[5] M. Miyahara and A. Matsuzawa, "A low-offset latched comparator using zero-static power dynamic offset cancellation technique," in *Proc. IEEE Asian Solid State Circuit Conference*, Taipei, Taiwan, Nov.16-18, 2009, pp. 233–236.

[6] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise selfcalibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE Asian Solid State Circuit Conference (A-SSCC)*, Fukuoka, Japan, Nov.3-5, 2008, pp. 269–272.

[7] http://en.m.wikipedia.org/wiki/ comparator

[8] R. S. Gamad, S. Kale, "Design of a CMOS Comparator for Low Power and High Speed," *International Journal of Electronic Engineering Research*, vol. 2, 2010.

[9] P. Uthaichana and E. Leelarasmee, "Low Power CMOS Dynamic Latch Comparators," *IEEE*, pp. 605-608, 2003.

[10] Z. Huang and P. Zhong, "An Adaptive Analog-to-Digital Converter Based on Low-Power Dynamic Latch Comparator," *IEEE conference*,p. 6pp, 2005.