LOW POWER CMOS CHARGE SHARING DYNAMIC LATCH COMPARATOR USING 0.18µm TECHNOLOGY

Nurul Aisyah Nadiah Binti Zainal Abidin
Faculty of Electrical Engineering
Universiti Teknologi Mara
Shah Alam, 40450, Selangor, Malaysia
e-mail: aisyahnadiah@gmail.com

***Abstract*—This paper discusses the design and analysis of a latching comparator using charge sharing circuit topology for low power and high speed. This topology combines the good features of the resistive dividing comparator and the differential current sensing comparator. This design will be focusing on the minimization of propagation delay and the power dissipation of the comparator, which will improves the comparator performance. Simulation results have been obtained using 0.18µm technology, for a 100 MHz clocked comparator, considering 1.8V supply voltage and 1.8V input range. Design has been carried out in SILVACO EDA tool, the schematic simulation are using Gateway SILVACO EDA tool and layout simulation of design are verified using Expert SILVACO EDA tool.**

Keywords-component—ADC; charge sharing comparator; low power consumption.

I. INTRODUCTION

Comparators are used in A/D converter, switching power regulators, data transmission, and many other applications. The comparator design plays an important role in high speed A/D converters [1]. Comparator is the simplest circuit that moves signals between the analog and digital worlds and compares the difference between two inputs and produces relevant outputs. The speed, power consumption and chip area are the important factors while designing comparators. The ever-growing application of portable devices makes the power consumption a very critical constraint for circuit designers[1]. Low power consumption and high speed is important feature of many A/D converters design to reduce energy use or to minimize heat dissipation to lower cooling and packaging costs. Instead of using the traditional amplifier-chain type comparators, the dynamic latch comparators are applied in order to achieve low power dissipation beside achieving a smaller area by removing the pre-amplifying stage [2],[3]. This paper will focus on charge sharing comparator because this topology combines the good features of the other two of dynamic latch comparator that suitable with pipeline A/D converters which is resistive dividing comparator and differential current sensing comparator [2]. This paper compares the simulation result between the proposed designs of 0.18µm technology with the reference paper of low power CMOS dynamic latch comparator using 0.5µm technology which will minimize the size, delay and the power consumption of the comparator. So, the comparator will be more sensitive and comparing speed tends to be fast.

This paper is divided into four main parts. Section 2 is a methodology of the design of the comparator and overview of the waveform output. In section 3, simulation results and how to choose the parameter to get the low power and propagation delay are presented with the comparison to the previous work. Finally, a brief conclusion for the low power charge sharing dynamic latch comparator is presented in section 4.

II. DESIGN OF THE COMPARATOR

The flow chart on Fig. 1 shows the step to complete the designing of the low power CMOS charge sharing dynamic latch comparator using 0.18µm technology:

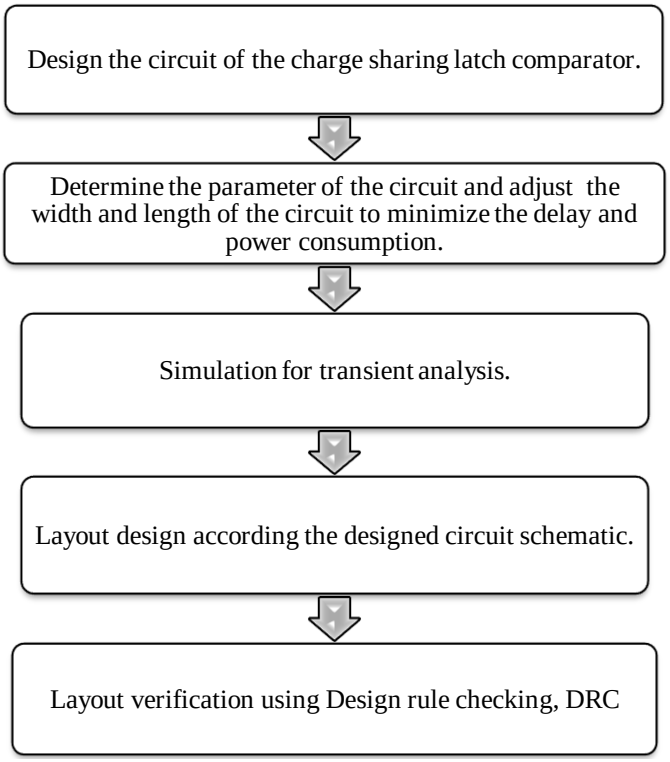

Figure 1. Flow chart of the project.

Fig. 2 shows the circuit topology of a new dynamic latch comparator. To give low power during the regeneration mode, a latch with resistive comparing circuits in series with NMOS is used. However, there is no PMOS precharging circuit and NMOS pass transistor M7 for output pass transistor is to equalize the two output voltages approximately $V_{DD}/2$ during the reset mode. This is possible because the latch is totally disconnected from both V_{DD} and GND by M11 and M10 when CLK is low[2].

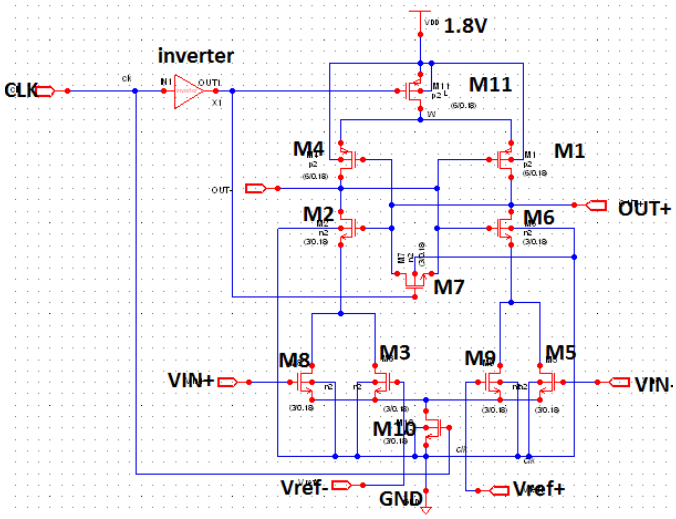

Figure 2. Proposed design of CMOS comparator

Fig. 3 shows the simulated output voltage waveform of this circuit when $V_{ref}+ = V_{ref}- = 0.9V$ and $V_{in}+ = V_{in}- = 1.8V$ is a square wave. The parameters of all the transistors are shows in Table I.

TABLE I. MOS PARAMETERS

	All PMOS	All NMOS
Width	6µm	3µm
Length	0.18µm	0.18µm

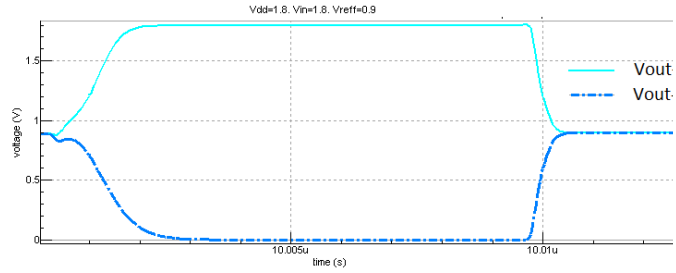

Figure 3. Charge sharing output voltage waveform

If the input of the comparator is greater than the reference voltage , V_{ref} it has to give an output of '1' and if the comparator input is less than reference voltage then the output of the comparator should be '0'. A simple comparator performs the required function efficiently as shows in the Fig. 4.

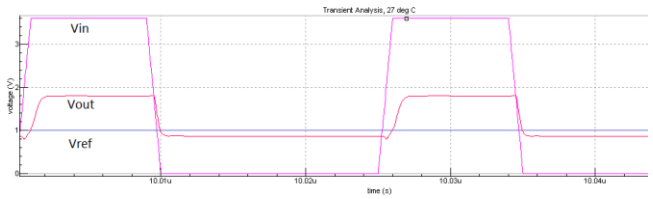

Figure 4. Waveform of the V_{in}, V_{ref} and V_{out} of the comparator

III. SIMULATION RESULTS AND DISCUSSION

Simulation of reported design is done using the 0.18 µm CMOS technology. In this project, 1.8V supply voltage is used for operation and clock period is 10ns. During the process, speed of the comparator is 100MHz. This design can be used where low power, high speed and low propagation delay are the main requirements. Finally simulation results of the comparator are shows in Fig. 5. The width of the transistor used is as in the Table I. This simulation result is compared to the previous work by[2]. Table III shows the comparison of present design results with previous work and got improvement in the present results.

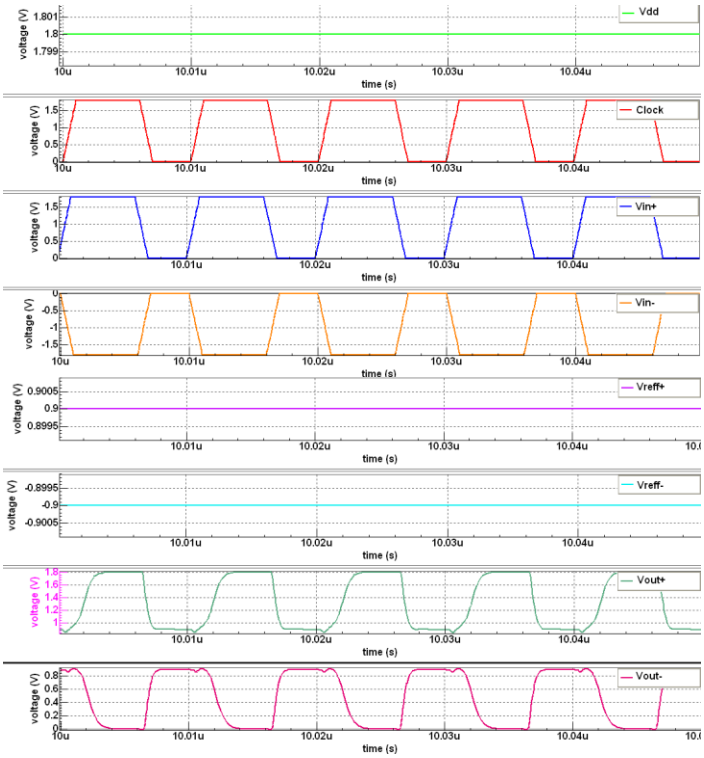

Figure 5. Simulation result of the charge sharing dynamic latch comparator

A. *Parameter choosen*

1) *Effect of the technology choosen*

This project use 0.18µm technology which is smaller length than technology used in the previous work by[2], so the minimum length for this project is 0.18µm. Simulation in the Fig. 6 shows that the smaller length will produce the higher speed due to less propagation delay compared to the 0.5µm and 1.0µm.

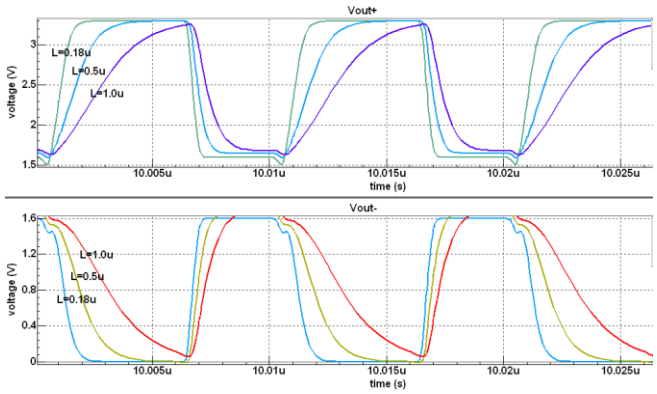

Figure 6. Output waveform when use different length

2) *Effect of the width of transistor*

The study reference paper use width of transistor for PMOS is 10µm and NMOS is 5µm. This paper proposes 6µm width for PMOS and 3µm width for NMOS, as shows in Fig. 7, the propose width produce the slower speed compared to the width of the previous work. Although the speed will be slower when using smaller width, but the area for this project will be smaller. Small area will reduce the cost of the comparator.

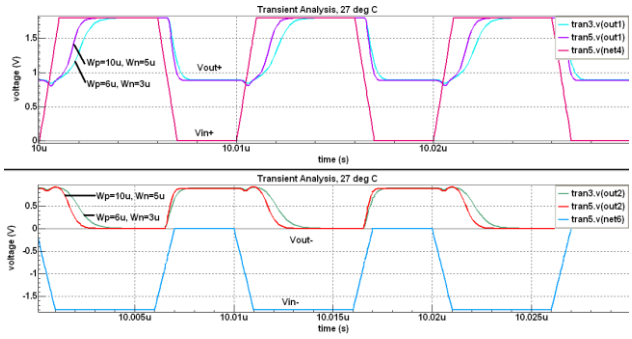

Figure 7. Output waveform when use different width

3) *Effect of the load capacitance*

Capacitor acts as filter to remove ripple from power supplies. The function of capacitor is to store electrical charge. Since it can store a charge and then release that charge, it can resists any change of voltage across it. As shows in Fig. 8 below, the smaller capacitor will produce the faster output. This situation is proved by the Eq. (1) which shows that time delay is proportional to the capacitor used. So, this paper chooses to use 1pF of capacitor as load. Capacitor is used to eliminate the offset voltage[4], Offset voltage should be small as possible to minimize the error voltage at the output of the comparator, especially for applications where small voltages are being amplified. In this project, the capacitor is connected at the V_{out}+ and V_{out}-.

$$\tau = RC \quad (1)$$

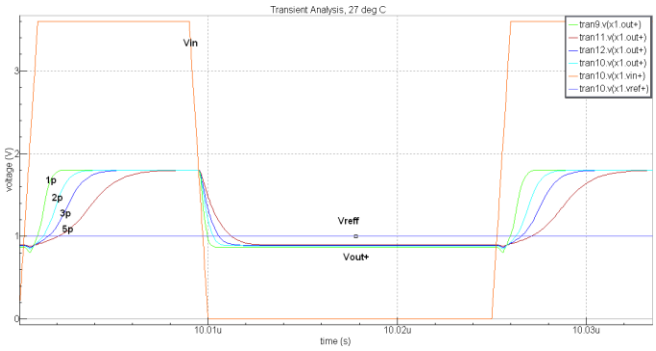

Figure 8. Output waveform with different load with V_{in} and V_{reff}.

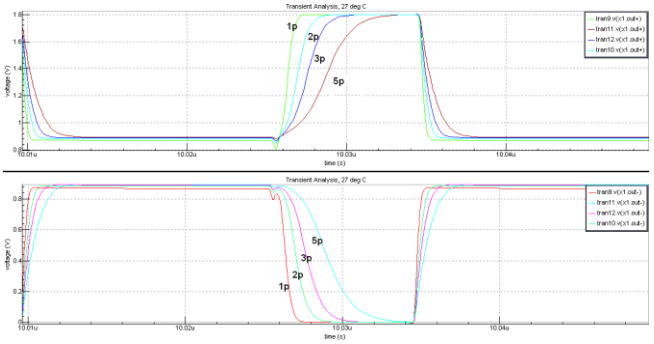

Figure 9. Output waveform when use different load

B. *Propogation delay of the comparator*

The most important dynamic parameters that determine the speed of a comparator are the propagation delay and the settling time [5]. Propagation delay is the amount of time that it takes for a change in the input signal to produce a change in the output signal [6]. The shorter propagation delay, the higher the speed of the circuit and vice-versa. For reducing delay and increase sensitivity, latched comparators are used. Delay time is measured at 50% transition of the point. The propagation delay is determined using two basic time intervals, which is t_{plh} and t_{phl}. t_{plh} is the delay time measured when output is changing from logic 0 to logic 1 and t_{phl} is from logic 1 to 0. The simulation results in Fig. 10 shows the propagation delay of the previous work which is 1.927ns while Fig. 11 shows the propagation delay of the present work which is 1.699ns. The comparison between previous and present work of the propagation delay are shows in Table II. The result shows that the propagation delay of the present work has reduce 12% compare to the previous work.

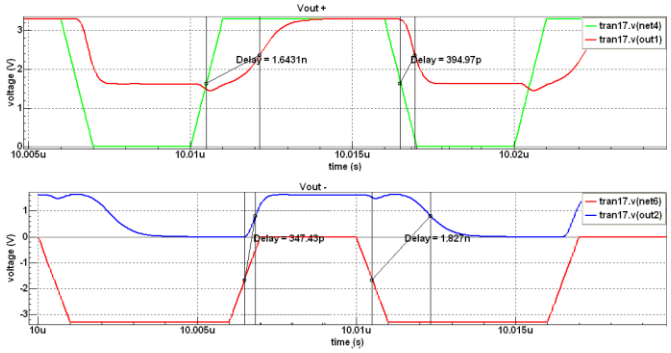

Figure 10. Propagation delay of the previous work

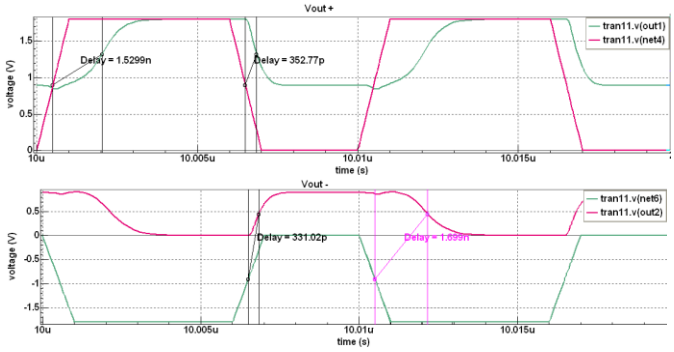

Figure 11. Propagation delay of the present work

TABLE II. COMPARISON BETWEEN PREVIOUS AND PRESENT WORK OF THE PROPAGATION DELAY.

		t_{plh}(s)	t_{phl}(s)
Previous work	V_{out}+	1.6431n	394.97p
	V_{out}-	347.43p	1.927n
Present work	V_{out}+	1.5299n	352.77p
	V_{out}-	331.02p	1.699n

C. *Power dissipation*

Power is secondary consideration behind speed and area for many chips [7]. Minimize power dissipation are very important nowadays to reduce cost, and reduce noise. Power dissipation is the wasted power in the form of heat, voltage drop. To determine the power dissipated by the comparator, sum of the currents supplied by the constant current sources, I_{DD} multiply with supply voltage, V_{DD} as in Eq.(2) [4]. The power P drawn from the power supply is proportional to the supply current I_{DD} and the supply voltage V_{DD}.

$$P = V_{DD} \times I_{DD} \qquad (2)$$

Fig. 12 shows the total current of the previous work and Fig. 13 shows the total current of the present work. From Eq. (2), the power dissipation of this comparator is calculated with 1.8V V_{DD} for the current work and the 3.3V for the previous work. The calculated power dissipation of previous work is 23.18nW and power dissipation of present work is 1.33nW which is 94% reduced from previous work.

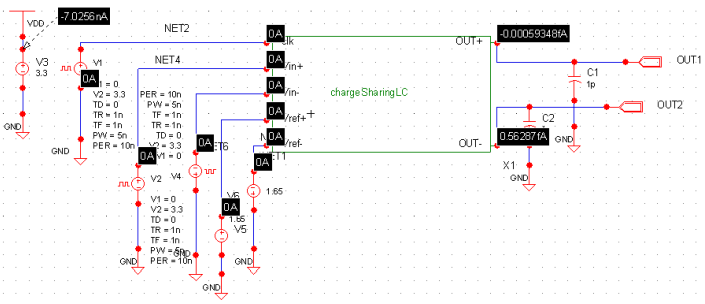

Figure12. Total current of the previous work.

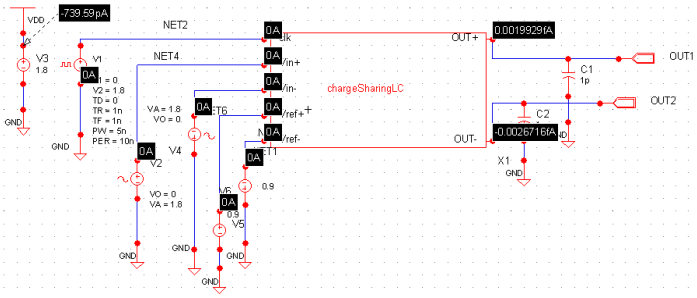

Figure 13. Total current of the present work.

D. Average dynamic power dissipation

Power average is the average amount of work done or energy converted per unit of time. The energy consumed over some interval time, T is the integral of the instantaneous power[7].

$$E = \int_0^T I_{DD}(t) V_{DD}\, dt \qquad (3)$$

The average dynamic power dissipation over this interval is shows in Eq. (4).

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T I_{DD}(t) V_{DD}\, dt \qquad (4)$$

The integral finds the average Current delivered by V_{dd}. In this project, power average are straightly find from the simulations by edit the SEdit as shows in Fig. 14 and the results of the average dynamic power dissipation are shown in Fig. 15 and 16. The average dynamic power dissipation of present work has reduced 82% compared to the previous work.

```
.measure tran pwr avg p(V3) from=0ns to=200ns
.print tran p(V3) power
```

Figure 14. SEdit for measure the average power

Index	meas23.pwr()
1	2.55761e-003

Figure15. Measured power of the previous work

Index	meas24.pwr()
1	4.58281e-004

Figure16. Measured power of the present work

IV. LAYOUT OF THE COMPARATOR

The layout of the complete low power CMOS charge sharing dynamic latch comparators using 0.18µm is shows in Fig. 17. The area of the layout is 54.57µm x 40.69µm. This layout minimizes area by sharing drain and source connections between MOSFETs. Fig. 18 shows the DRC of the layout with no errors.

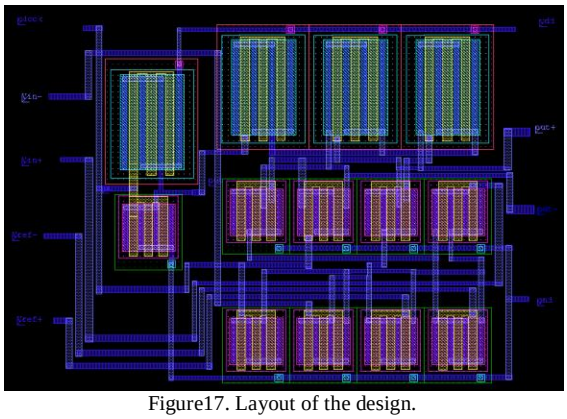

Figure17. Layout of the design.

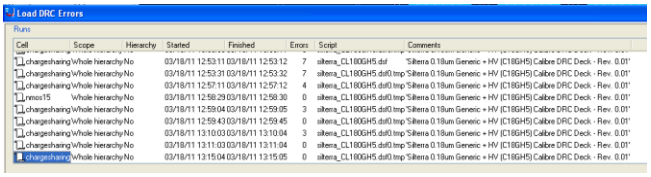

Figure18. DRC of the layout

V. CONCLUSION

This paper has presented the CMOS charge sharing dynamic latch comparator design and its simulation results of high speed, and low power by considering 1.8V power supply. Author have compared the results of the present work with earlier reported work and the improvements are shown in Table III. In conclusion, the proposed design reduces the power dissipation without deteriorating the comparing speed. From simulation result, the average dynamic power dissipation is reduced approximately 82%, while power dissipation reduced approximately 94% compared to the previous work and minimize the delay approximately 11%. The proposed design of the comparator runs faster and provides more stable output signal than the previous work with low supply voltage. For future development, 90nm technology can be apply to this charge sharing dynamic latch comparator to obtain lower power and higher speed.

TABLE III. COMPARISON OF THE PRESENT COMPARATOR DESIGN WITH THE PREVIOUS WORK.

	Previous work	Present work
Length	0.5µm	0.18µm
Wp/ Wn	10µm/5µm	6µm/3µm
Voltage supply	3.3V	1.8V
delay	1.827ns	1.699ns
Power dissipation	23.18nW	1.33nW
Average dynamic power dissipation	2.56mW	0.46mW

ACKNOWLEDGMENT

This work has been carried out in Microelectronic laboratory, Faculty of Electrical Engineering Universiti Teknologi MARA, Shah Alam, Malaysia. Authors are thankful to the Universiti Teknologi MARA for facilities provided and to Miss Ili Shairah Abdul Halim for her supervision in this project.

REFERENCES

[1] R. S. G. S.Kale, "Design of a CMOS Comparator for Low Power and High Speed," *International Journal of Electronic Engineering Research*, vol. 2, 2010.

[2] P. Uthaichana and E. Leelarasmee, "Low Power CMOS Dynamic Latch Comparators," *IEEE*, pp. 605-608, 2003.

[3] Z. Huang and P. Zhong, "An Adaptive Analog-to-Digital Converter Based on Low-Power Dynamic Latch Comparator," *IEEE conference*, p. 6pp, 2005.

[4] R. J. Baker, E. Institute of, E. Electronics, and I. S.-S. C. Society, *CMOS: circuit design, layout, and simulation*: IEEE Press, 2008.

[5] R. S. G. Meena Panchore, "Low Power and High Speed CMOS Comparator Design Using 0.18µm Technology," *International Journal of Electronic Engineering Research*, vol. 2, pp. 71-77, 2010.

[6] A. P. Godse and D. A. Godse, *Digital Systems Design - I*: Technical Publications, 2008.

[7] N. H. E. Weste and D. F. Harris, *CMOS VLSI design: a circuits and systems perspective*: Pearson/Addison-Wesley, 2005.