Area Efficient 4-Bit Full Adder Design

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Abstract

Area efficient ultra-low power CMOS digital integrated circuits are one of the emerging technologies for the modern portable systems. Requirement of fewer transistors on chip and less power consumption for the operation of these devices proves the efficiency of these systems. To achieve the efficiency of these devices in terms of area and power, we are on the way to design these devices by using Nano technologies. Higher functionally and higher performance of digital circuits at lower power consumption can also be achieved if the required output can be obtained by adding few more transistors in already used circuits in that device.

I. Introduction

Any digital circuit with power on whether performing its function or not, consumes power, which is dissipating as heat. Based on the process of power dissipation there are three major sources of power dissipation in CMOS circuits: firstly, static dissipation occurs due to the leakage current, subthreshold conduction, junction leakage and tunneling through gate oxides. In addition, dynamic dissipation caused by switching of transient current, and charging discharging of load capacitances. In addition, short circuit dissipations attributed to short circuit current that arises when pair of NMOS and PMOS transistors conduct simultaneously. In present day technology scenario due to the increased use of portable electronic devices, power and area efficiency has become a major concern for circuit designers. As direct implementation of area and power efficient technologies on designing platform cannot be cost effective so before actual implementation of these digital circuits on layout it is necessary to take estimation criteria in to consideration on transistor level designing. Therefore, there is a need of ultra-low power designing technology, which can reduce the power dissipation as well as area of the VLSI logic circuits. Digital circuits with area and power inefficiency have become one of the show stoppers in efficient development of Nano electronics digital circuits and main reason for this is reduced factor of lambda and increased number of functions on a same chip.

Project in its big picture is to see how small changes will affect the circuit to be much faster and less power consuming. In addition, because of Adder are used for many hours without breaks any good changes that made it faster will cause the whole average and performance to be much better and better.

II. Problem Statement

In this Project, we introduce new design and implementations of a 4-bit full adder design.

III. Methodology and Solution:

1.Xor Gate:

To build 4-bit adder with good area. We start thinking about basics and component for one-bit adder. one-bit adder It is built from Xor gate for sum and AND, OR gates for carry. Based on this information we have gone to build XOR gate in transistor level. First design we think about it is in figure 1.

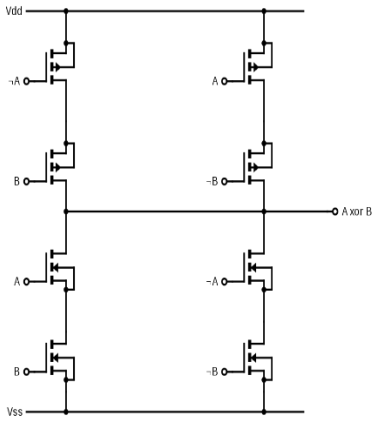

Figure 1:Xor gate 8 level transistor

As we note this design for XOR use 8 transistors, we think about optimized design so we go to search about design for Xor gate using a smaller number of transistors. Fortunately, we found many designs for Xor gate and we have tried many of them where we have encountered a lot of problems that we do not know the reasons but finally managed to apply one of these designs successfully. this design contains only three transistors as shown in figure 2, this may be will be best optimization for 4-bit-adder.

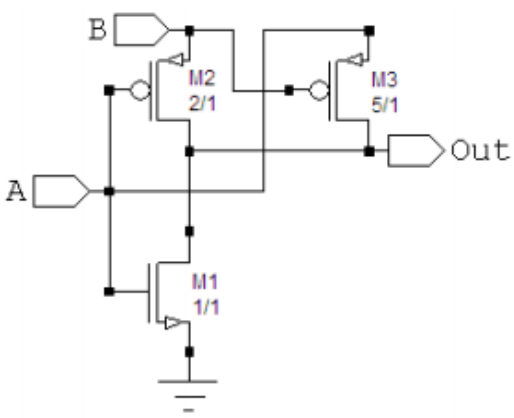

Figure 2:Xor gate three level transistor[ref1]

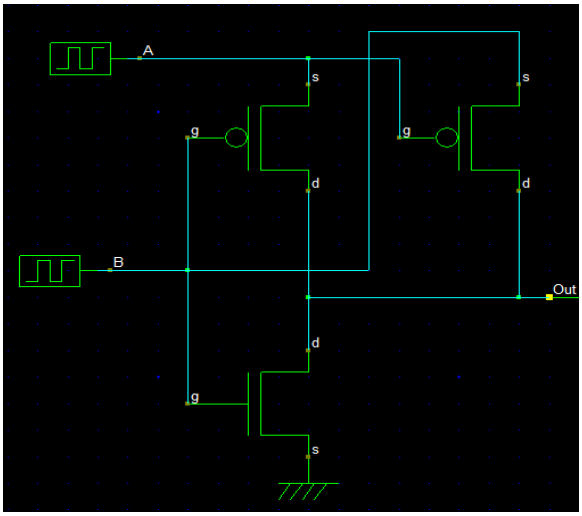

Figure 3: Xor gate three level transistor (our schematic).

This design named 3T XOR gate and work as like: When the input B is at logic high, the inverter functions like a normal CMOS inverter. There is threshold loss when input B is at logic low. When the input B is at logic low, the CMOS inverter output is at high impedance. Here, the pass transistor M3 is enabled and the output terminal Out will get the same logic value as input A. The operation of the whole circuit is thus like a 2-input XOR gate. When A=0 and B=0, (logic '0' representing Ground and logic '1' representing Input supply voltage) there is voltage degradation due to threshold drop that occurs across transistor M3 and

consequently the output 'Out' is degraded with respect to the input. A second problem of current feedback through transistor M1 also occurs when A=1 and B=0.

Layout for Xor gate:

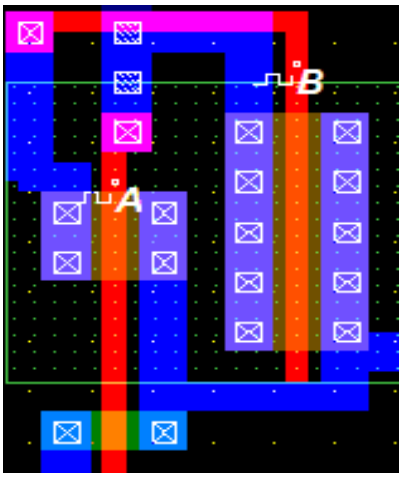

Figure4: layout Xor gate

2.One-bit full adder:

After we build Xor gate we will go to build one-bit adder using this Xor gate as shown in figure 5 schematic for one-bit adder.

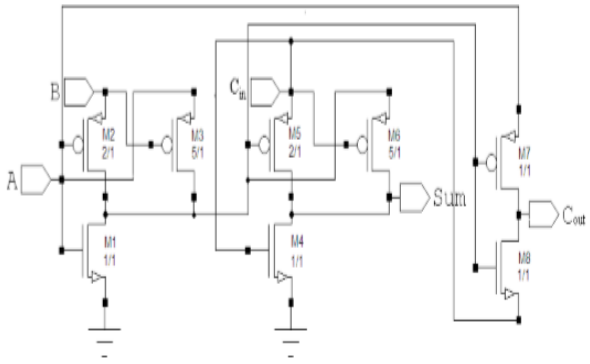

Figure3:Schematic of existing 8T Full Adder[ref1]

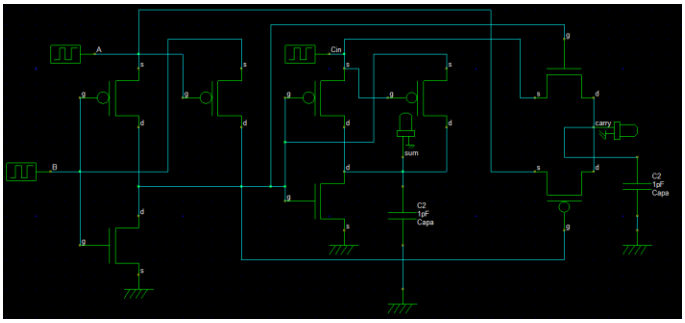

Figure6: DSCH-Schematic of existing 8T Full Adder

As we note from schematic, we build full one-bit adder using 8 transistors only nested of 24 transistor that shown in figure 7.

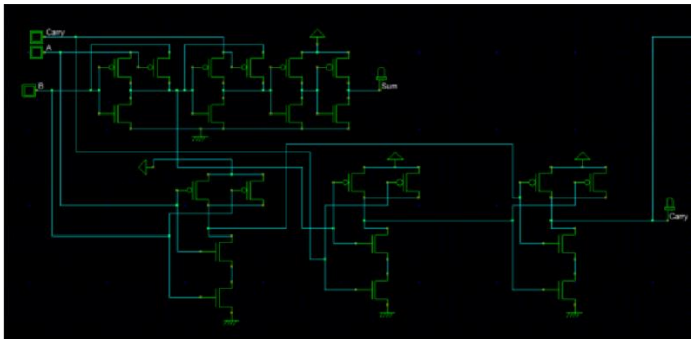

Figure 7: Schematic of existing 24T Full Adder

The simulation of our Full adder in figure8:

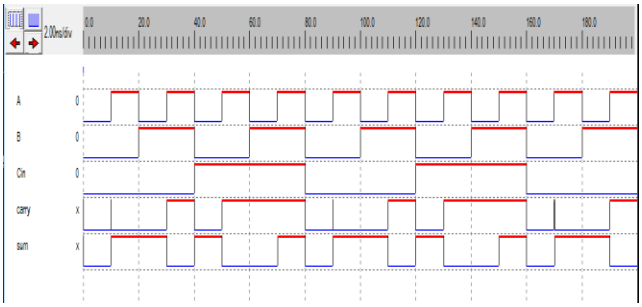

Figure8: Simulation of existing 8T Full Adder

Layout for one-bit adder:

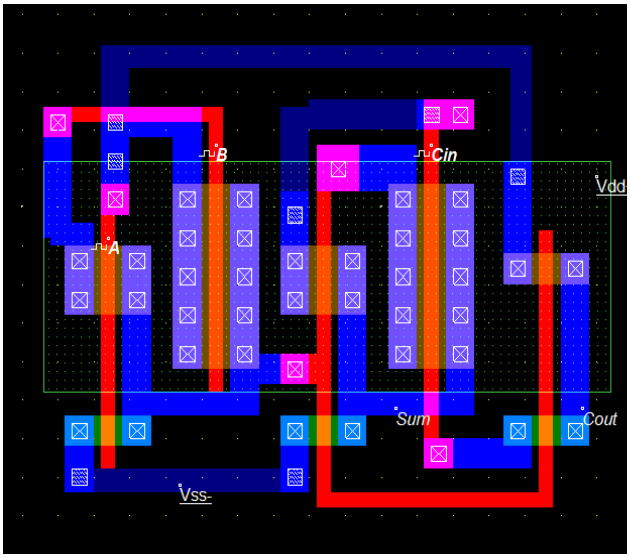

Figure 9: one-bit adder layout

Simulation:

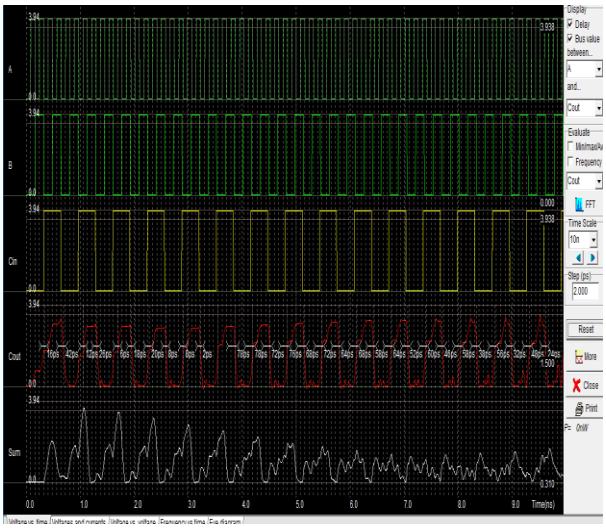

Figure 10: simulation for one-bit adder

Result Area for one-bit adder using CMOS 32nm process technology:

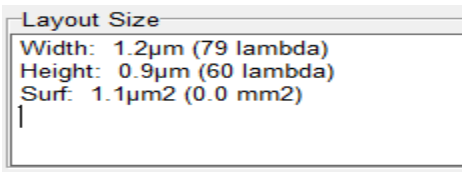

Figure 11: area

using this design, we collect good area minimum as possible and good speed less power.

3. 4-bit full adder:

Finally, we use one-bit adder to build 4-bit full adder using design as shown below in figure 12.

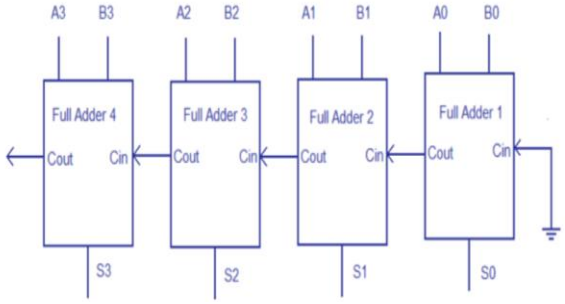

Figure 12:4-bit full adder design

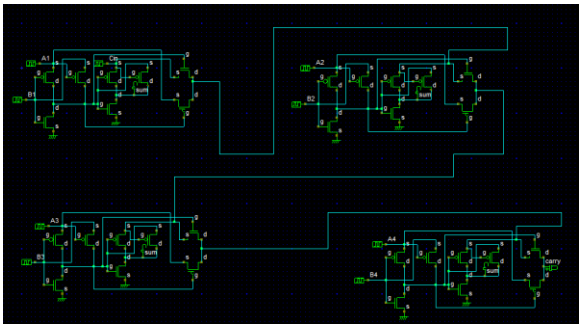

Figure 13: DSCH -4-bit full adder design

The simulation of the schematic as we see in the figure 14 below:

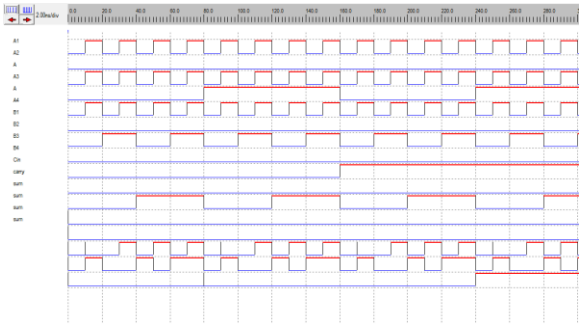

Figure 14: 4-bit adder schematic simulation.

Then the schematic of 4-bit adder made by making connections between one-bit full adders out from 1st to carry in to 2nd adder.

Layout and area result and simulation:

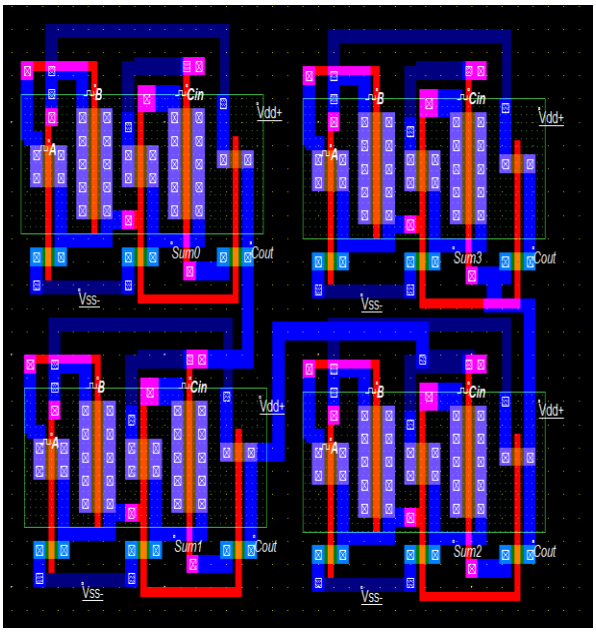

Figure 15: layout for 4-bit adder

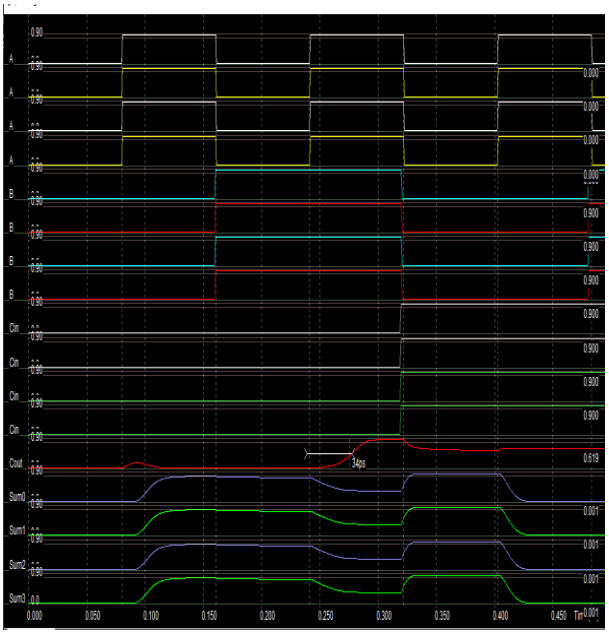

Figure 16: simulation result for adder

When the all inputs are set to '1' the power is 2.904uW. As we see in figure17 and this is the worst case.

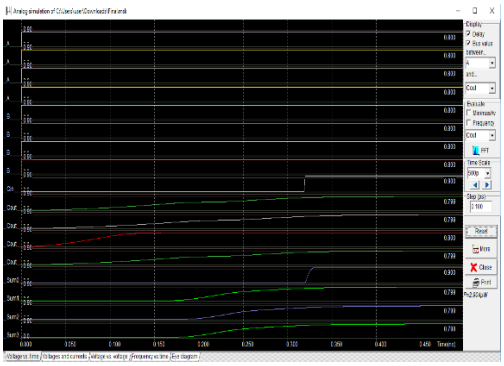

Figure 17: layout simulation for 4-bit adder

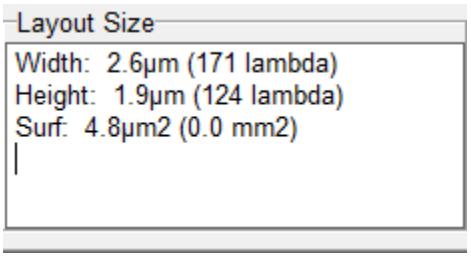

Figure 18: area

The delay is 34us as we see in figure18:

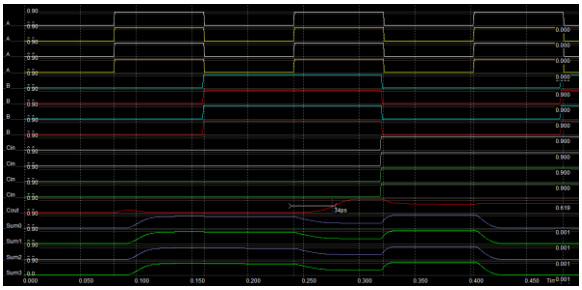

Figure 18: layout simulation for 4-bit adder

IV. Conclusion

In conclusion, we can note that by using optimized design for Xor gate we can get adder with much more speed and less delay by making it predict the carry so the next adders don't need to wait for too long to process.

V. References:

[1]: https://drive.google.com/open?id=1ZYrY0xEIyIZh1hdOe4a8egvORND3Ytci