Q1: Determine the bias state (region of operation) for the circuit conditions if Vtn = 0.4 V. The source voltage is always lower than the drain voltage in an nMOS transistor. First identify the correct terminals.



*VGS* = *VG* – *VS* = 2.2 V – (– 2.3 V) = 4.5 V. *VDS* = *VD* – *VS* = 0.5 V – ( –2.3) = 2.8 V.

Therefore, *VGS* = 4.5 V > 2.8 V + 0.4 V = 3.2 V. the transistor is in non-saturation.



*VGS = VG – VS = 0.9 V – (– 2.5 V) = 3.4 V. VDS = VD – VS = 0.5 V – (– 2.5 V) = 3 V.*

*Therefore, VGS = 3.4 V = VDS + Vtn = 3 V + 0.4 V = 3.4 V, and the transistor is at the boundary of the saturated and non-saturated regions. Either sat or linear equation can be used to calculate ID.*

Q2: Draw cross section view of the 4 terminal PMOS device?

 

Q2: What is the main materials the transistors are made off? What does technology/process mean in terms of transistor geometry?

Silicon /length of the device