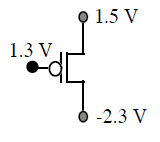
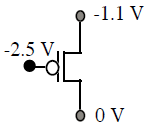
Q1: Determine the bias state (region of operation) for the circuit conditions if Vtn = 0.4 V. Vtp = -0.4 V. The source voltage is always lower than the drain voltage in an nMOS transistor. First identify the correct terminals.

The gate voltage is not sufficiently more negative than either drain or source

terminal to invert holes at the oxide interface, so that the transistor is in the offstate.

*VGS* = – 2.5 – (– 1.1) = – 1.4 V, *VDS* = 0 – ( – 1.1) = 1.1 V. What is wrong? The gate voltage is sufficiently negative to turn on the transistor, but the source to drain

voltage is negative. Holes must leave the source and flow to the drain, but they

can’t under this conclusion. The answer is that the drain terminal with a lower

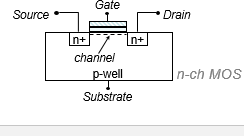
voltage is on the top and the source on the bottom so that *VGS* = – 2.5 – 0 = – 2.5 V,

*VDS* = – 1.1 – 0 = – 1.1 V. Therefore *VGS* > *VDS* + *Vtp*, or – 2.5 V < – 1.1 + (– 0.4) V,

so the transistor is in non-saturation. *The pMOS source terminal always has a*

*higher voltage than the drain terminal*

Q2: Draw cross section view of the 4 terminal NMOS device?



Q3: Q3: Which device is faster NMOS or PMOS AND Why ? What does? What does technology/process mean in terms of transistor geometry?

NMOS/ Mobility

LENGTH OF THE DEVICE