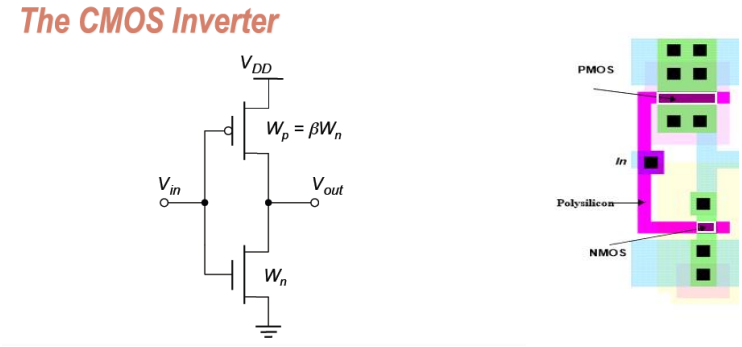
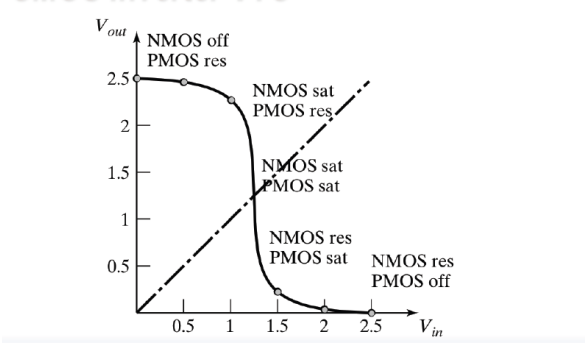
Q1: Draw a schematic and layout (estimate) for CMOS invertor. Assuming P/N ratio is 2 and process is 32nm.

(2.5 points) (2.5 points)



Q2: Draw the VTC curve for the inverter and mark region of operation for each transistor on the curve.

(3 points)



Q3: following up in Q2, If we keep the P size the same and double the N mos size how does the curve will look like ?

Nmos larger then the fall slope will be less and the curve will push to the left

(2 points)