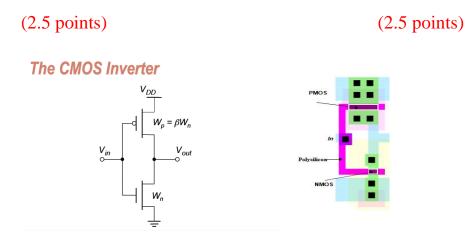
Q1: Draw a schematic and layout (estimate) for CMOS invertor. Assuming P/N ratio is 2 and process is 32nm.



Q2: Draw the VTC curve for the inverter and mark region of operation for each transistor on the curve.

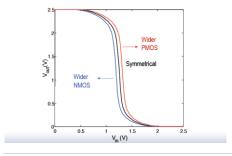
(3 points)

CMOS Inverter VTC V_{out} ↑ NMOS off PMOS res 2.5 NMOS sat PMOS res 2 NMOS sat 1.5 MOS sat 1 NMOS res PMOS sat NMOS res 0.5 PMOS off 0.5 1.5 2.5 V_{in} 1 2

Q3: following up in Q2, If we keep the P size the same and double the N mos size how does the curve will look like ?

Nmos larger then the fall slope will be less and the curve will push to the left (2 points)

Impact of Sizing



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