KH1STSEM2021

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ENCS333_SEC2_QZ2

Align Quiz to Standard

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SOC-51558169

1. Threshold voltage in CMOS can be defined ----- ? SELECT ALL RIGHT ANSWER

A The Threshold voltage, VT for a MOS transistor can be defined as the voltage applied between the gate and the drain of the MOS transistor below which the gate to source current, IGS effectively drops to zero

B The Threshold voltage, VT for a MOS transistor can be defined as the voltage applied between the gate and the bulk of the MOS transistor below which the drain to source current, IDS effectively reach maximum value

C The Threshold voltage, VT for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, IDS effectively drops to zero

2. NMOS transistor can be molded as -------- (select all that apply)

A open circuit all the time

B current source, in saturation region

B current source in saturation region

C short circuit in cutt off

D resistive load in leaner region

3. There are four main different layers in MOS transistors which are

A Drain , Source, Gate , bulk

B capacitance , resistance, inductance , voltage

C waver , package, diod , voltage

4. The transistor **current changes** with the operating temperature but is not affected by mobility

False

5. As the channel length decreases, the depletion region below the gate can no longer be approximated as a rectangular region. So, L ----------

A does not change

B increases

C decreases

6. As Vd is higher, the drain depletion region increases, causing a --

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---------- in Vt.

A decrease

B increase

7. For MOS devices, leakage current occurs in what region

A Linear

B Saturation

C cutt off

8. For the same VDS, as VGS increases, The IDS will ----------

A increase

B decrease

C does not change

D has no effect

9. Hot-e degradation will occure when : When,

A a MOS transistor is in Linear region, , the electric field across the pinch-off region may be high enough that carriers gain there enough energy to excite electron-hole pairs.

B a MOS transistor is in cutt off region, the electric field across the pinch-off region may be high enough that carriers gain there enough

energy to excite electron-hole pairs.

C a MOS transistor is in saturation , the electric field across the pinch-off region may be high enough that carriers gain there enough energy to excite electron-hole pairs.

D In all regions

Add a Question

Multiple Choice **True / False** **Short Answer**