Name Date

ENCS333 QZ1 MARCH 24 Score

**1.** What are the different operating regions foe a MOS transistor?

**A** Cutoff region

**B** Non- Saturated Region

**C** Saturated Region

**D** All are correct

**2.** What are the different MOS layers?

**A** n-diffusion

**B** p-diffusion

**C** Polysilicon

**D** Metal

**E** all of the above

**3.** What are the various Silicon wafer Preparation?

**A** Crystal growth & doping

**B** Ingot trimming & grinding

**C** Verilog code preparation

**D** Wafer polishing & etching and Wafer cleaning.

**E** all of the above are correct except Verilog code preparation

**4.** If a large Vds is applied this voltage with deplete the Inversion layer .This Voltage effectively pinches off the channel near the source.

**T** True

**F** False

**5.** There are only three different layers in MOS transistors which are Drain , Source & Gate

**T** True

**F** False

**6.** Threshold voltage in CMOS Defined as : The Threshold voltage, VT for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, IDS effectively drops to zero.

**T** True

**F** False

**7.** The Channel-length modulatio , the The current between **drain and source terminals is constant and** independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied VDS, increasing VDS causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

**T** True

**F** False

**8.** Define Rise time ? which device nMOS or PMOS determines the Rise time?

In slides rise related to p device size, we mesure 20-80% of the rise signal

**9.** Define Fall time ? which device nMOS or PMOS determines the fall time?

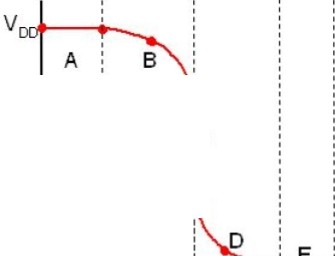
In slides fall related to ndevice, same we mesure 20-80% of fall time

**10.** Define Delay time ?

In slides

Between two signal or input and output measured at 50%

11. What are the different operating regions for an NMOS transistor IN EACH REGION AS SHOWN IN THE FIGURE?



In slides

REGION

A

nMos pMOS c

B

0"1 --Vnaoo-­

c

D

E

.,.



vn