جامعة بيرزيت

BIRZEIT UNIVERSITY

Faculty of Engineering and Technology

Electrical and Computer Engineering Department

Digital Integrated Circuit

ENCS333

Quiz No. 3

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1. **List thee advantage of domino design (Dynamic Logic)?**

- ✓ Full swing outputs (VOL = GND and VOH = VDD).
- ✓ Non-ratioed sizing of the devices does not affect the logic levels.
- ✓ Faster switching speed.

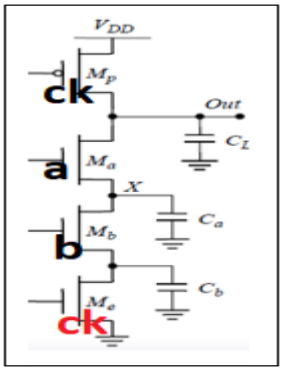
2. **What are the issues of domino design (Dynamic Logic)?**

- ✓ Overall power dissipation usually higher than static CMOS.
- ✓ Pull down network starts to work as soon as the input signals exceeds VTN, so VM, VIH and VIL equal to VTN. (Low noise margin)
- ✓ Needs a precharge/evaluate clock.

3. **List three CMOS Logic advantage?**

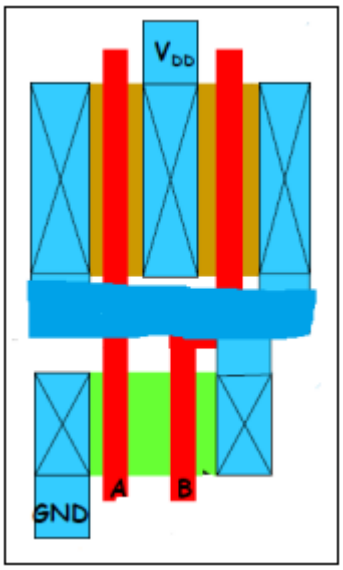
- ✓ Full rail-to-rail swing: **High Noise Margin**.
- ✓ No direct path steady state between power and ground: **No static power dissipation.**
- ✓ Always a path to V_{DD} or Ground in steady state: **Low output impedance.**

4. **Define Charge Sharing? Do we have charge sharing problem in the attached figure? if yes how do we solve it**



- ✓ Charge sharing: Charge stored originally in C_L is redistributed (shared) over C_L and other capacitors leading to reduce roubstness.
- ✓ Yes we have charge sharing problem.
- ✓ To solve: Precharge internal nodes using a clock driven transistor (at the cost of increased area and power).

5. **What is the function of the attached layout? Is this an optimal design? Explain**



- ✓ Nand Gate.
- ✓ No, It's not the optimal design as there exists many capacitance which can be reduced if we shred the diffusion