Question 1

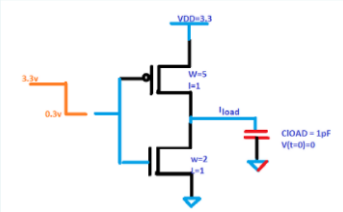
Correct

Mark 5.00 out of 5.00

Flag question

A step input is applied at time t=0 to the loaded inverter with dimensions and initial conditions as shown below.

For all transistors: $L_{min} = 1\ \mu m$, $W_{min} = 1\ \mu m$, $V_{T,p} = -1\ V$, $\mu_p C_{ox} = (1/6) \times 10^{-3}\ A/V^2$, $\lambda_p = 0.0V^{-1}$, $V_{T,n} = 1\ V$, $\mu_n C_{ox} = (1/2) \times 10^{-3}\ A/V^2$, $\lambda_n = 0.0V^{-1}$.



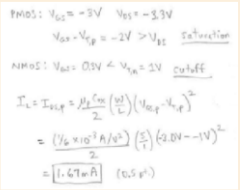
What region the PMOS will be in? (Linear, Cutoff, Saturation) — Saturation ✔

What region the NMOS will be in ? — Cutoff ✔

What is the current *Iload* immediately after the step is applied in mA? — 1.67 ✔

Note: do not add a unit, just the number

Your answer is correct.



The correct answer is:

What region the PMOS will be in? (Linear, Cutoff, Saturation) → Saturation,

What region the NMOS will be in ? → Cutoff,

What is the current *Iload* immediately after the step is applied in mA?

Note: do not add a unit, just the number → 1.67

Question 2

Partially correct

Mark 0.67 out of 1.00

Flag question

Match to the correct answer

Performance	Directly affects cost ✖
Area	Directly affects cost ✔
Body (substrate) normally connected to ---------- for NMOS	Power-Delay Product ✖
The interface between designer and process (CMOS fabrication) engineer	Design Rules ✔
used in chip manufacturing	Silicon ✔
Raising source voltage increases ---------- of transistor	Threshold Voltage ✔

Your answer is partially correct.

You have correctly selected 4.

The correct answer is:

Performance → Power-Delay Product,

Area → Directly affects cost,

Body (substrate) normally connected to ---------- for NMOS → Threshold Voltage,

The interface between designer and process (CMOS fabrication) engineer → Design Rules,

used in chip manufacturing → Silicon,

Raising source voltage increases ---------- of transistor → Threshold Voltage