DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

Digital Integrated Circuits - ENCS333

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Lecture #5

Static CMOS Logic part 1

PROCESS FILE LINK:

- https://github.com/siwS/vlsi/blob/master/vlsi_2011/MW3.1.7/MW3.1.7/rules/cmos65n.rul
- http://ptm.asu.edu/
- www.mosis.orgwww.mosis.org

Agenda

- **General complementary logic design,**

perspective, stick-figure circuit diagrams

- **•Examples: constructing PDN/PUN duals,**

logic -> circuit, circuit -> logic,

circuit -> layout, layout -> circuit,

cross sectional views of layout

What is a MOSFET?

A resistor: $$R_n = \frac{1}{\mu_n C_{ox}(V_{GS} - V_{Tn})}\left(\frac{L}{W}\right)$$

- (among other things ...) Increasing W decreases the resistance; allows more current to flow

Oxide capacitance $C_{ox} = \varepsilon_{ox} / t_{ox}$ [F/cm^2]

Transconductance $\beta_n = \mu_n C_{ox}\left(\frac{W}{L}\right) = k'_n\left(\frac{W}{L}\right)$

Gate capacitance $C_G = C_{ox} WL$ [F]

nFET vs. pFET

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})} \qquad \beta_n = \mu_n C_{ox} \left(\frac{W}{L}\right)_n$$

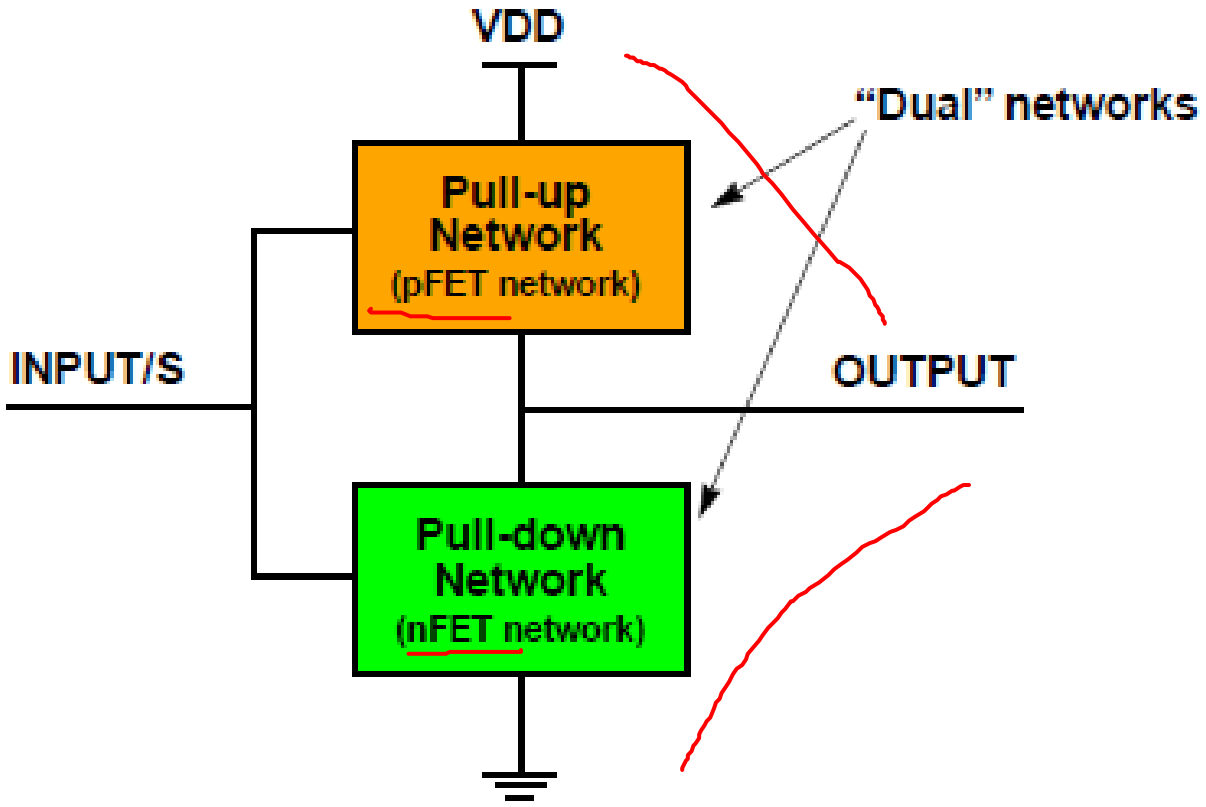
$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)} \qquad \beta_p = \mu_p C_{ox} \left(\frac{W}{L}\right)_p$$

$$\frac{\mu_n}{\mu_p} = r \quad \text{Typically } (2 \ldots 3)$$

(μ is the carrier mobility through device)

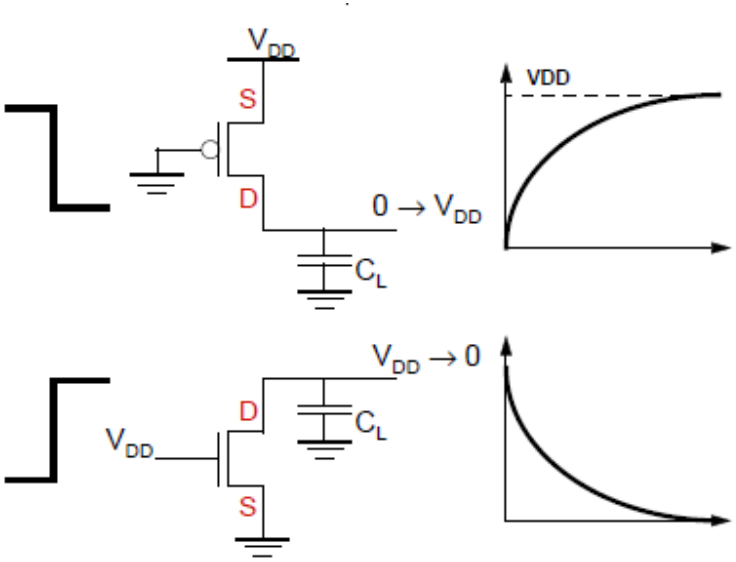
(We will return to this later …)

Complementary Design

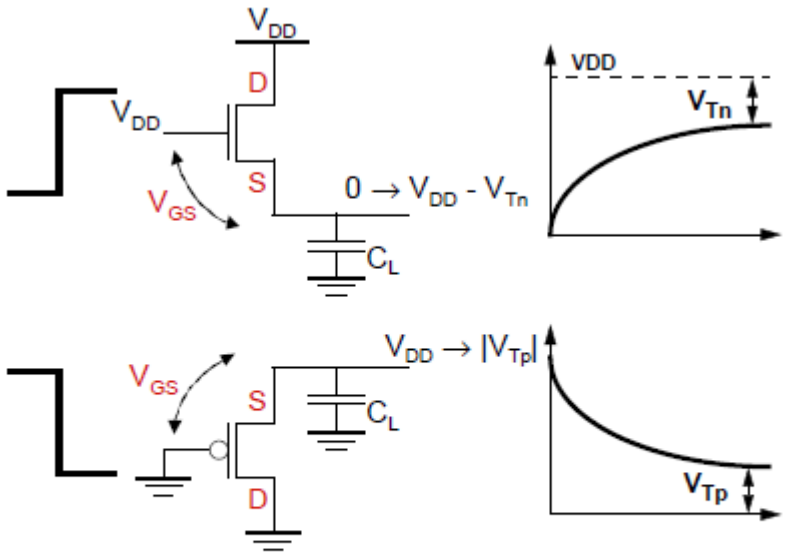


- PMOS "Pull-Up" Network (PUN)
- NMOS "Pull-Down" Network (PDN)

Why Division?

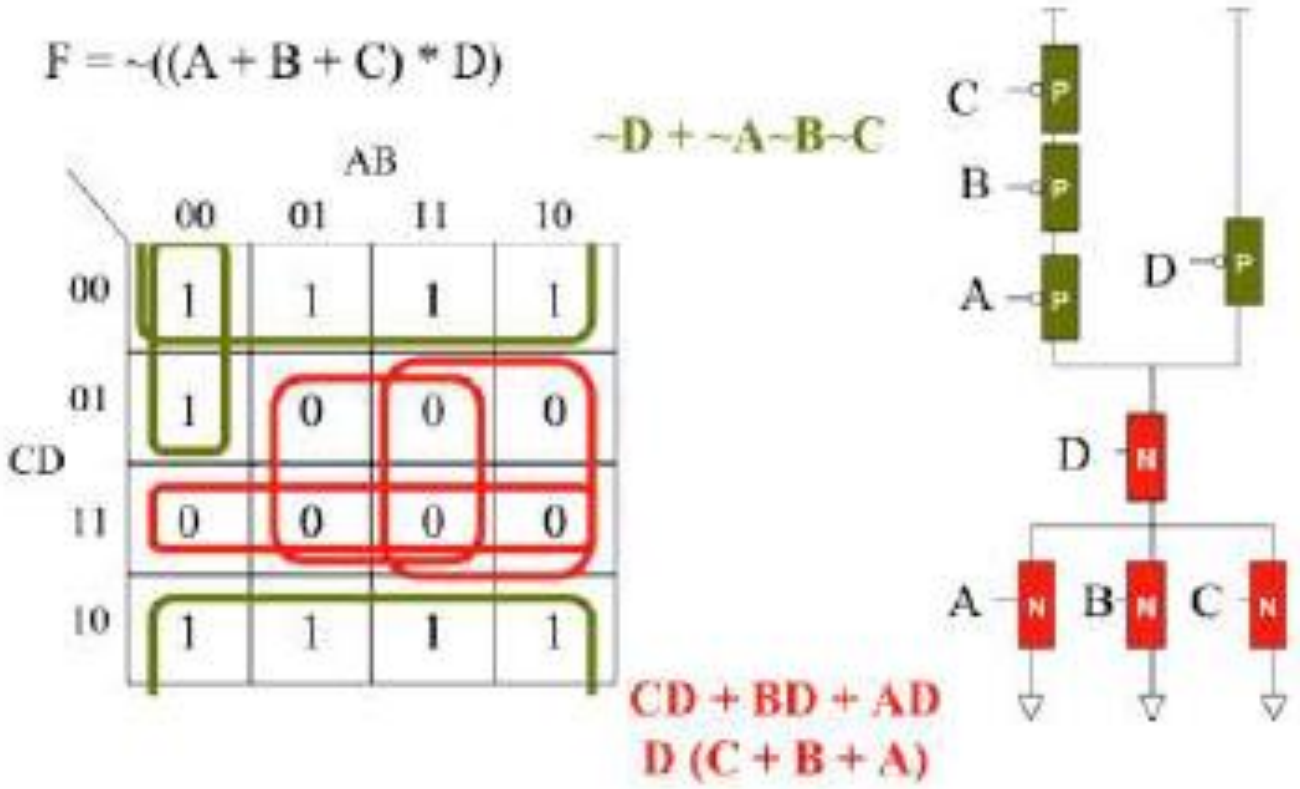


PMOS will pass a "1"
NMOS will pass a "0"



NMOS will not pass a "1"
PMOS will not pass a "0"

Implements Arbitrary Logic



- Pull-Up Network: on when function = 1
- Pull-Down Network: on when function = 0

Static CMOS: Perspective

- "Static" as in "output is logic function of inputs, and, given stable inputs, does not change over time"

- Propagation delay function of load capacitance and resistance of transistors

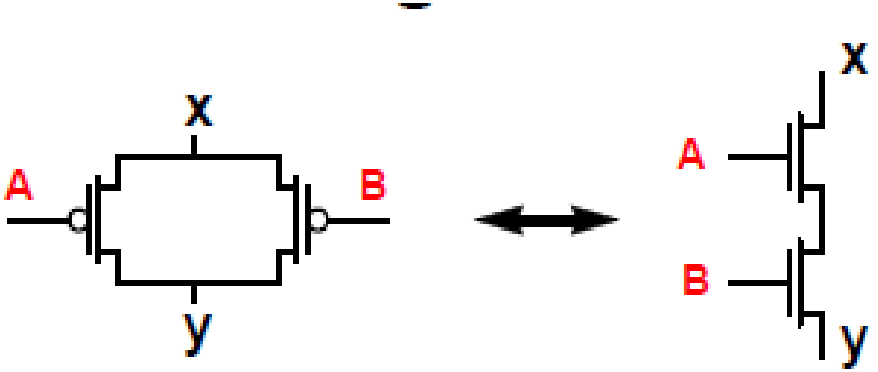
PROS:

- Full rail-to-rail swing; high noise margins
- Logic levels not dependent upon relative device sizes
- Always a path to Vdd or Gnd in steady state; low output impedance
- Extremely high input resistance; nearly zero steady-state input current
- No direct path steady state between power and ground; no static power dissipation

CONS:

- N inputs => 2N transistors in design

Constructing the Dual

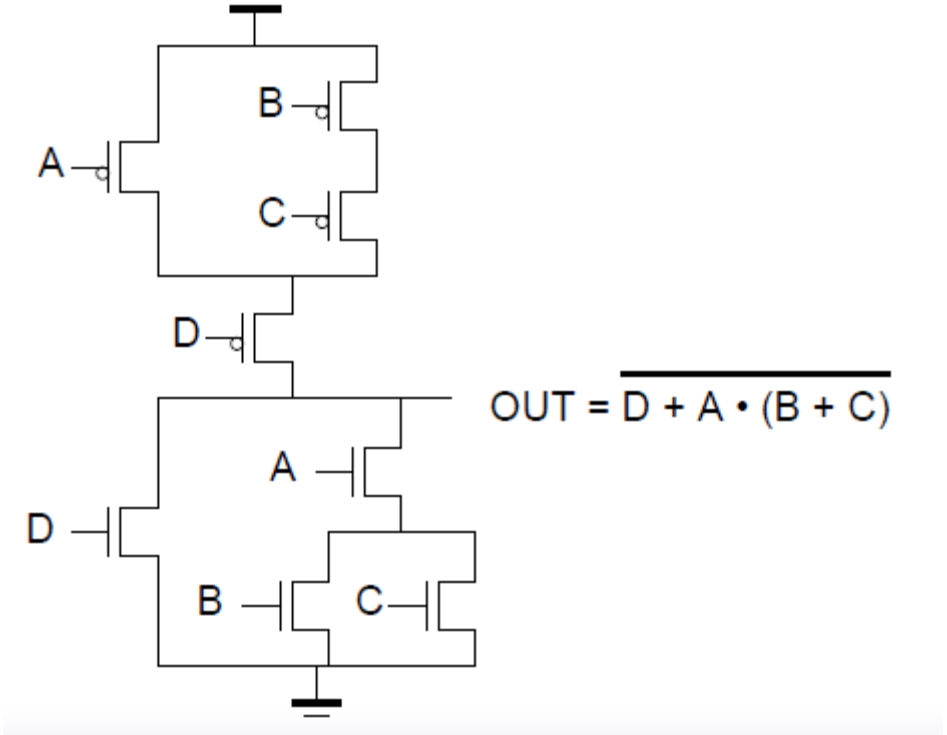


Transistors in parallel are in series in dual; transistors in series are in parallel in dual

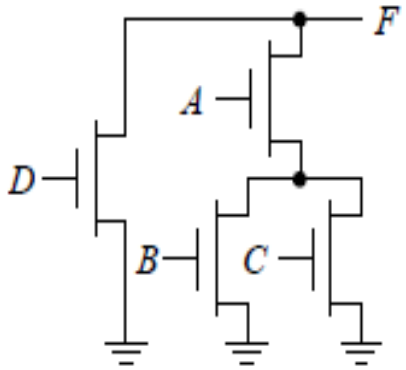
This is the physical realization of DeMorgan's theorems:

- **A + B = A • B [!(A + B) = !A • !B *or* !(A | B) = !A & !B]**
- **A • B = A + B [!(A • B) = !A + !B *or* !(A & B) = !A | !B]**

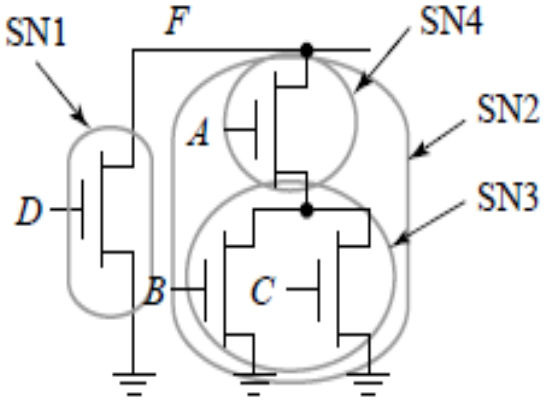
Complex CMOS Gate



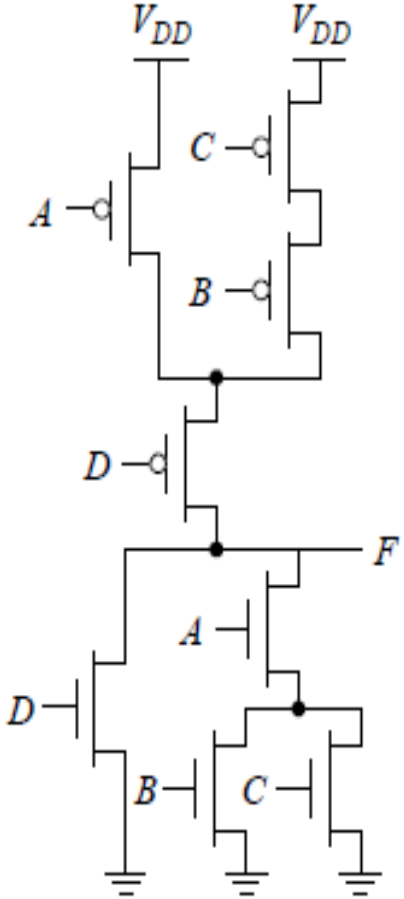
Constructing a Complex Gate



(a) pull-down network



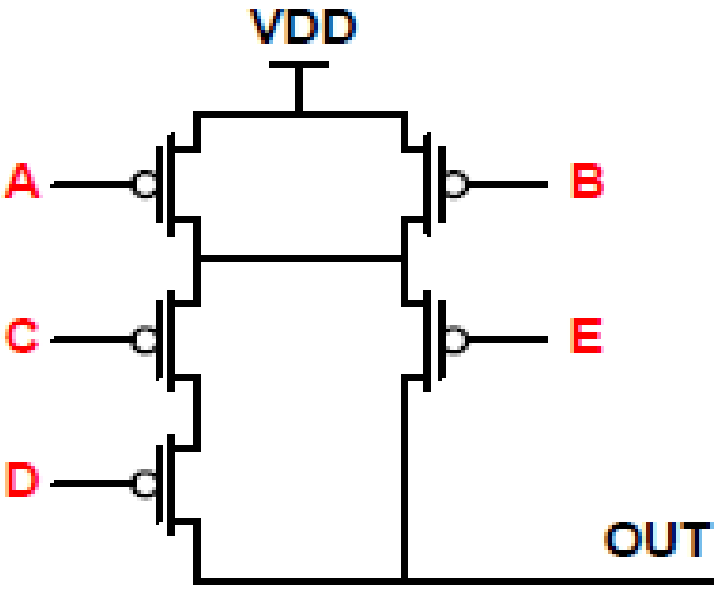
(b) Deriving the pull-up network hierarchically by identifying sub-nets



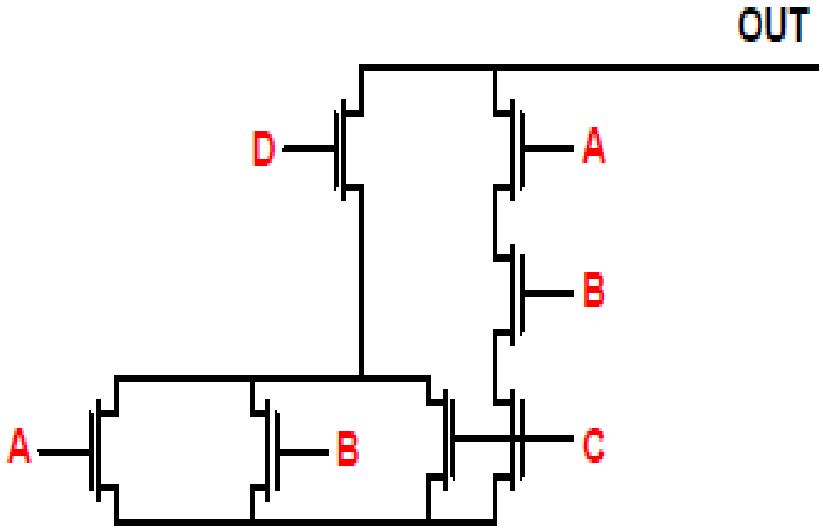
(c) complete gate

Complex CMOS Gate

Constructing the Dual

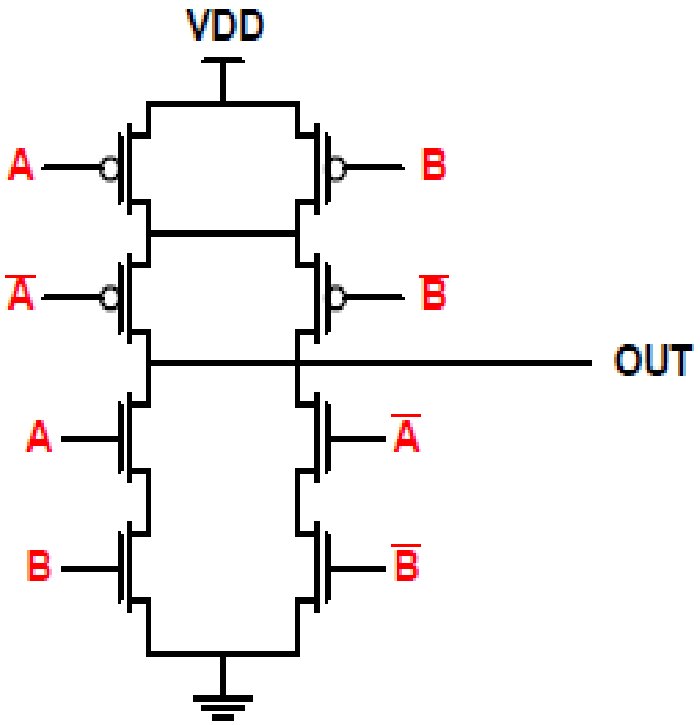


Constructing the Dual



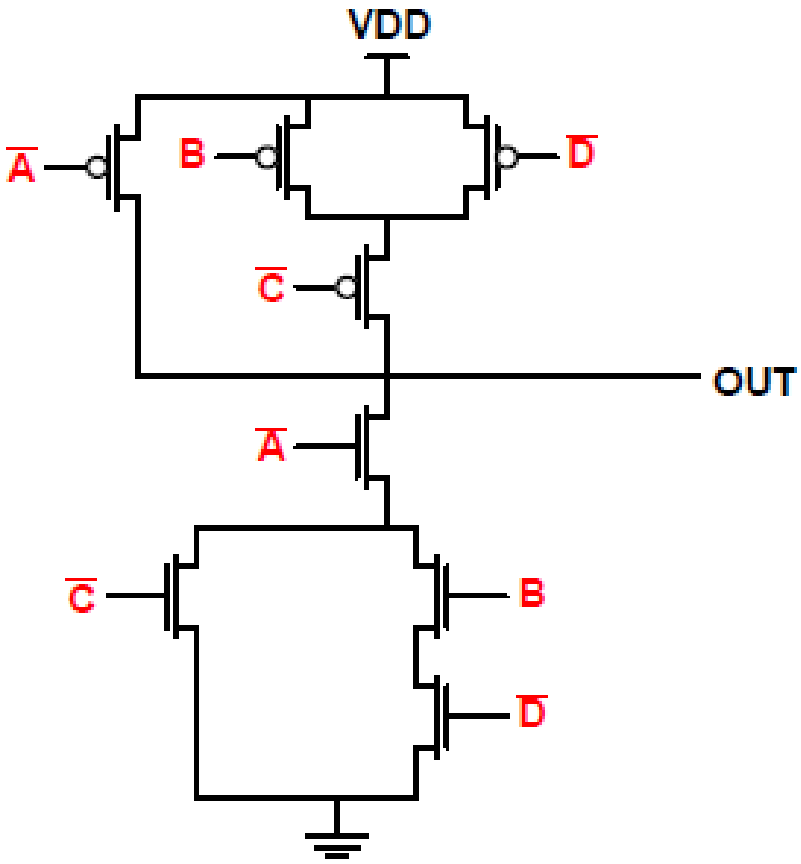
Examples: Logic <-> Circuit

XOR [out = ~($\overline{A}\,\overline{B}$ + A B)]



Examples: Logic <-> Circuit

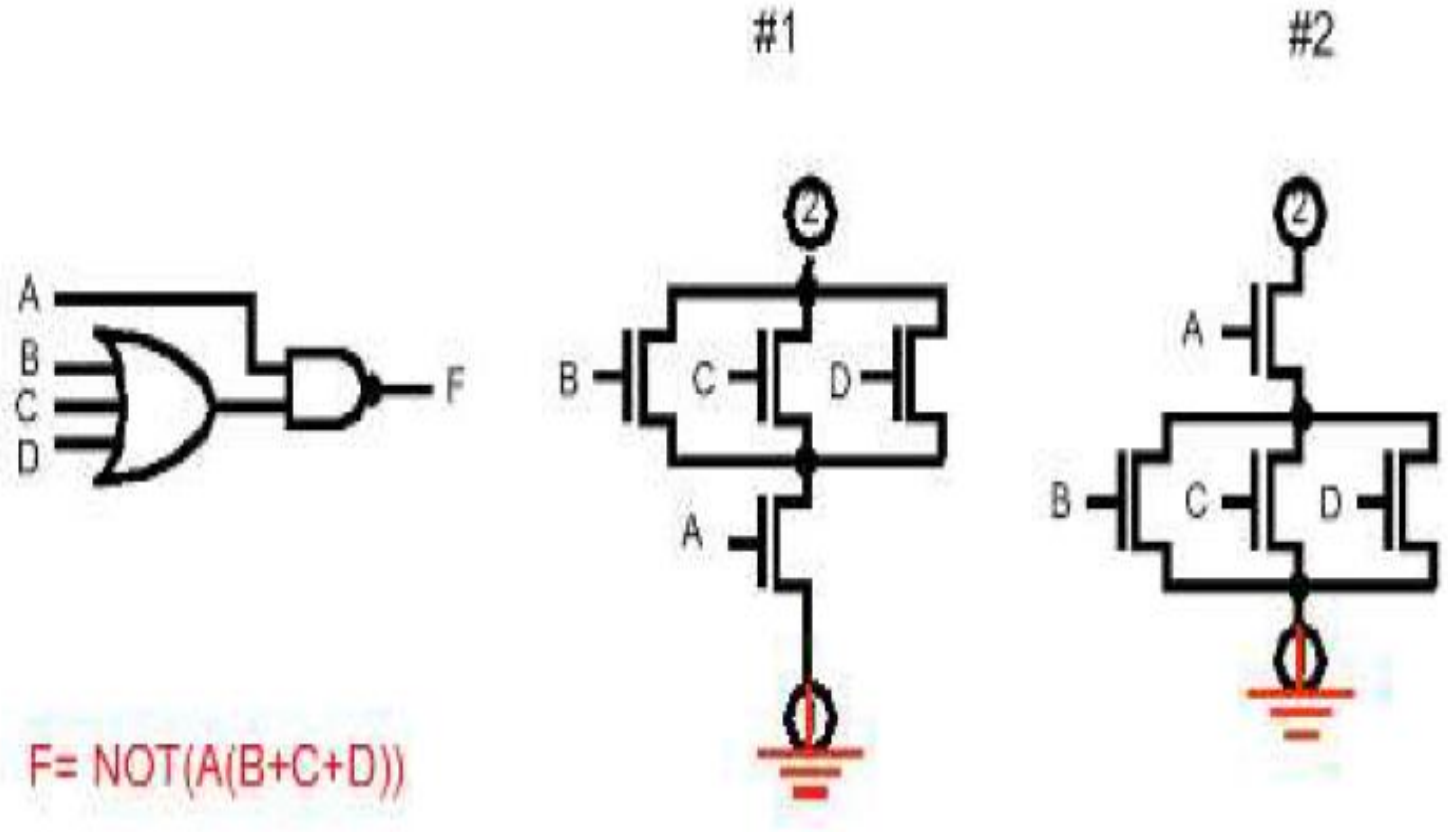
$out = \sim(\overline{A} \cdot (\overline{C} + B\overline{D}))$



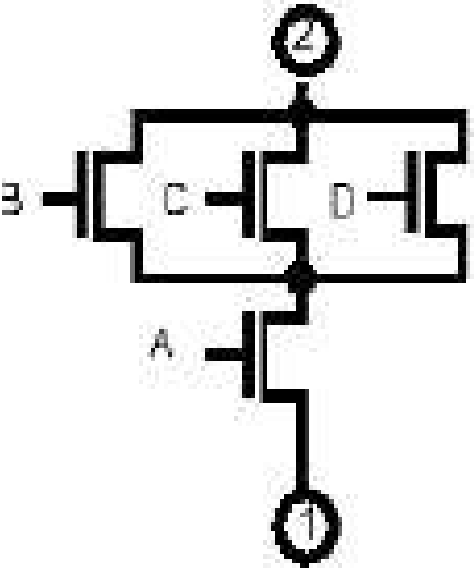
Examples: Layout <-> Circuit

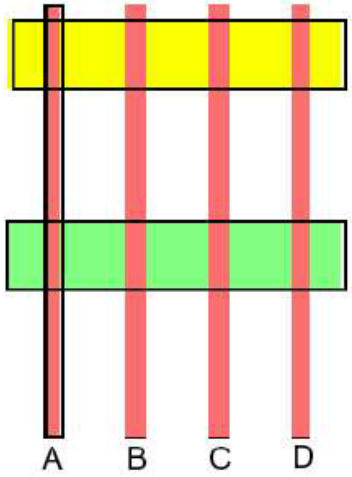
NOT ALL LAYOUTS ARE CREATED EQUAL

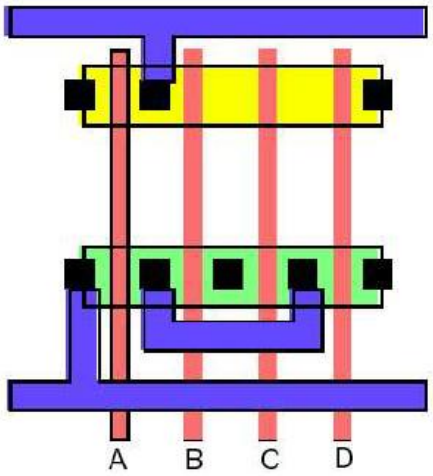
Let's look at two "equivalent" approaches

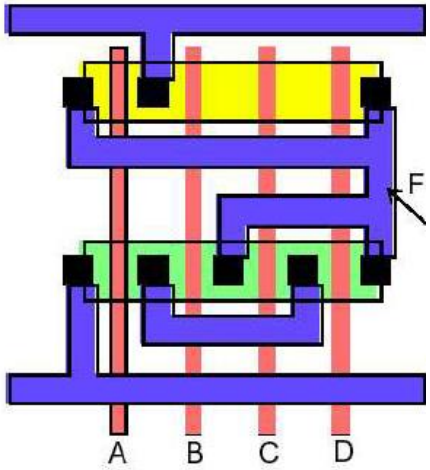


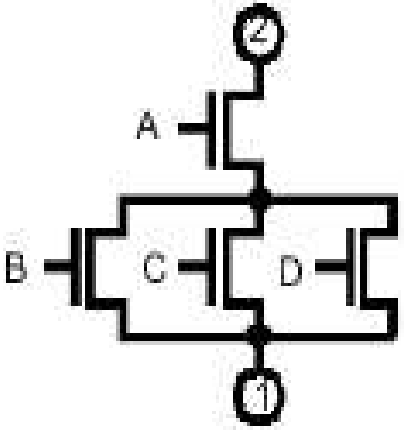
Examples: Layout <-> Circuit

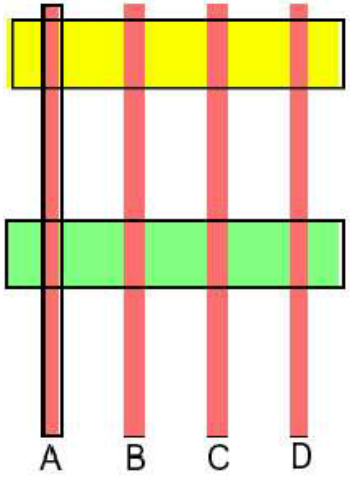


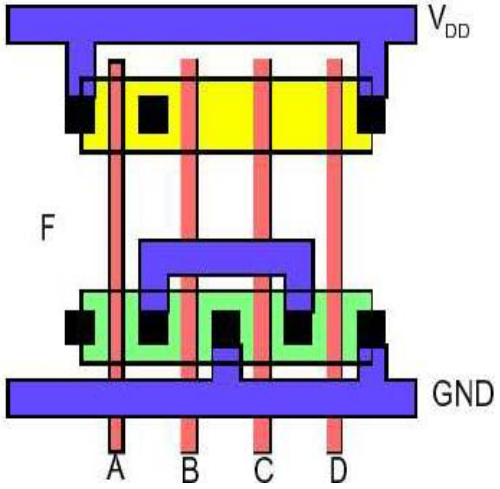


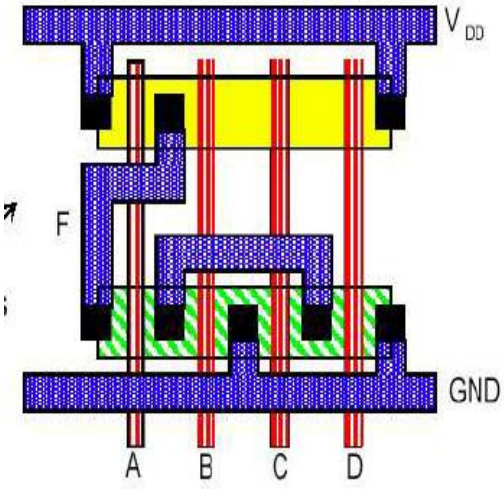






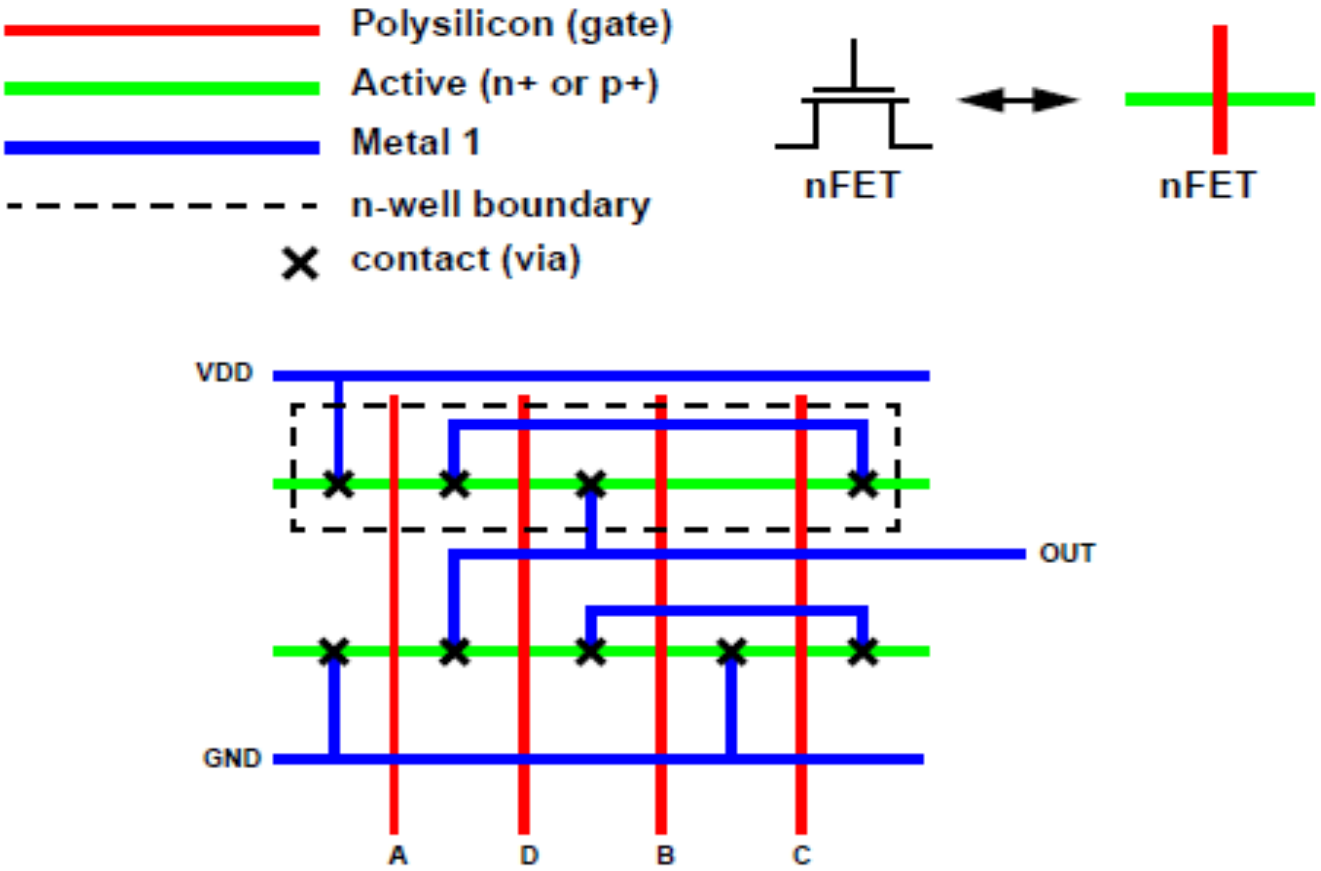






Stick Diagrams

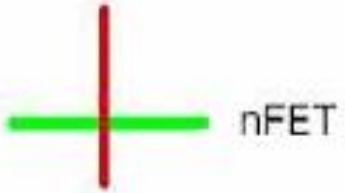
- **Introduced by Mead & Conway in 80's**
- **Every line of conduction-material layer is represented by line of distinct color**



Stick Diagrams

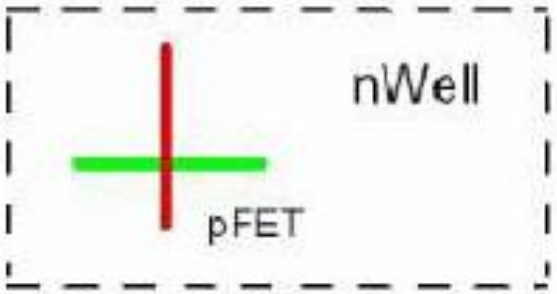
In terms of stick diagrams, we thus say that an nFET is formed whenever

Red (Poly) crosses over Green (Active)



This is consistent with a top view of the transistor.

A pFET is described by the same "red over green" coding, but the crossing point is contained within an nWell boundary

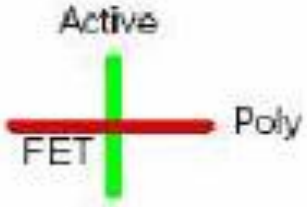


Stick Diagrams

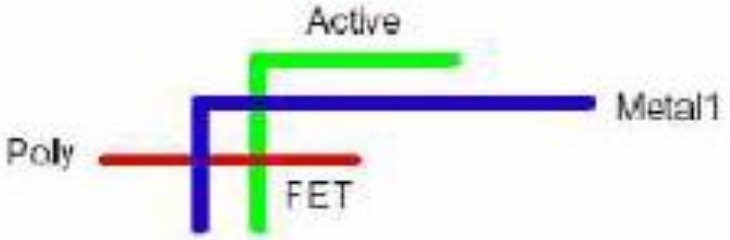
The rules for constructing stick diagrams are based on the characteristics of the conducting layers.

- Only the routing is important, not the line widths

- Red over green gives a FET
  (Poly) (Active)

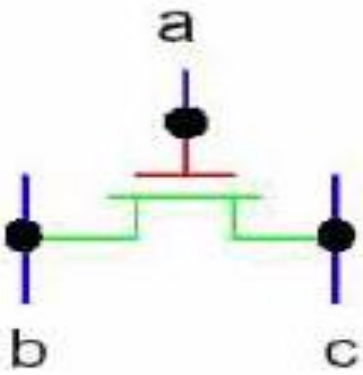


- Blue may cross over green or red without a connection
  (Metal1) (Active) (Poly)

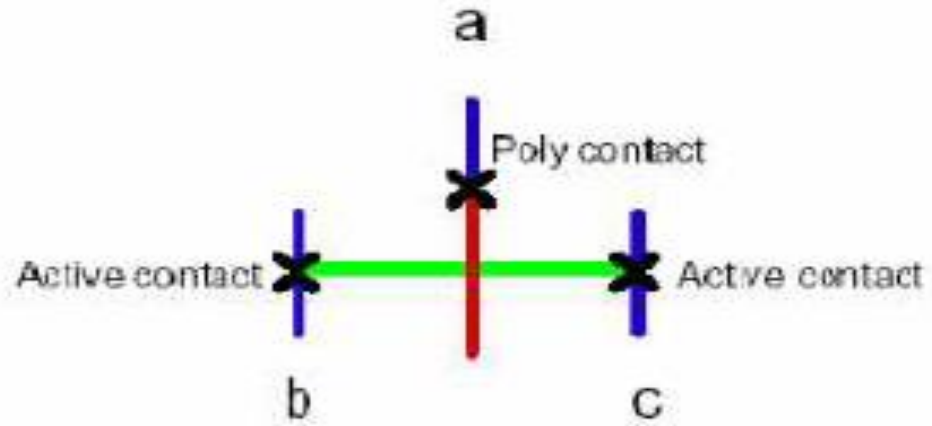


Stick Diagrams

Connections between layers are specified by ✖



Schematic

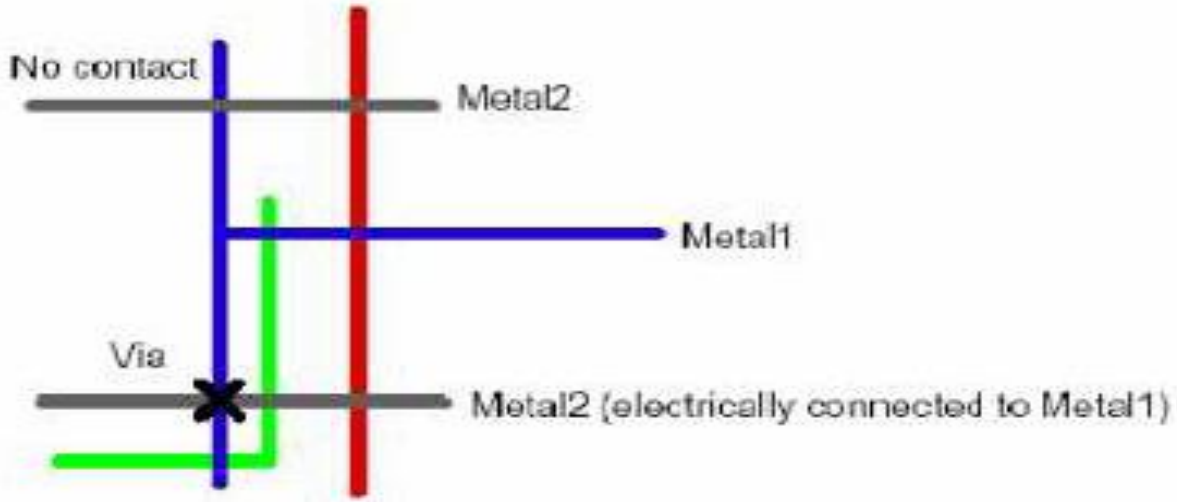


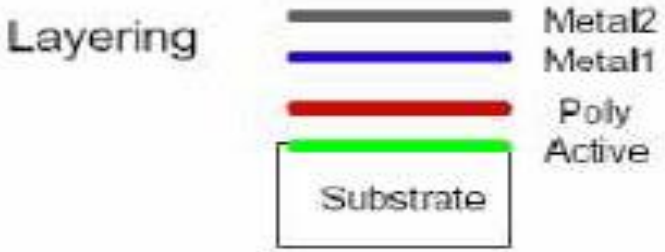
Stick diagram

Poly contact: Metal1-to-Poly
Active Contact: Metal1-to-Active

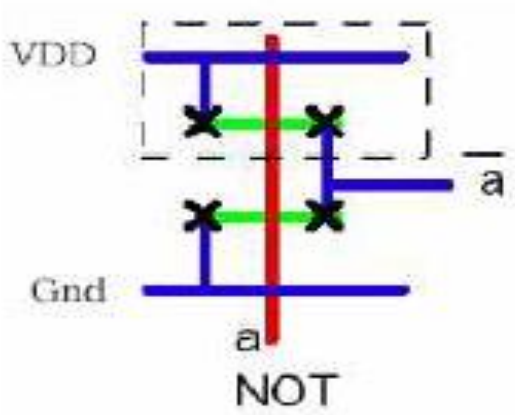
Stick Diagrams

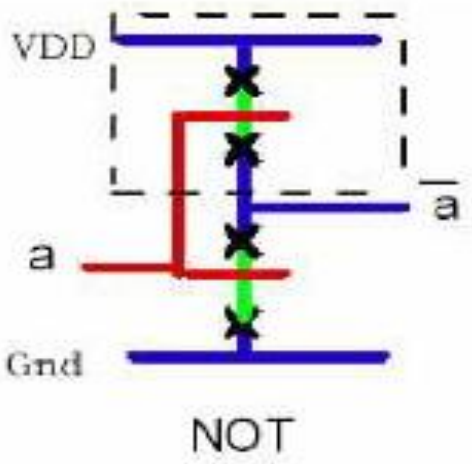
Metal lines on different layers can cross one another.
Contacting two metal lines requires a via

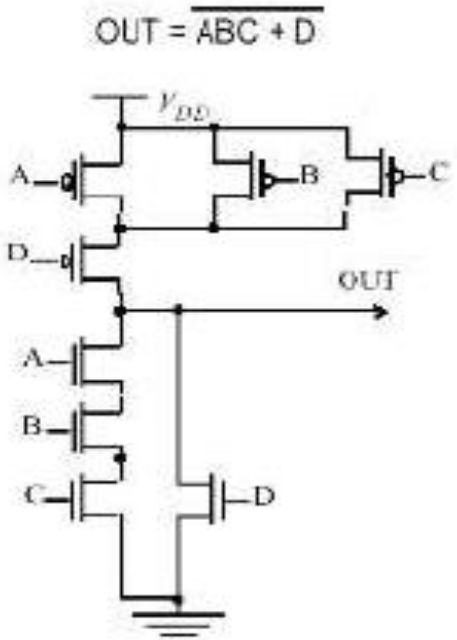


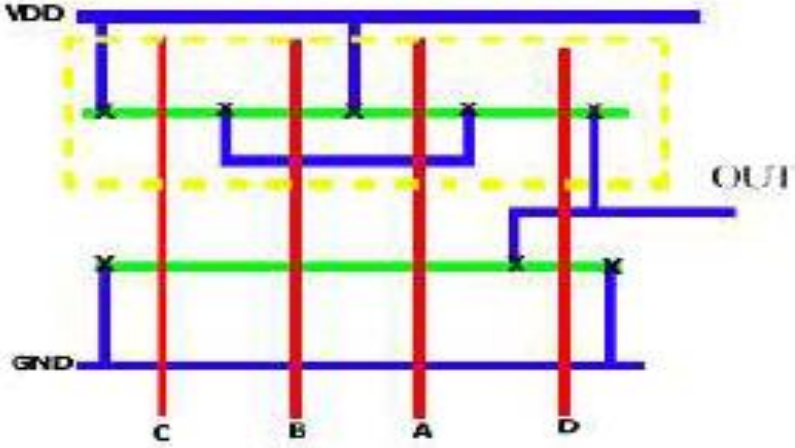


Stick Diagrams



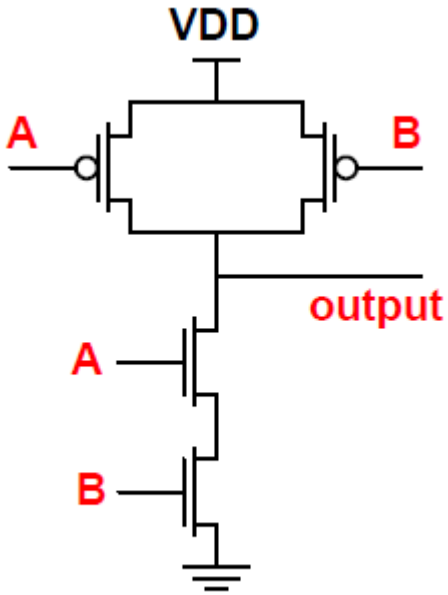


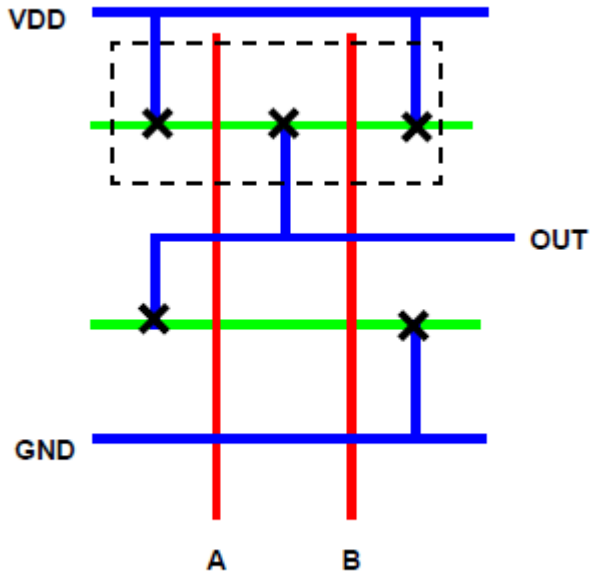




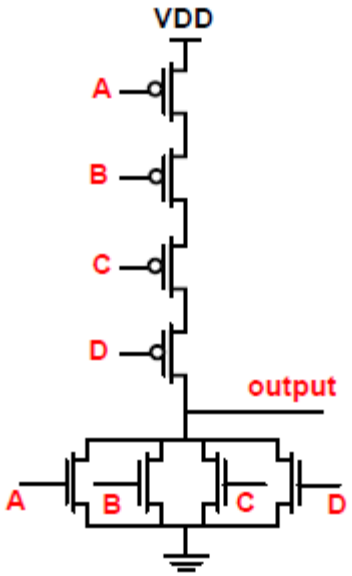
Examples

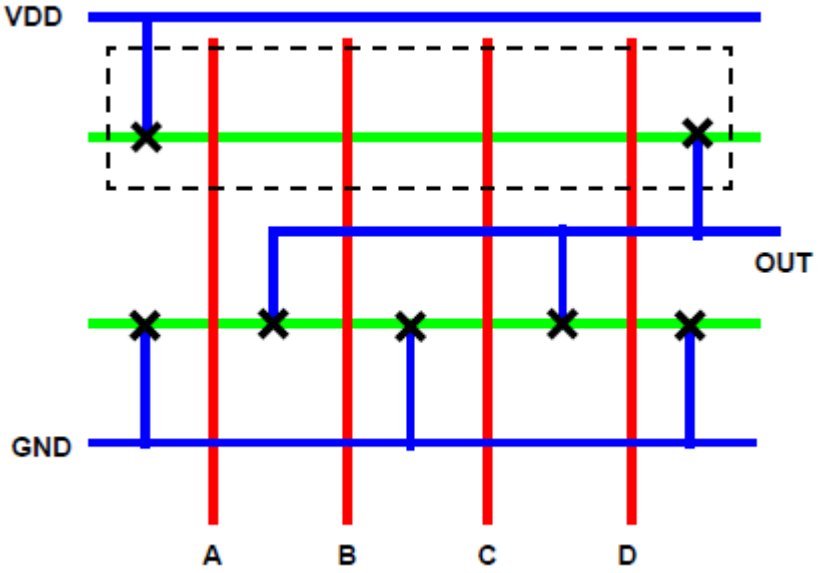
2-input NAND





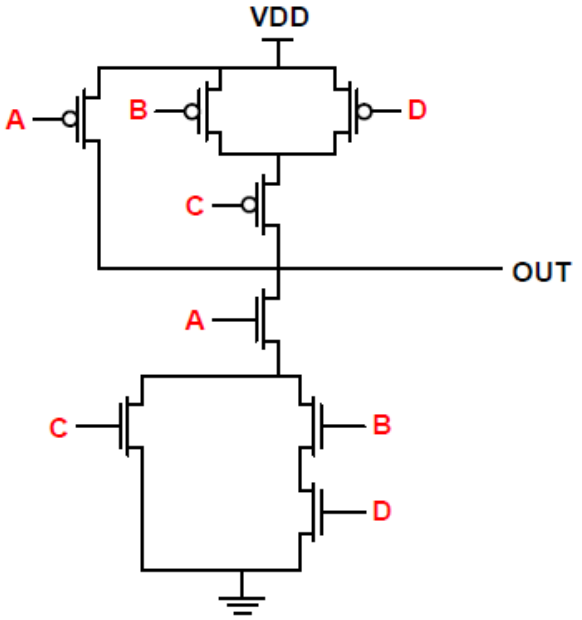
4-input NOR

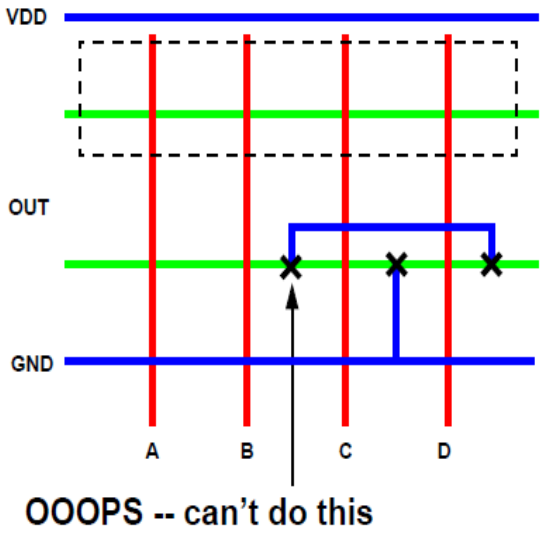




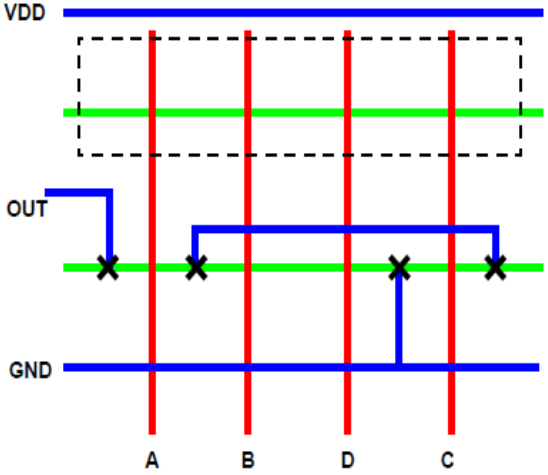
Examples

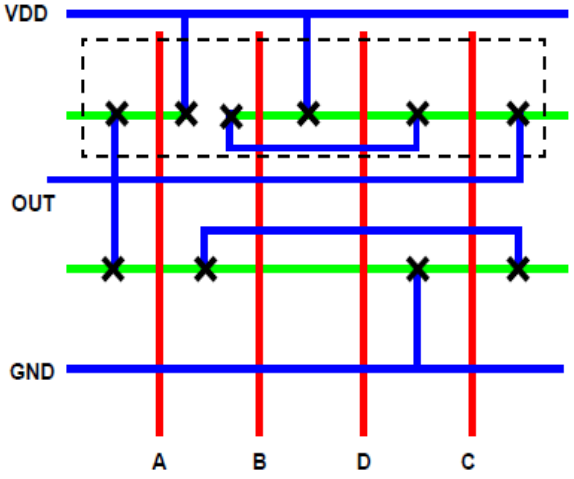
out = ~(A • (C + BD))





OOOPS -- can't do this





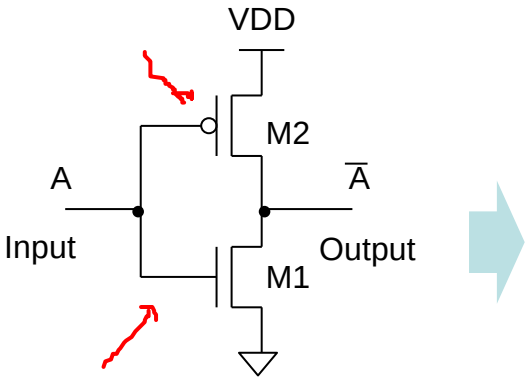
For PUN, either re-route poly or cut p-diff

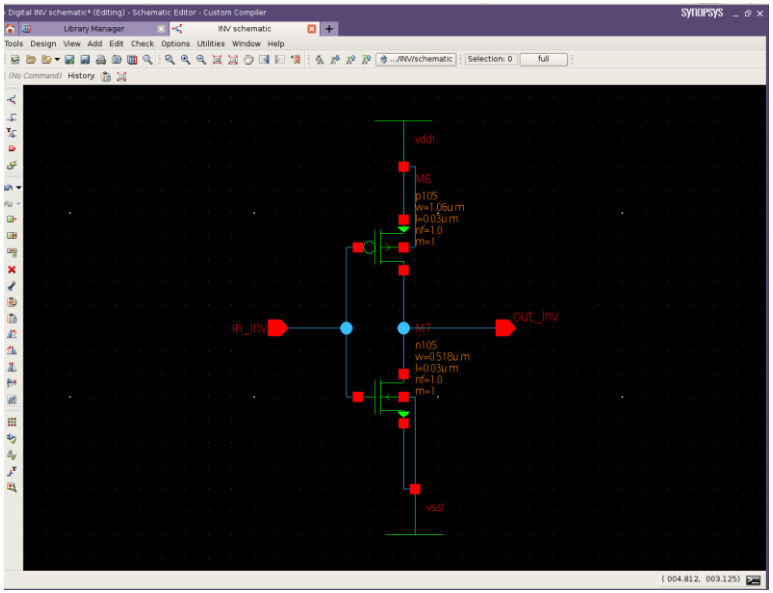
Schematic Design Goal

- The aim of schematic design is to create a circuit which works at operating conditions defined in specification and have the parameter values needed
- Schematic design
  - Structural synthesis
  - Parametric synthesis
  - Parametric optimization

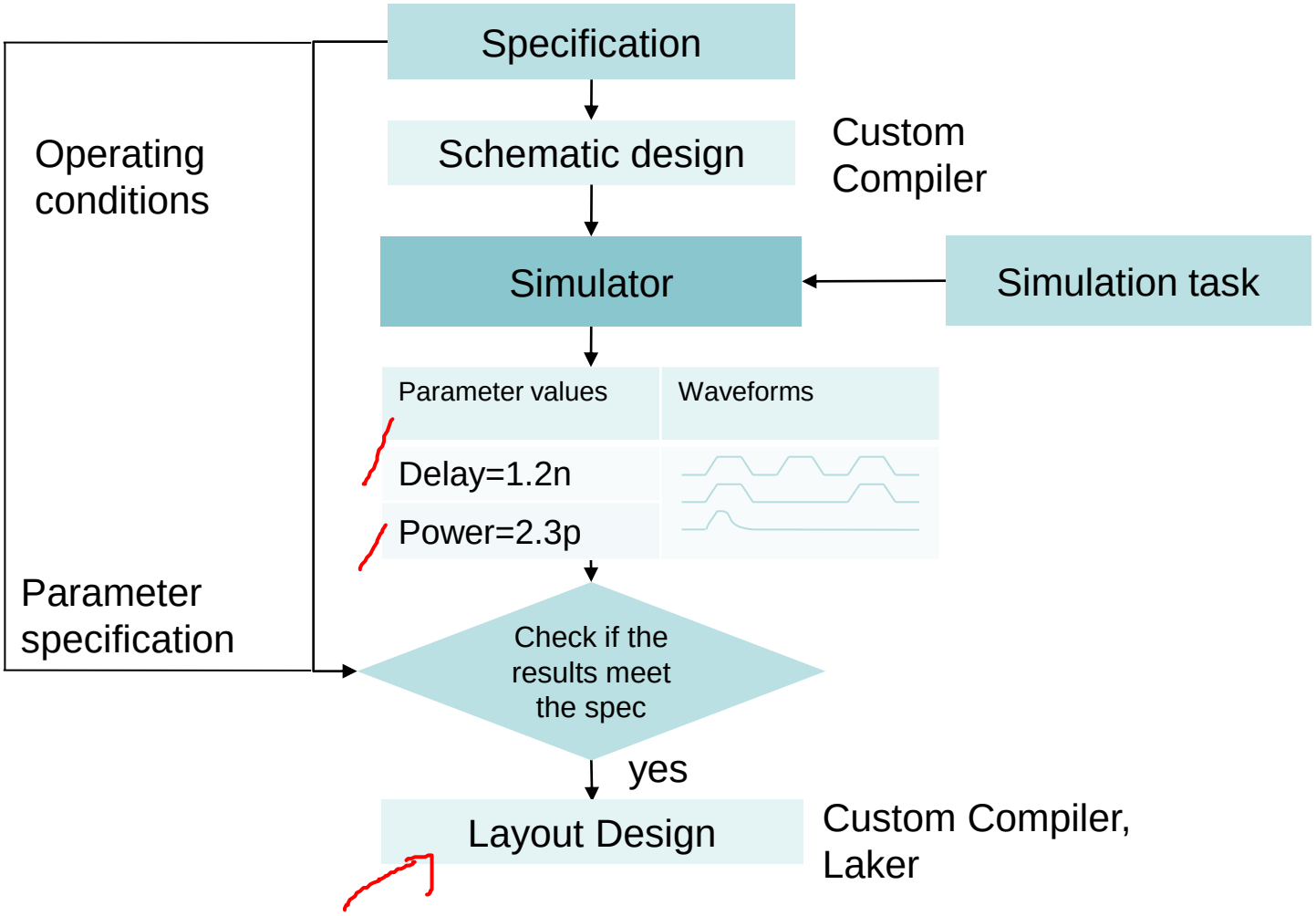
Circuit Selection

- Usually a known circuit structure is selected
- Design can find a convenient structure which is known to be good for the problem being solved



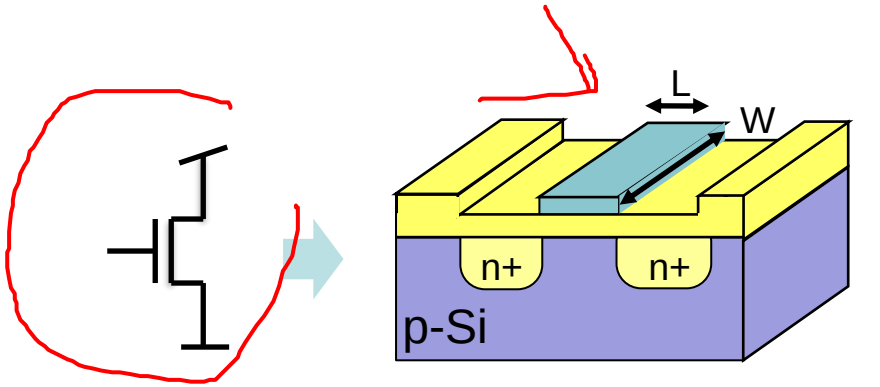


Schematic Design

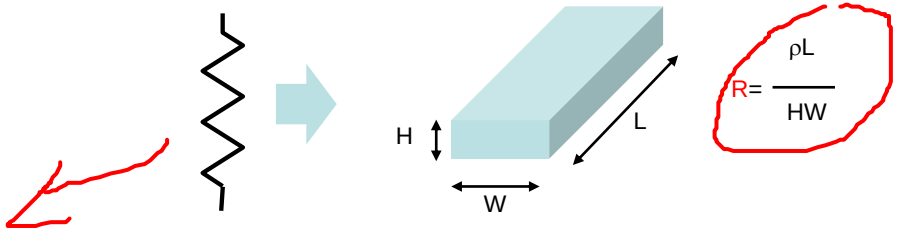


Parametric Optimization

- Each device has configurable parameters
- Schematic designer changes these parameters to get a circuit which meets the specification



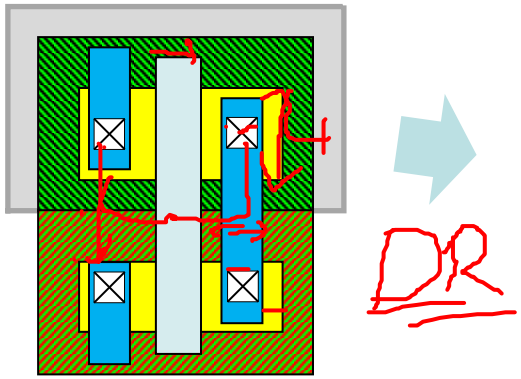
W - gate width, L - gate length

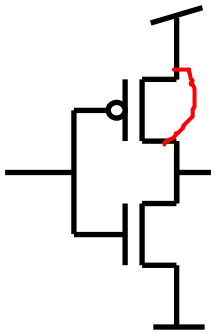


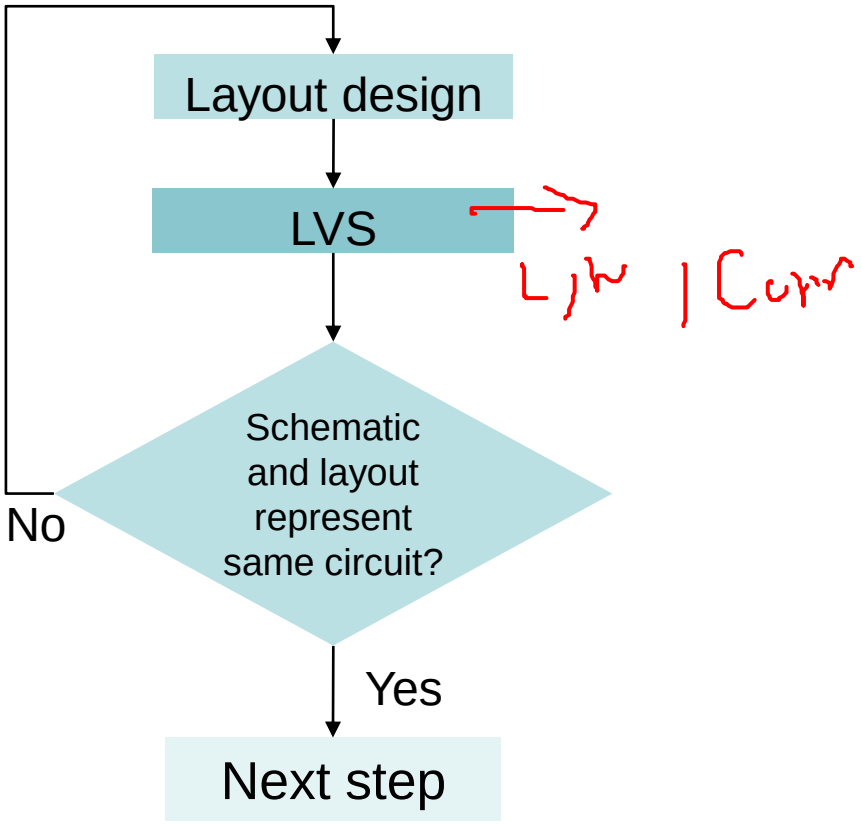
W - resistor width, L - resistor length

Transistor gate width and length, or resistor dimensions can be changed to change their electrical characteristics.

Layout Versus Schematic (LVS)

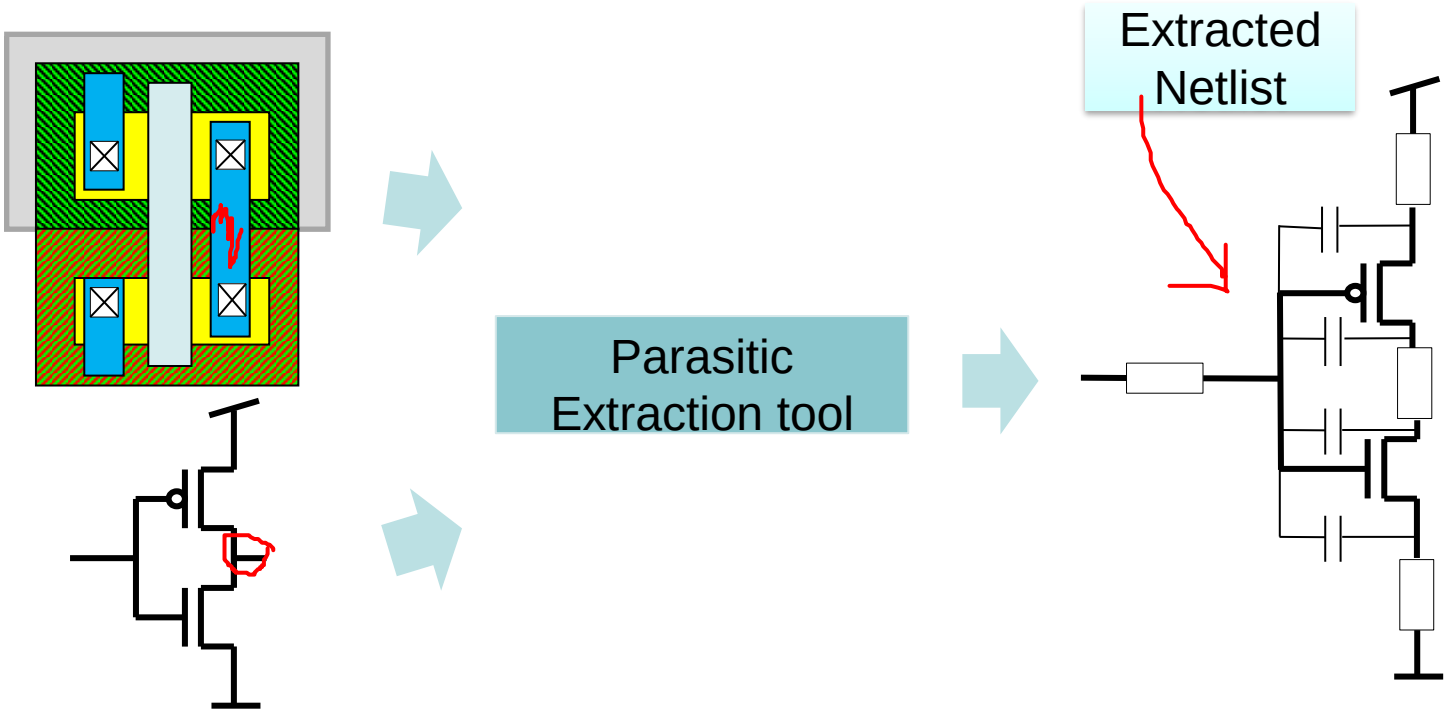






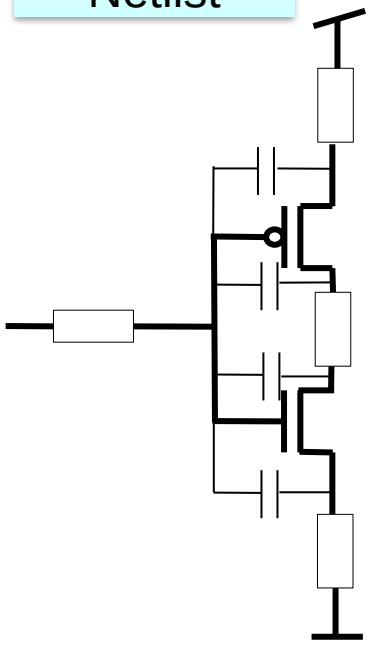
Layout Parasitic Extraction (LPE)

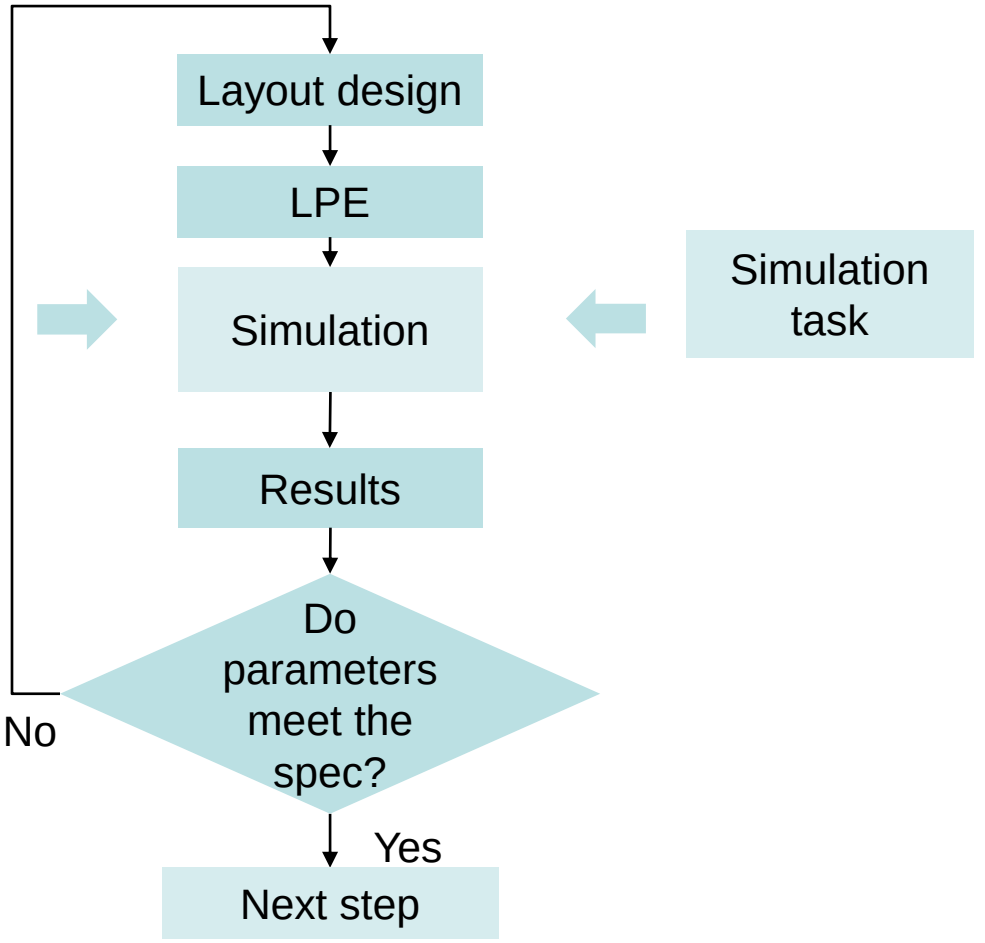
- There is a parasitic extractor tool which calculates parasitic devices present in layout adds them back to circuit



Simulation of Extracted Netlist

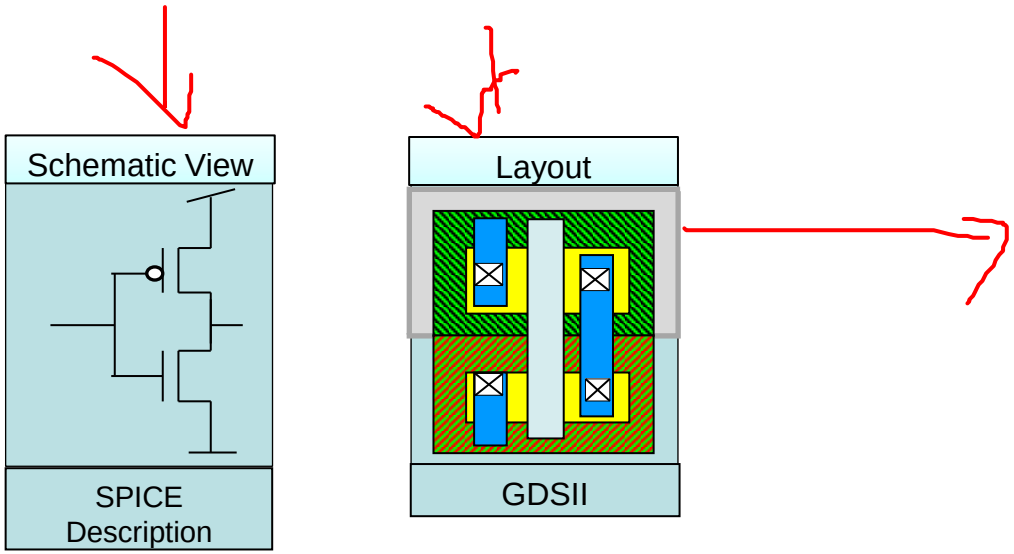
Extracted Netlist





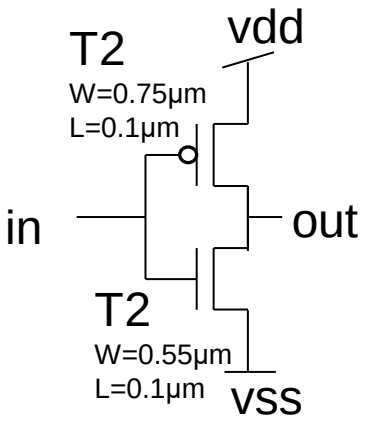
Deliverables

- Completed design is a set of files which represent different design views:
  - SPICE netlist format is used to deliver schematic view
  - GDSII binary format is used to deliver layout of the circuit



SPICE Description Example

- SPICE is a hardware description language (HDL) which enables to describe circuit at device level
- It has text-based format so is readable and can be easily modified

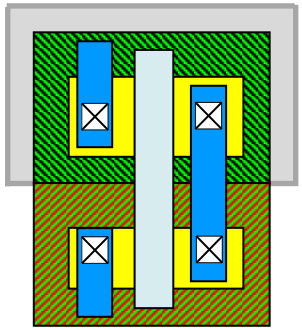


Inverter.sp

```
.subckt inverter
        mt1 out in vdd nmos l = 0.1u w = 0.75u
        mt2 out in vdd pmos l = 0.1u w = 0.55u
.ends
```

An Example of GDSII File

- GDSII is binary format, therefore it is not readable



Inverter.gds

```
02000200 60000201 1C000300 02000600 .........`.... 000000
01000E00 02000200 60002500 01000E00 .....%.`..... 000010
42494C45 4C504D41 58450602 12002500 .%....EXAMPLELIB 000020
413E0503 14000300 02220600 59524152 RARY.."".....>A 000030
1C00545A 9BA02FB8 4439EFA7 C64B3789 .7K...9D./..ZT.. 00004
60000000 01000E00 02000200 60000205 ...`.........` 000050
58450606 0C001100 01000E00 02000200 .............EX 000060
0100020D 06000008 04000045 4C504D41 AMPLE..... 000070
0000F0D8 FFFF0310 2C000000 020E0600 .....,..... 000080
FFFF204E 00001027 0000204E 00001027 '...N ..'...N .. 000090
0000F0D8 FFFFF0D8 FFFFF0D8 FFFFF0D8 ..... 0000A0
00000004 04000007 04000011 04001027 '..... 0000B0
00000000 00000000 00000000 00000000 ..... 0000C0
```

- Here you can see the video for the last semester :

  https://drive.google.com/drive/folders/1K93besY9AgrdZlNq_c_bJpYxee_Clc17?fbclid=IwAR1MqeygRwDNeaRO6qVidAMxVs16s_jDGKZCdi4UvsEDaYzSAS0vgfLLT00

Micro wind tool

Please find the session video and the NAND gate video in the following playlist:
https://www.youtube.com/playlist?list=PLnyw1IVZpaTvffKO_v6z3TmVYxZEsiTU-

Session :
https://www.youtube.com/playlist?list=PLnyw1IVZpaTvffKO_v6z3TmVYxZEsiTU-&fbclid=IwAR2aURctuJ3Hdwltm2ORqST37kL86wQibK-ZZxVZmBxNDWZ-bLP4etO6cBE

an example for designing nand gate using microwind.
http://bit.ly/34jlTzX