DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

Digital Integrated Circuits - ENCS333

Dr. Khader Mohammad

Lecture #1

Introduction

Integrated-Circuit Devices and Modeling

OFFICE HOURS -SCHEDULE

D. Khader Mohammad Schedule

Day	8	½	9	½	10	½	11:15	11:25	12	½	13	½	14	½	15	½	16	½
Monday	O. H.				ENCS234/Bamieh105								ENCS313/Masri407					
Tuesday			ENCS333/Masri108				O. H		ENCS333/Masri108									
Wednesday	O. H.				ENCS234/Masri404								ENCS313/Masri407					
Thursday			ENCS333/Masri108				O. H		ENCS333/Masri108									

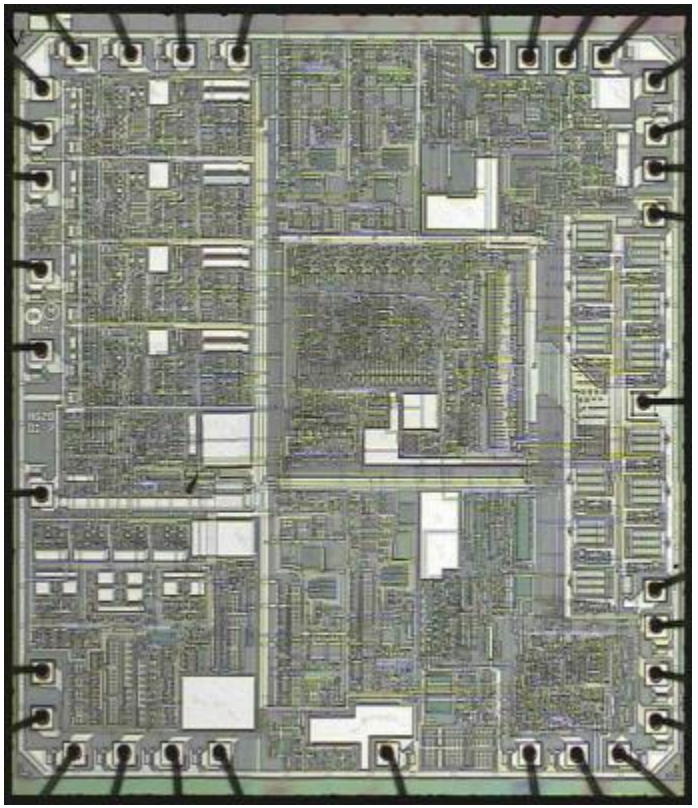
Assessment Policy		
Assessment Type	**Expected Due Date**	**Weight**
Short Exams//Quizzes	TBD	15%
Midterm Exam	TBD	30%
Projects/Assignments	TBD	20%
Final Exam	TBD	35%

Course content

	Course topics and Schedule
	Subject
1	Introduction to Digital Integrated Circuits Design
2	Semiconductor material: pn-junction, NMOS, PMOS
3	IC Manufacturing and Design Metrics CMOS
4	Transistor Devices and Logic Design The CMOS inverter
5	Combinational logic structures
6	Sequential logic gates; Latches and Flip-Flops
7	Layout of an Inverter and basic gates
8	Parasitic Capacitance Estimation
9	Device modeling parameterization from I-V curves.
	Short Test
10	Arithmetic building blocks
11	Interconnect: R, L and C - Wire modeling
12	Timing
	Power dissipation;
13	SPICE Simulation Techniques (Project)
14	Memories and array structures
	Midterm
15	Clock Distribution
16	Supply and Threshold Voltage Scaling
17	Reliability and IC qualification process
18	Advanced Voltage Scaling Techniques
19	Power Reduction Through Switching Activity Reduction
20	CAD tools and algorithms

Integrated circuits (ICs)

- Integrated circuits (ICs) are a keystone of modern electronics
- IC is a collection of electronic components – resistors, transistors, capacitors
- All stuffed into a tiny chip, and connected together to achieve a common goal
- Inside the IC : “The real “meat” to an IC is a complex layering of semiconductor wafers, copper, and other materials, which interconnect to form transistors, resistors or other components in a circuit.”
- IC Packages : The package is what encapsulates the integrated circuit die and splays it out into a device we can more easily connect to.

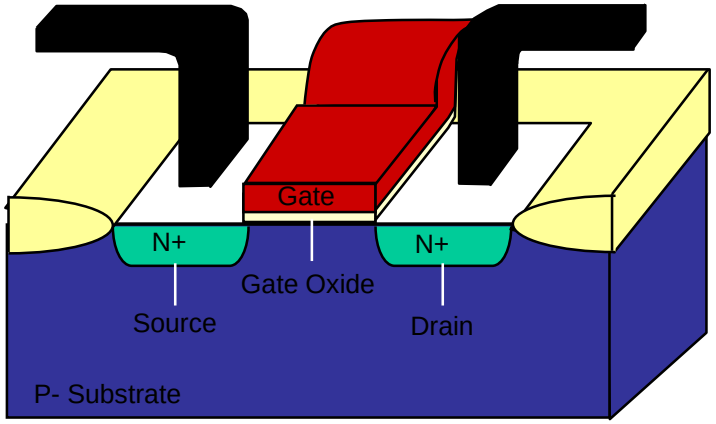


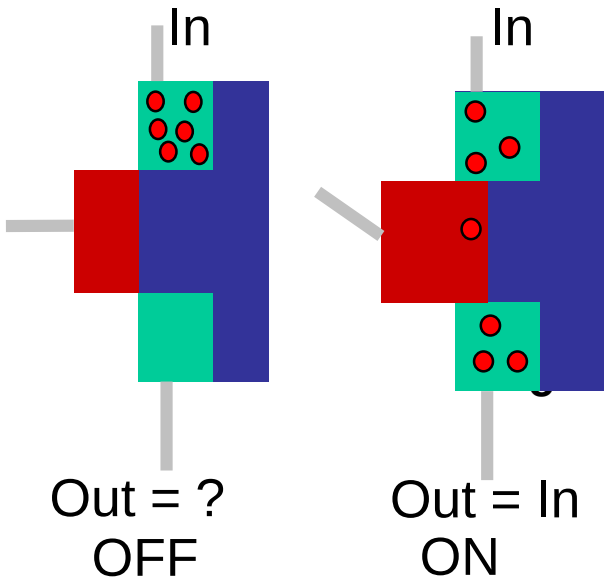
Digital Chips & Integrated Circuits)

- Chips are used everywhere:
  - Computers
  - Cellular phones
  - iPADs
  - iPhones
  - Gaming systems
  - DVD players, TVs
  - Watches
  - Cars
  - Medical devices
  - Pacemakers and coffee pots
  - Space stations
  - Greeting cards
  - . . .

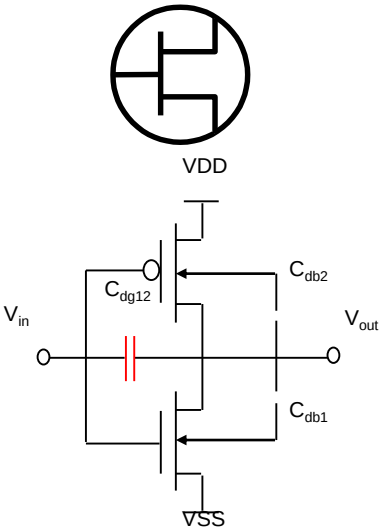
Basic Element

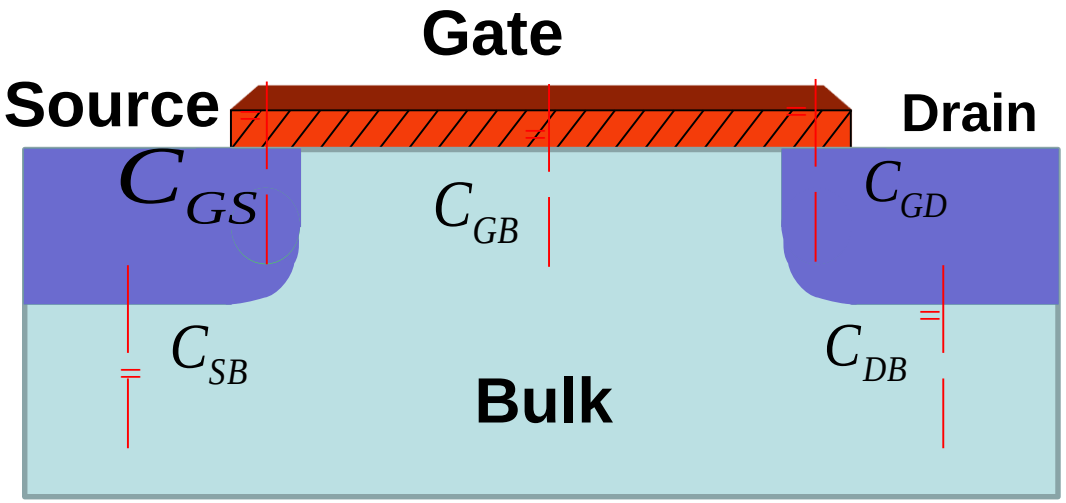
- CMOS Transistor is a switch





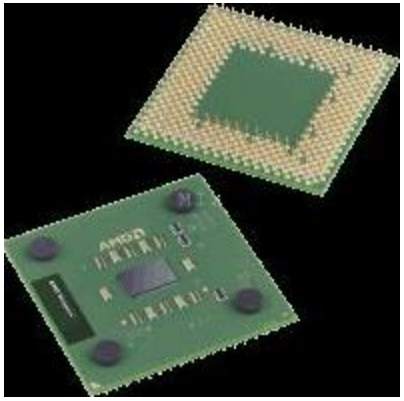
Smallest element in IC

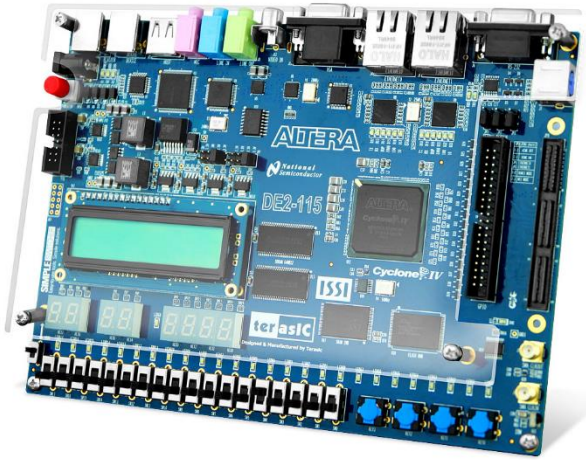


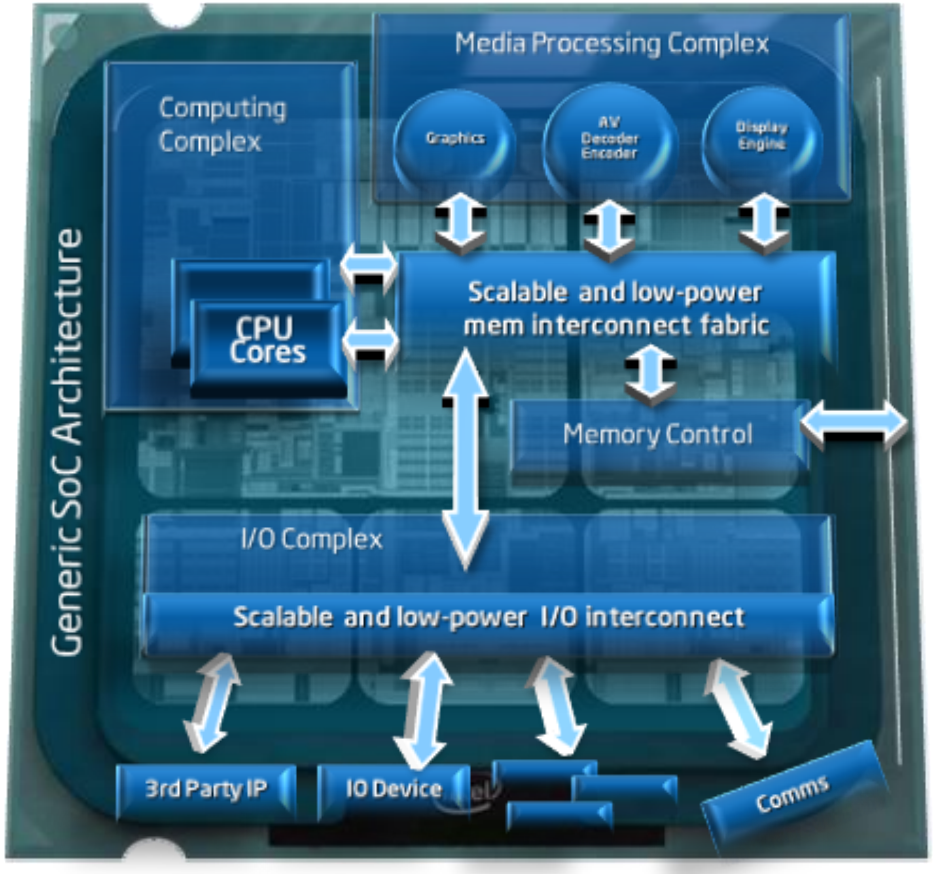


Useful

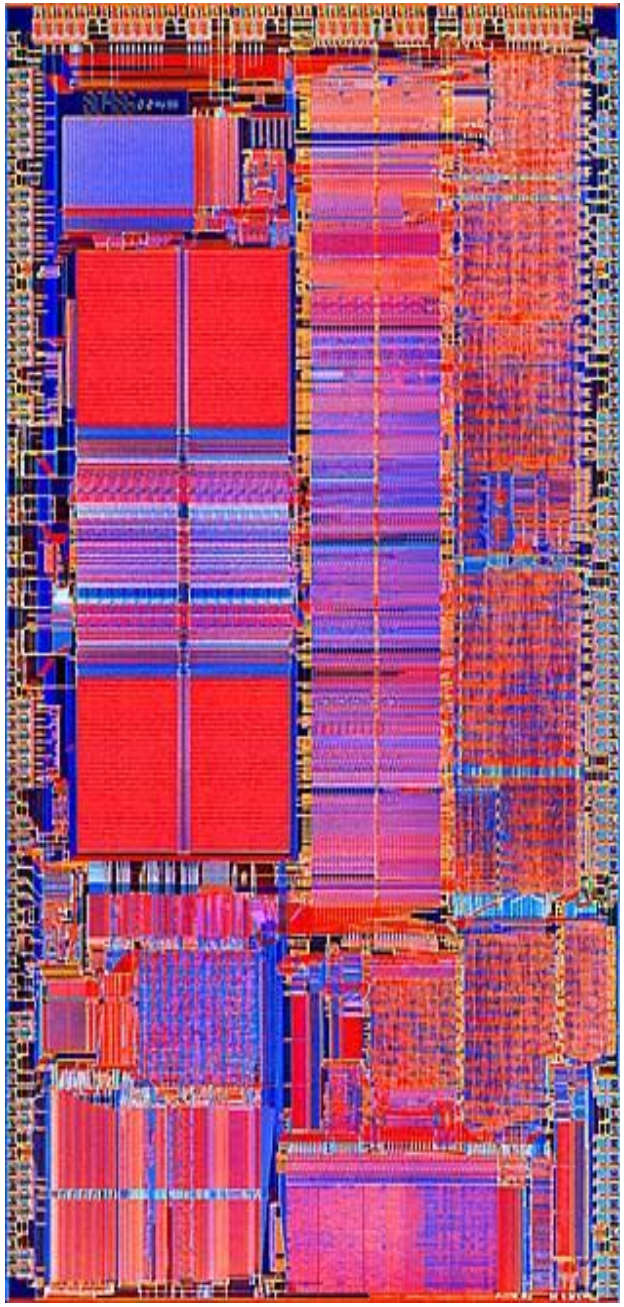
Parasitic



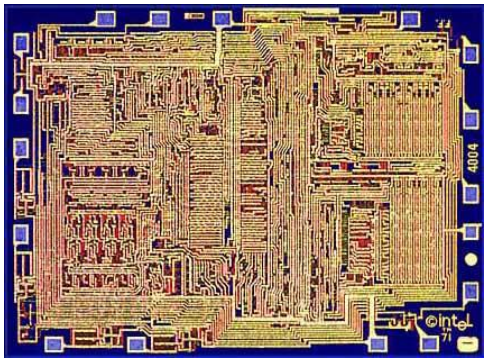

ALTERA
DE2-115
Cyclone IV
ISSI
terasic


Generic SoC Architecture
Media Processing Complex
Computing Complex
Graphics
AV Decoder Encoder
Display Engine
CPU Cores
Scalable and low-power mem interconnect fabric
Memory Control
I/O Complex
Scalable and low-power I/O interconnect
3rd Party IP
IO Device
Comms

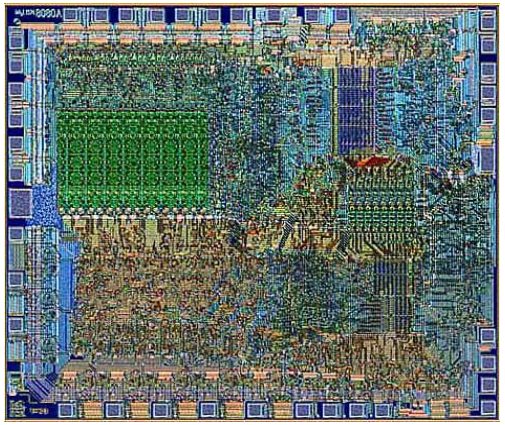
Intel 8486



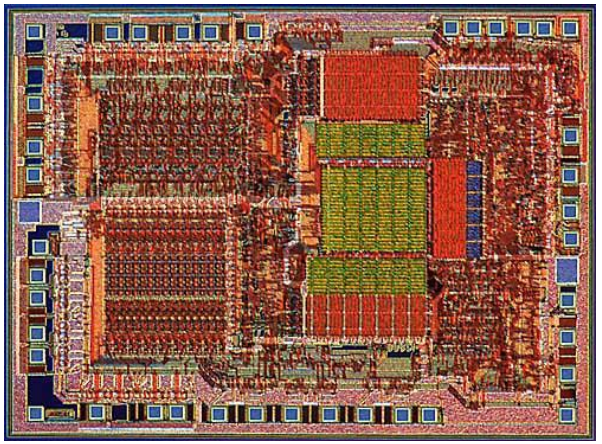
Technology Evolution: Intel CPU Chips



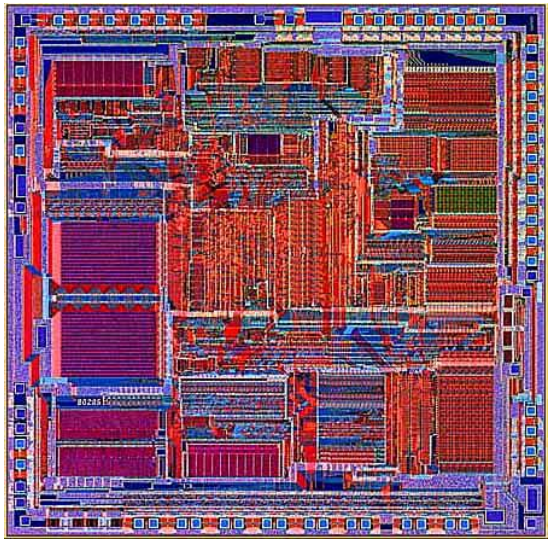
Intel 4004 (‘71)



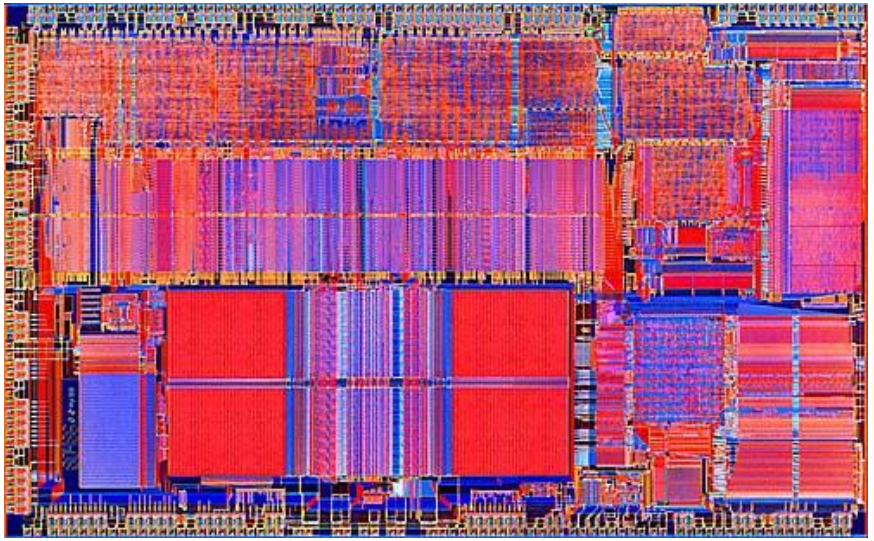
Intel 8080



Intel 8085



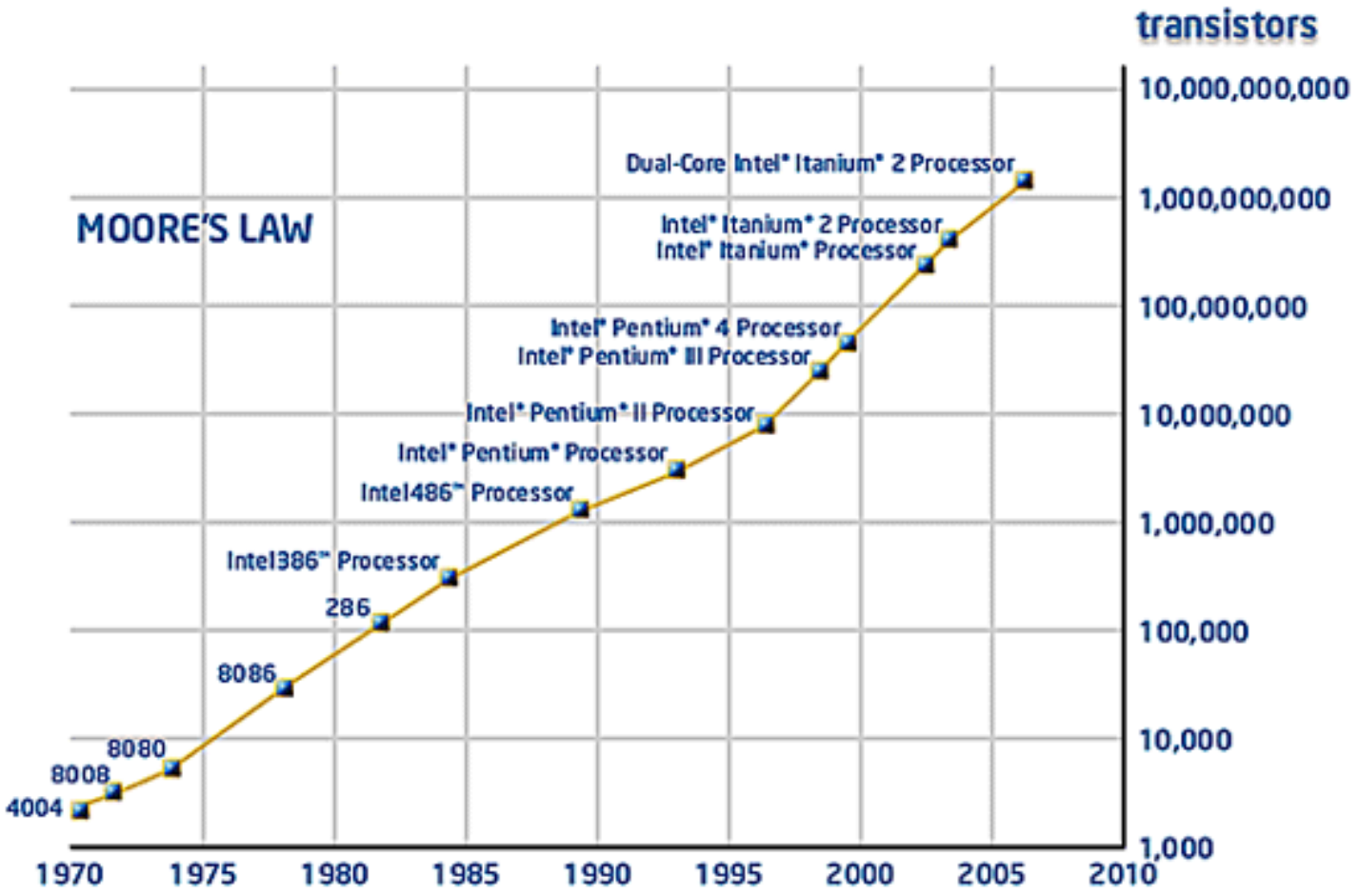
Intel 8286



Intel 8486

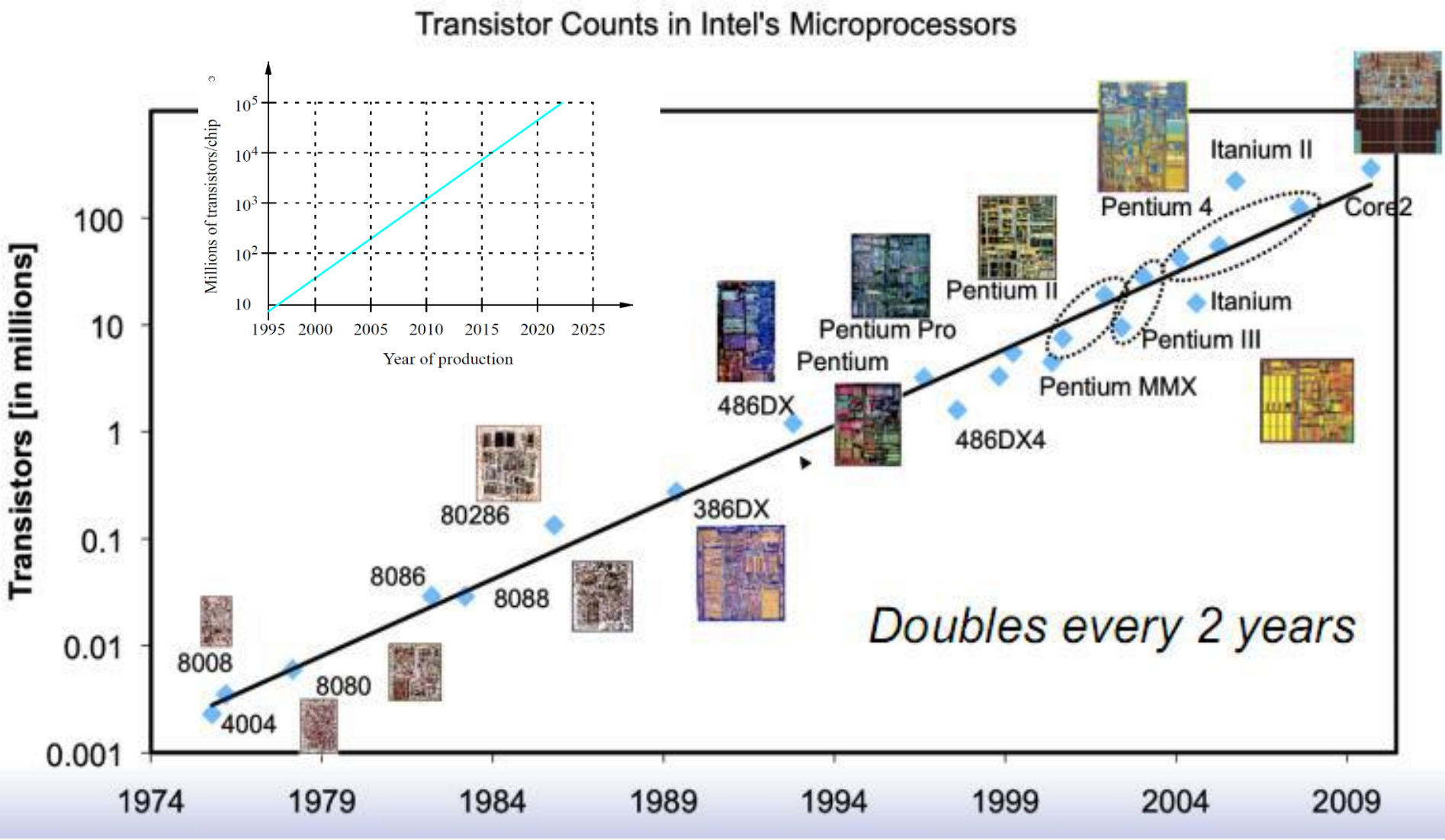
Courtesy Intel

Technology Scaling: Moore's Law



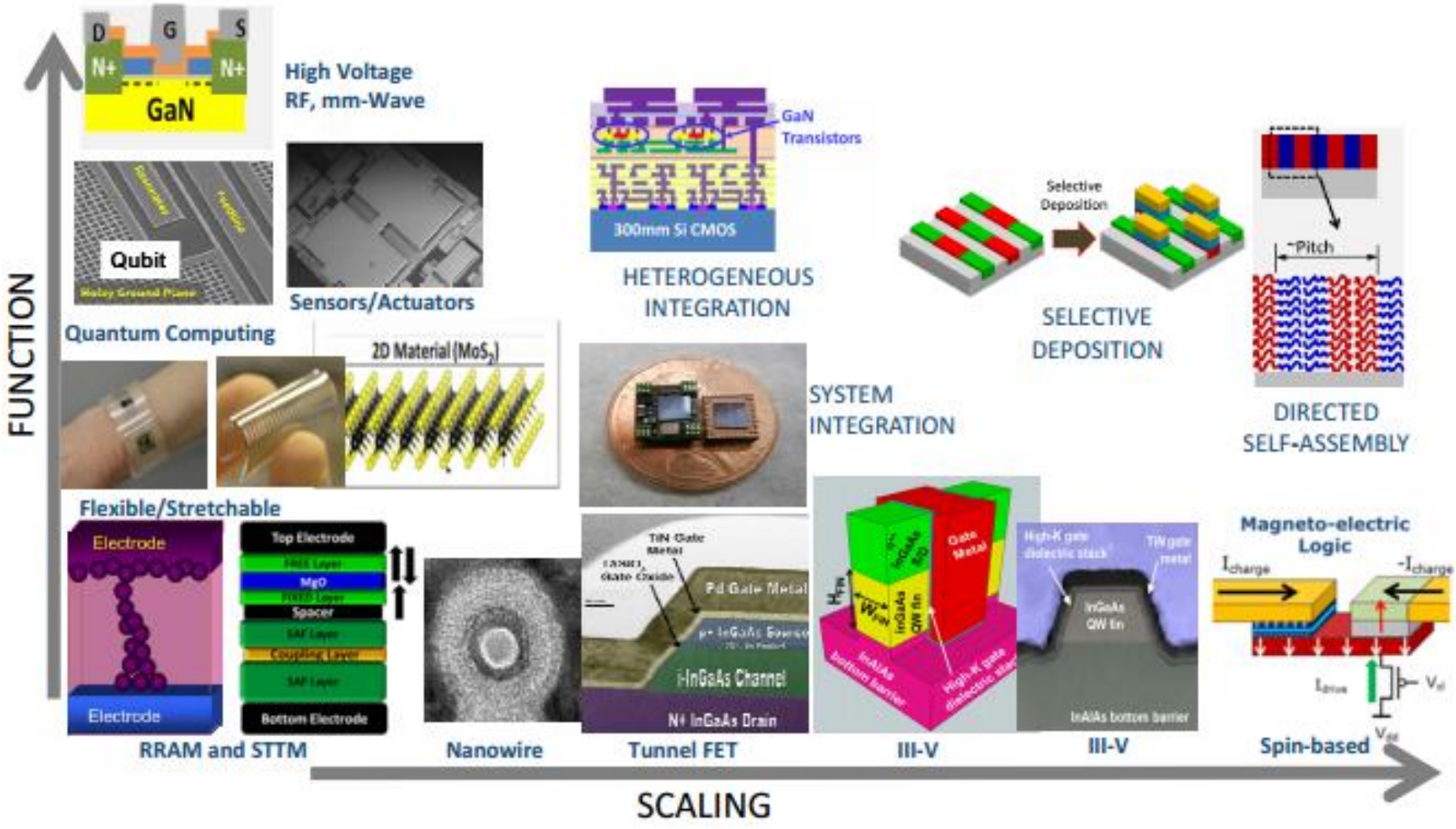
Courtesy Intel

Transistor Counts



An estimate of the maximum number of transistors per chip over time.

The Future is Full of Opportunity



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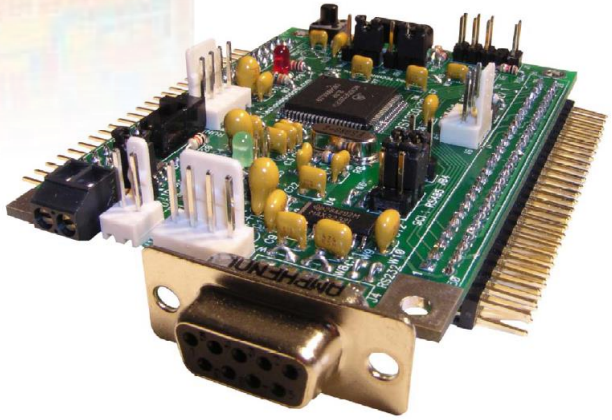
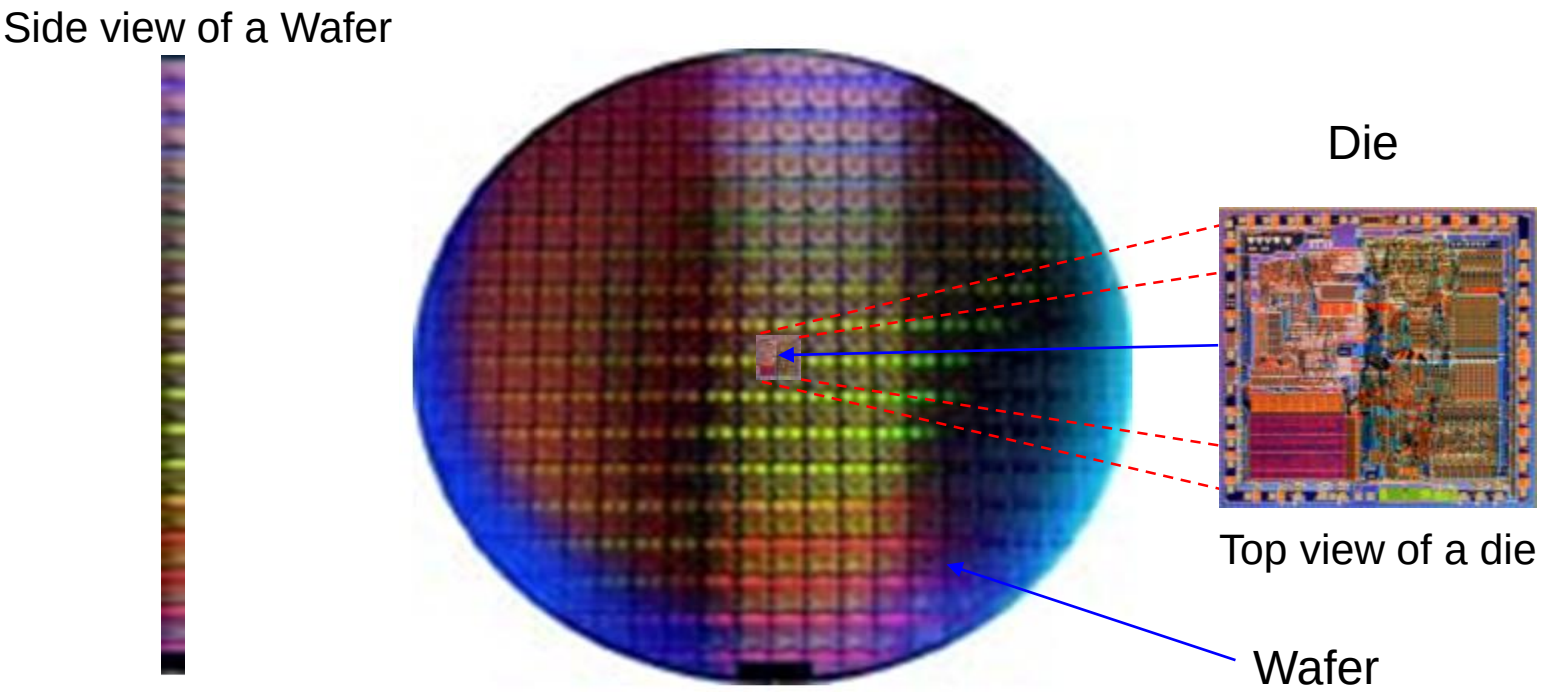
80x86 Evolution

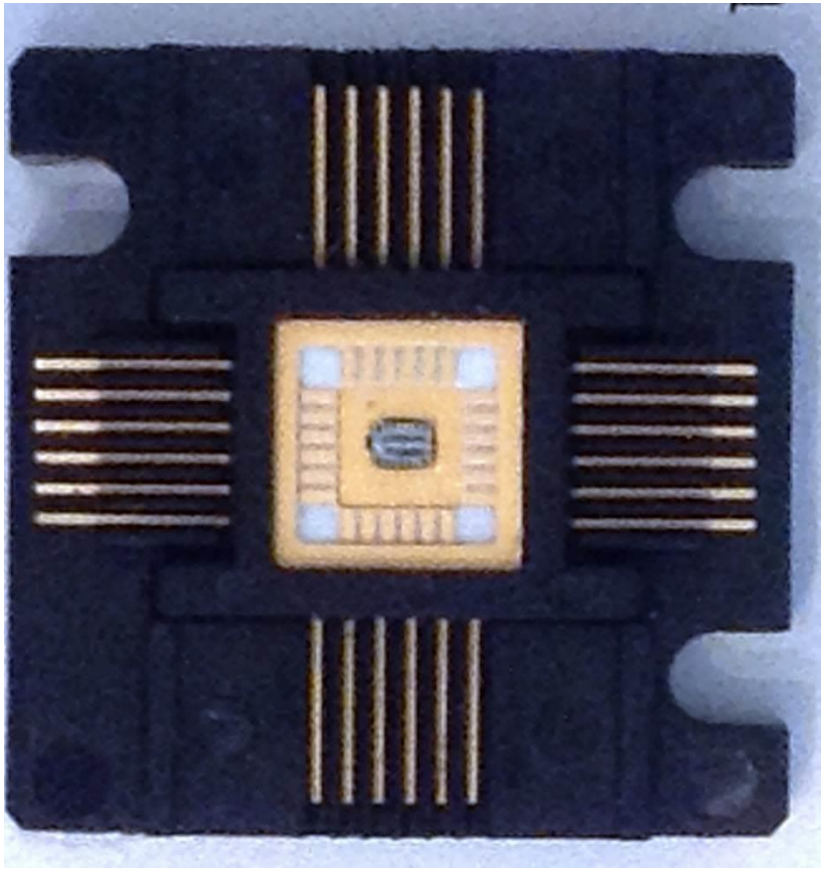


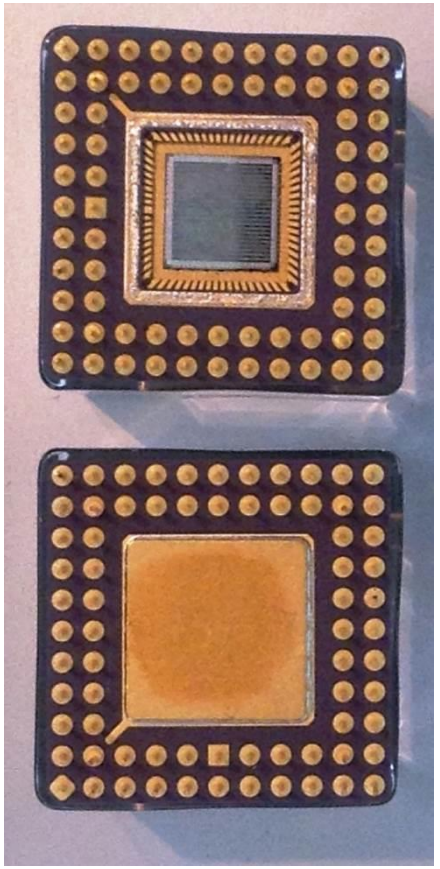
Wafer and Die

- CMOS ICs are fabricated on circular slices of silicon called wafers.
  - Wafer contains various identical dies.

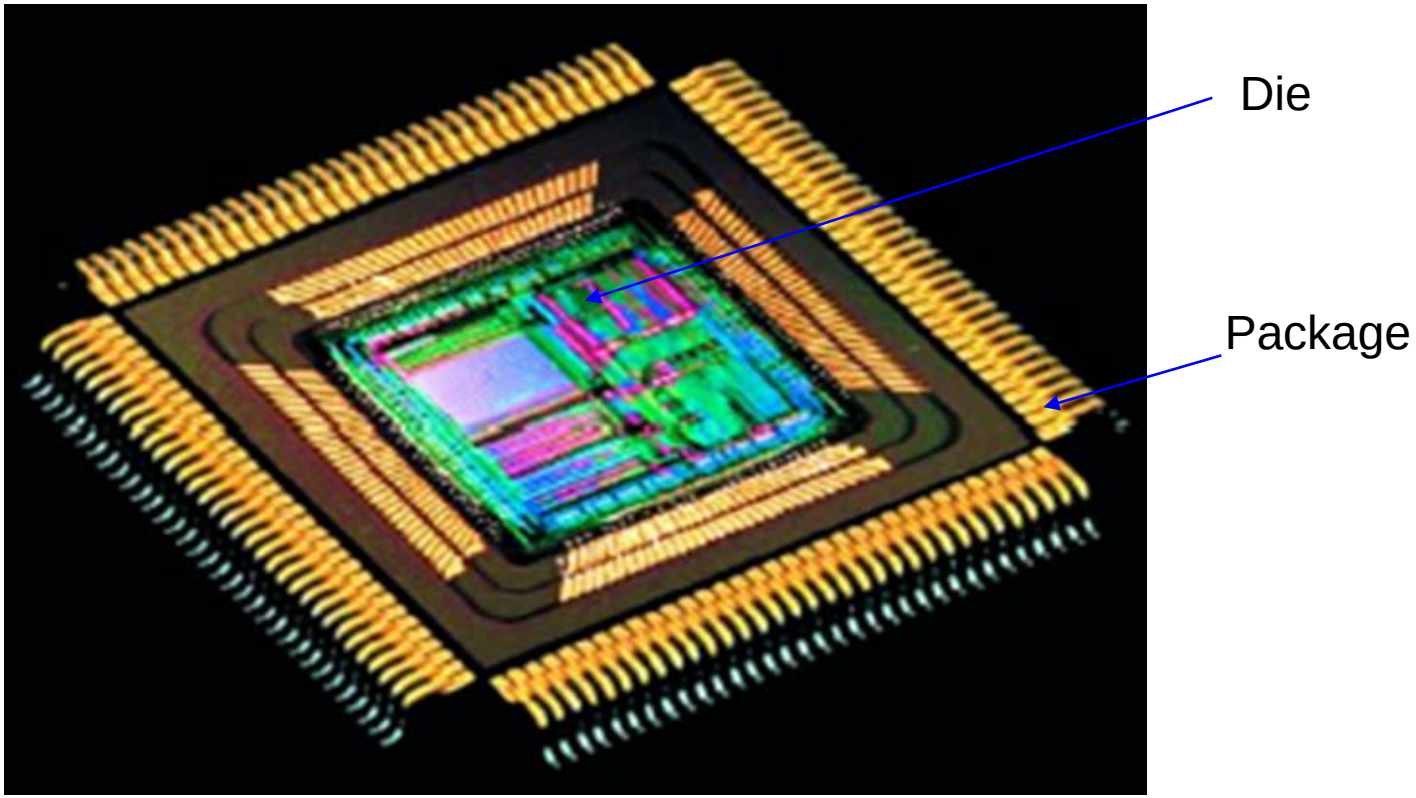


Chip Packages

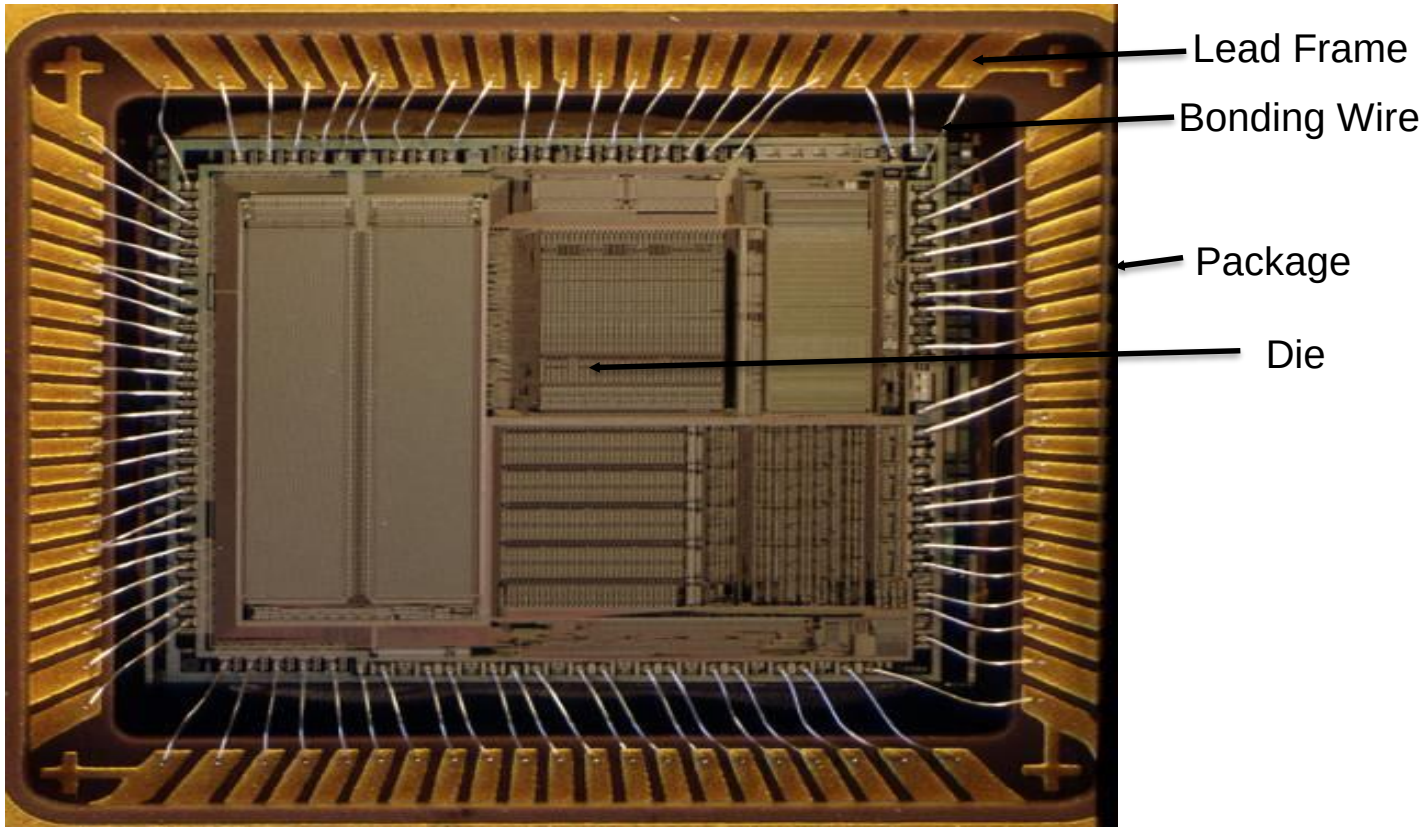




Die and Package

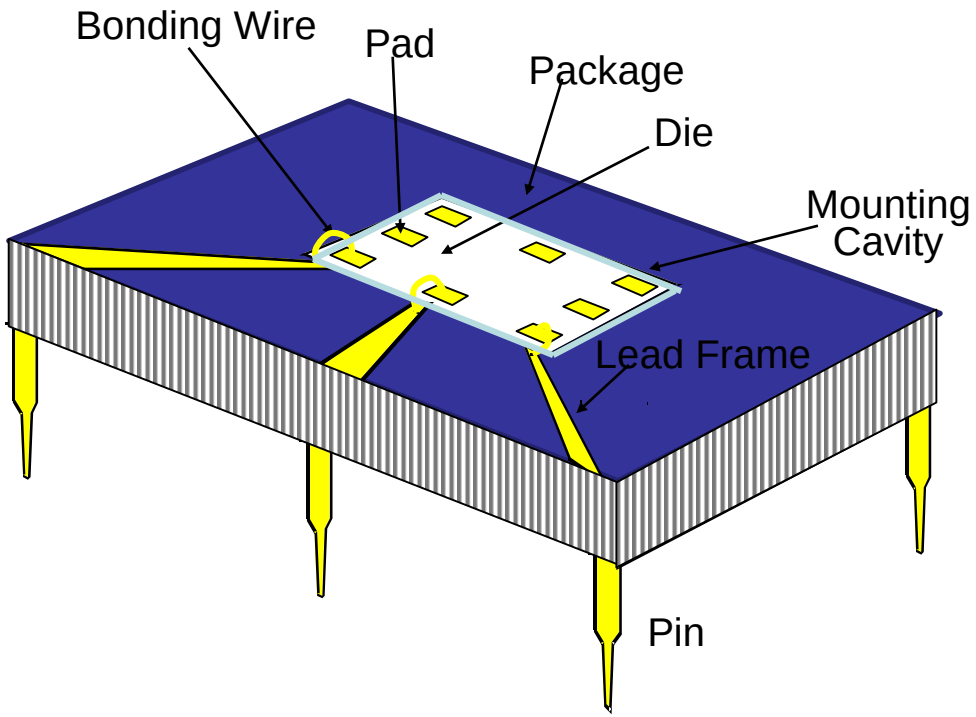


Packaging of Real IC



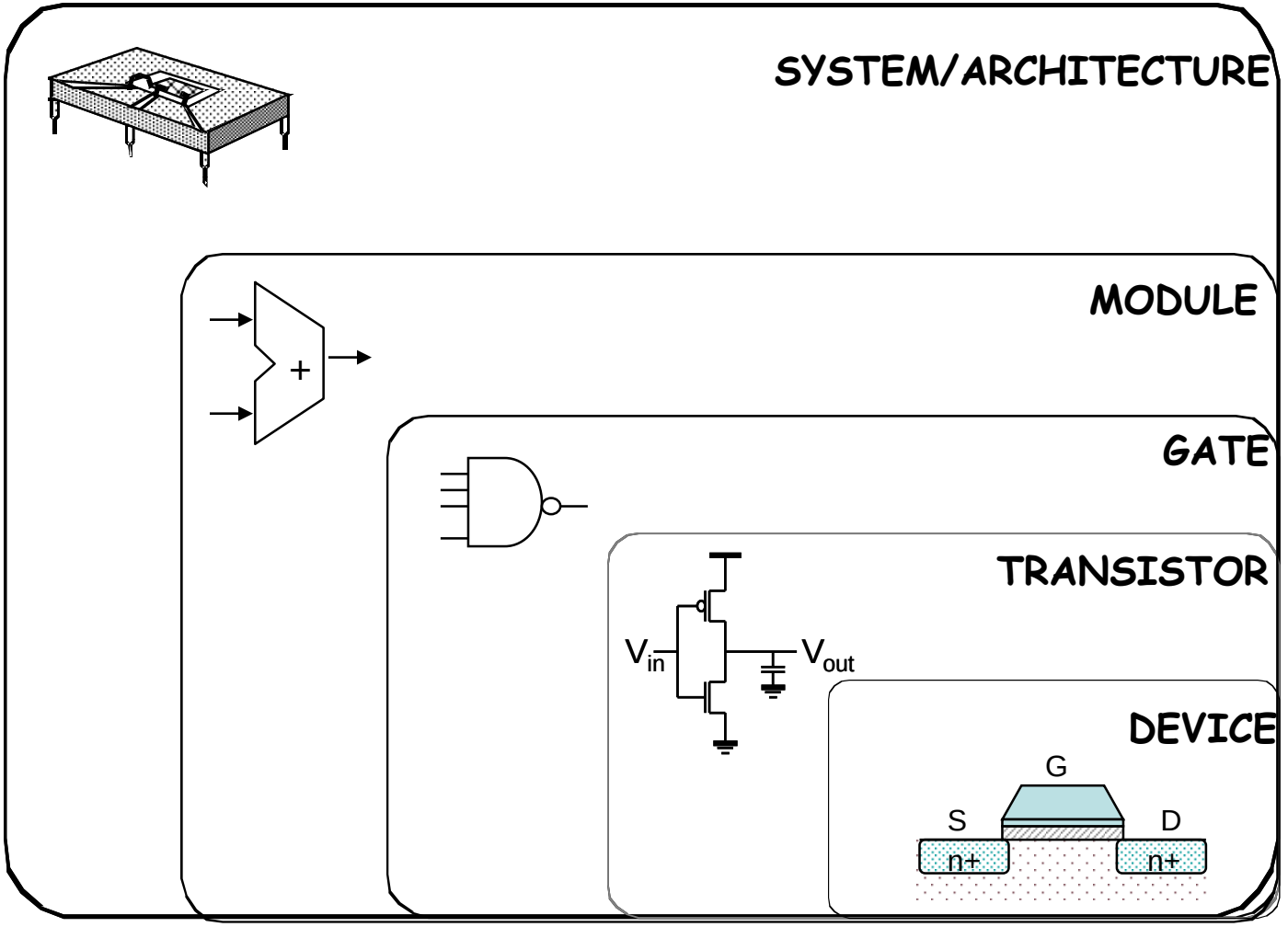
Chip Packaging

- Bonding wires connect the package to the chip.
- Pads are arranged in a frame around the chip.

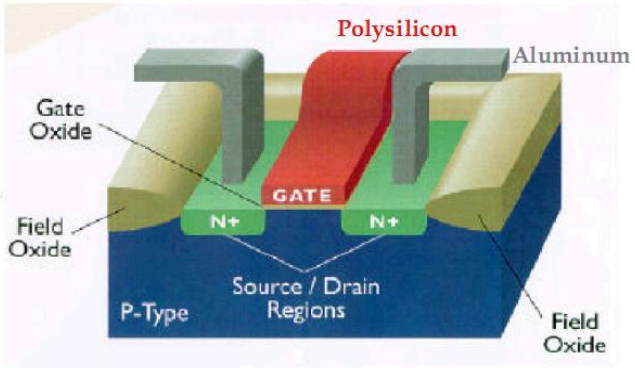


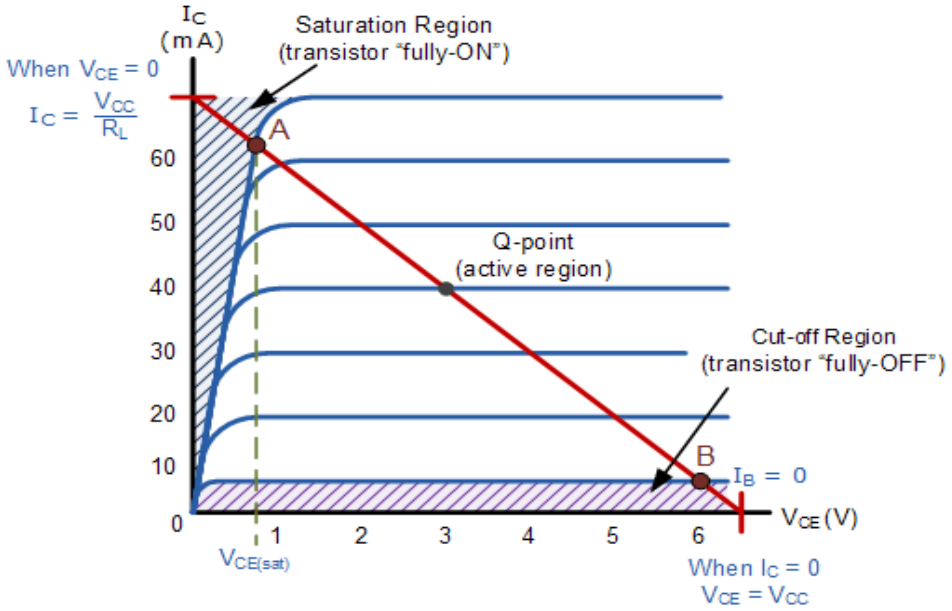
Chip, PCB

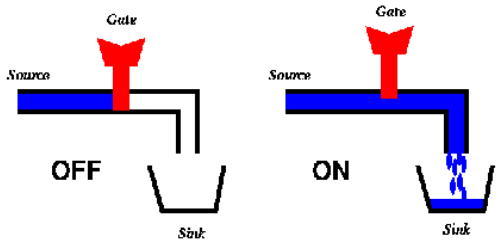
Design Abstraction Levels

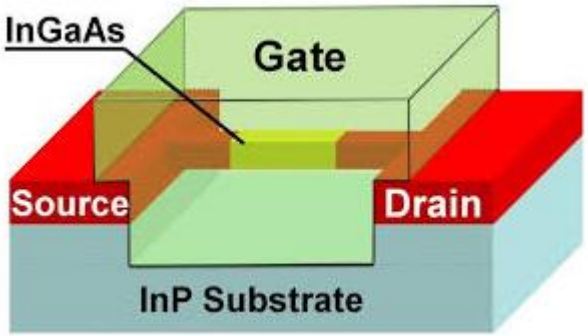


The MOS Transistor

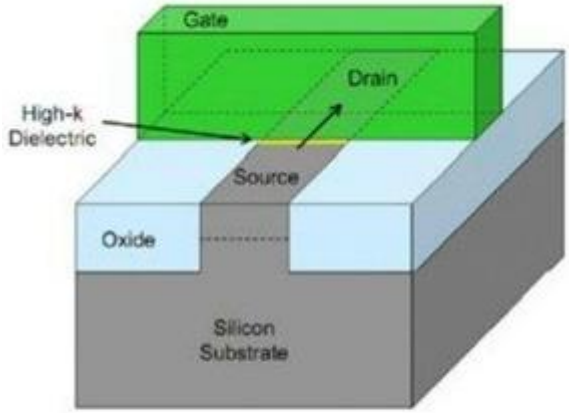






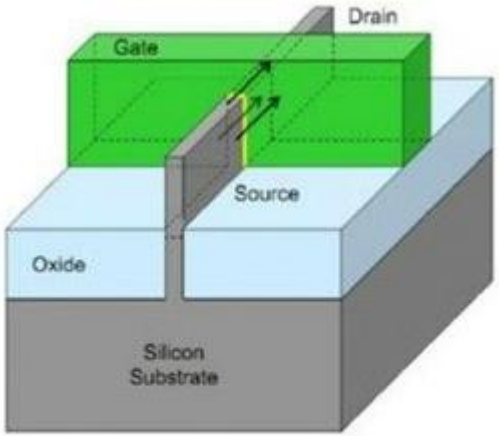


Traditional Planar



Traditional 2-D planar transistor form a conducting channel in the silicon region under the gate electrode when in the "on" state

3D FinFET

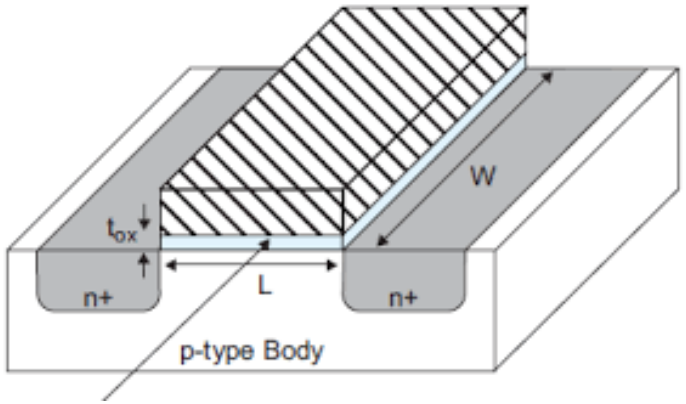


3-D Tri-Gate transistor form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

Process technology

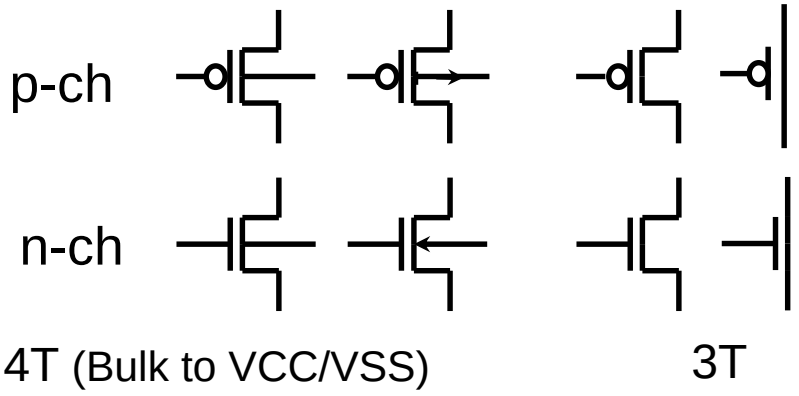
Intel Technology Roadmap

Process Name	P1266	P1268	P1270	P1272	P1274
Lithography	45 nm	32 nm	22 nm	14 nm	10 nm
1st Production	2007	2009	2011	2013	2015

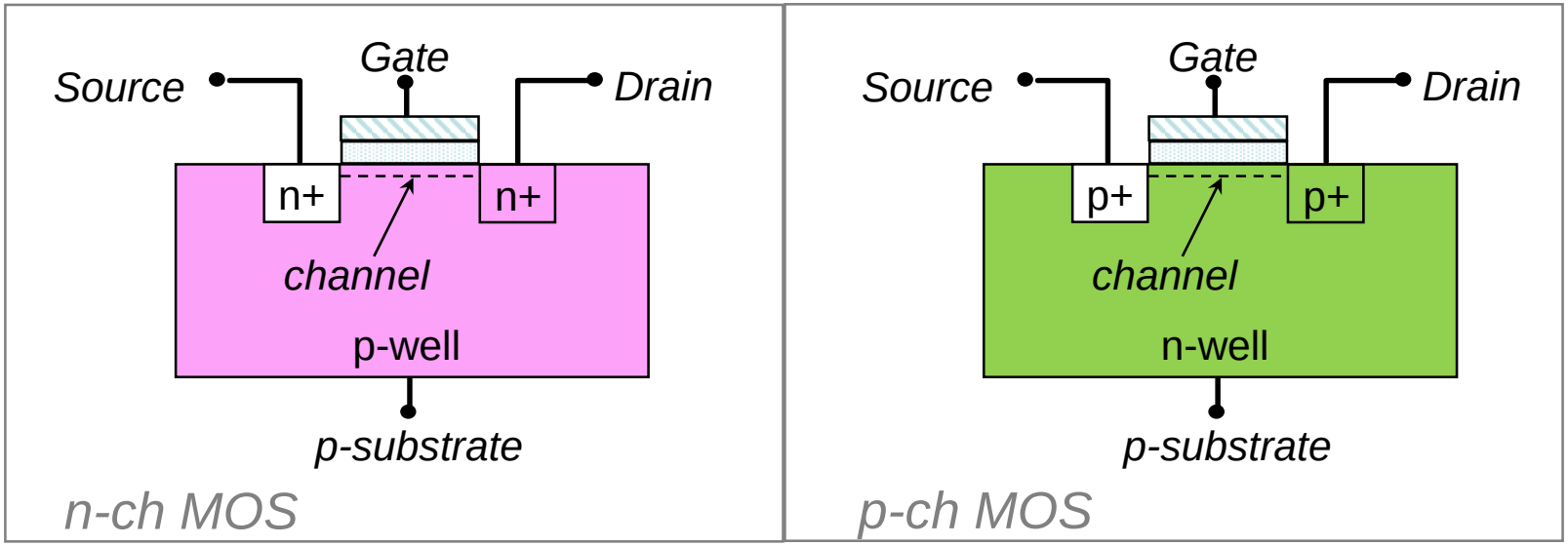


The MOS transistor

- Symbols:

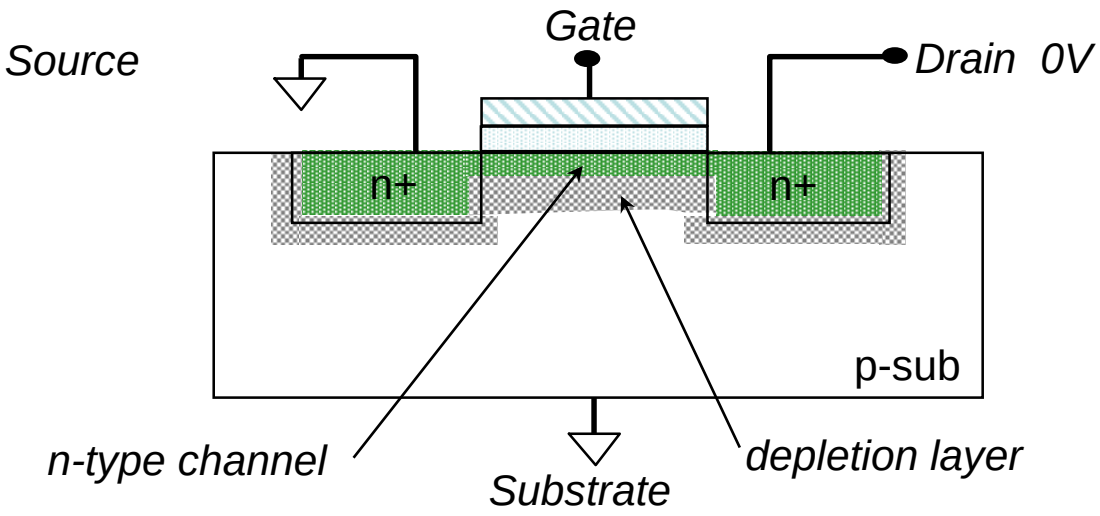


- Physical structure:

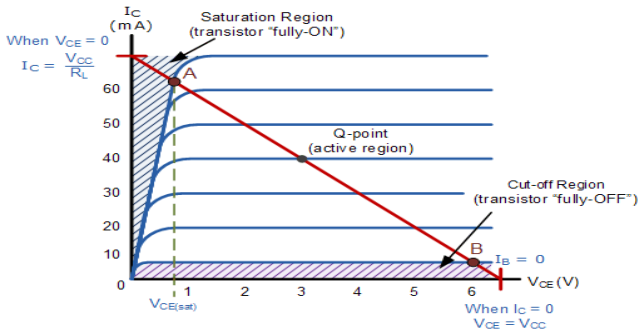


The MOS transistor - the different modes of operation

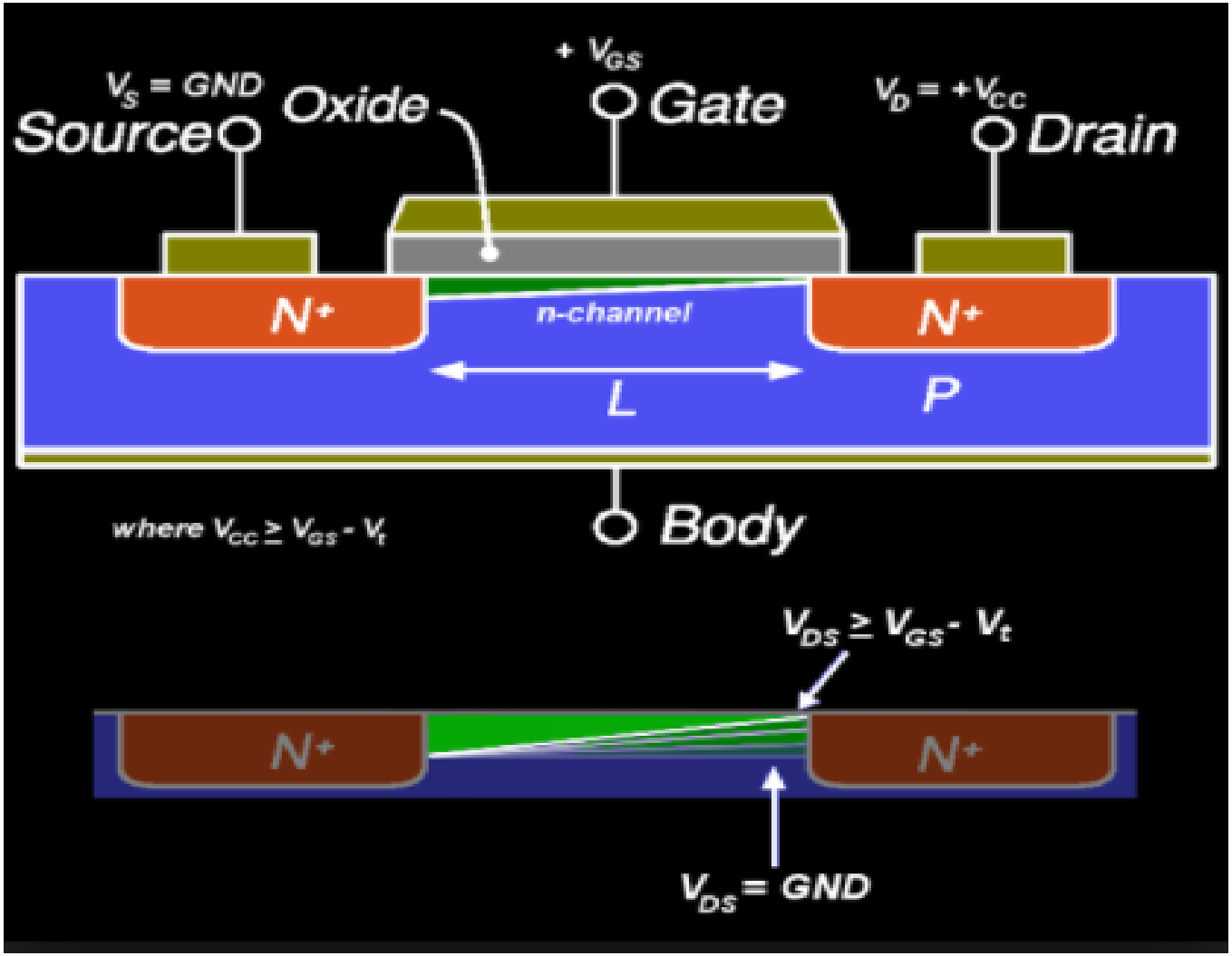
Vgs > Vt ; Vds=0V



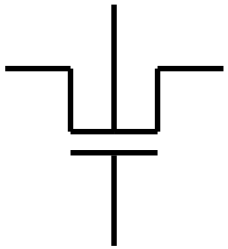
n-ch MOS

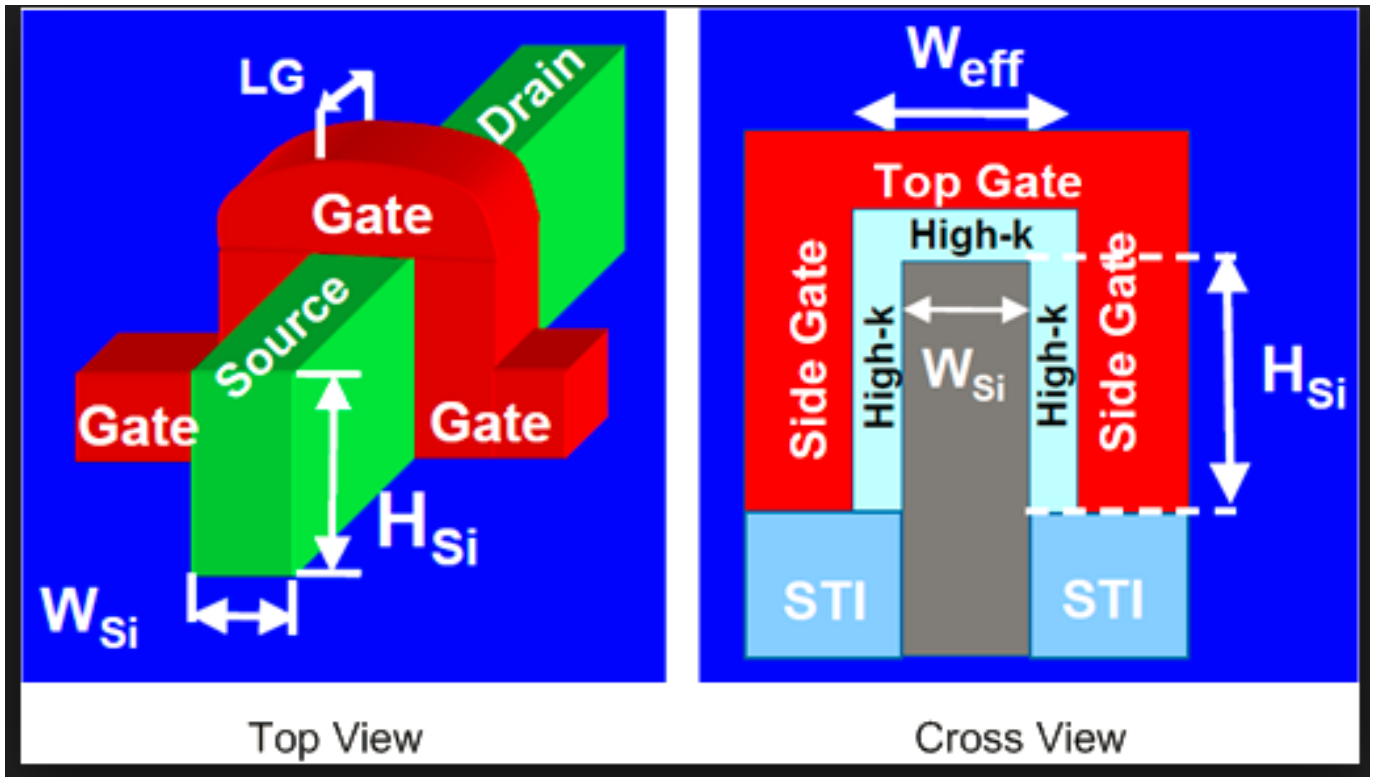


CMOS

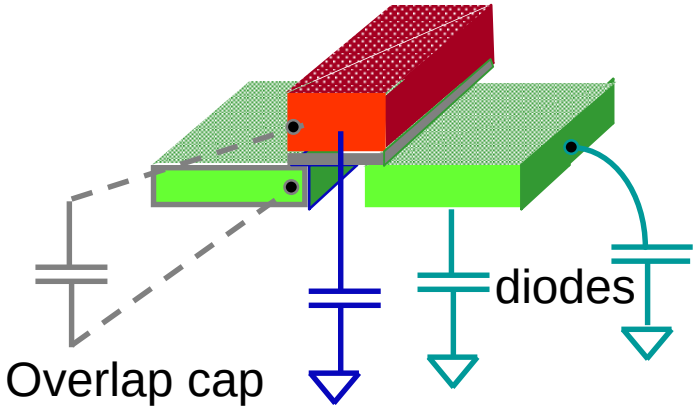

V_S = GND
Source
Oxide
+ V_{GS}
Gate
V_D = +V_{CC}
Drain
N+
n-channel
N+
L
P
where $V_{CC} \geq V_{GS} - V_t$
Body
$V_{DS} \geq V_{GS} - V_t$
N+
N+
V_{DS} = GND

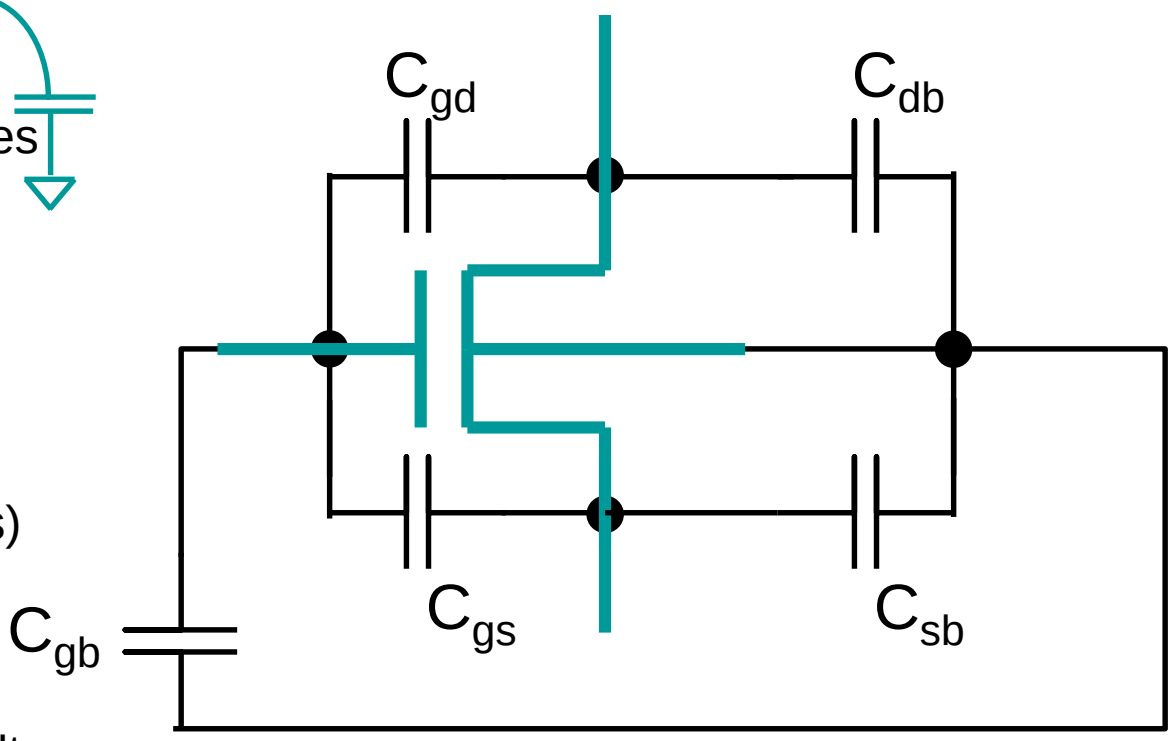
3D Gate




LG
Drain
Gate
Source
Gate
Gate
H_{Si}
W_{Si}
Top View
W_{eff}
Top Gate
High-k
Side Gate
High-k
W_{Si}
High-k
Side Gate
H_{Si}
STI
STI
Cross View

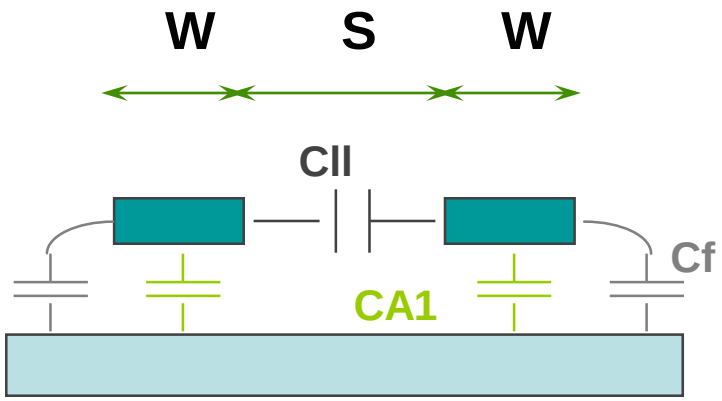
Capacitance of the MOS Transistor



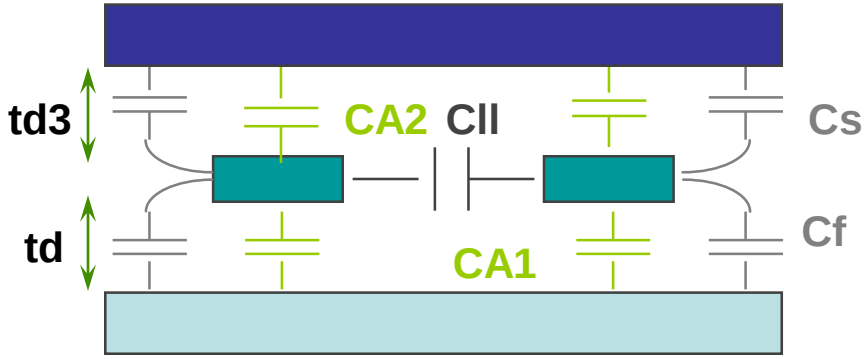


Parameters:
Diffusions area (diodes)
Diffusions perimeter (diodes)
Gate W (overlap cap)
Gate W*L (gate cap)
Doping profiles
Note: all capacitors have voltage dependence (not simple caps)

P1262 Line Capacitance Calculation



Pizza model

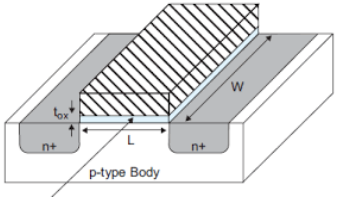


Sandwich model

Ctotal = Ca1 + Ca2 + 2*Cll + 2*Cf + 2*Cs

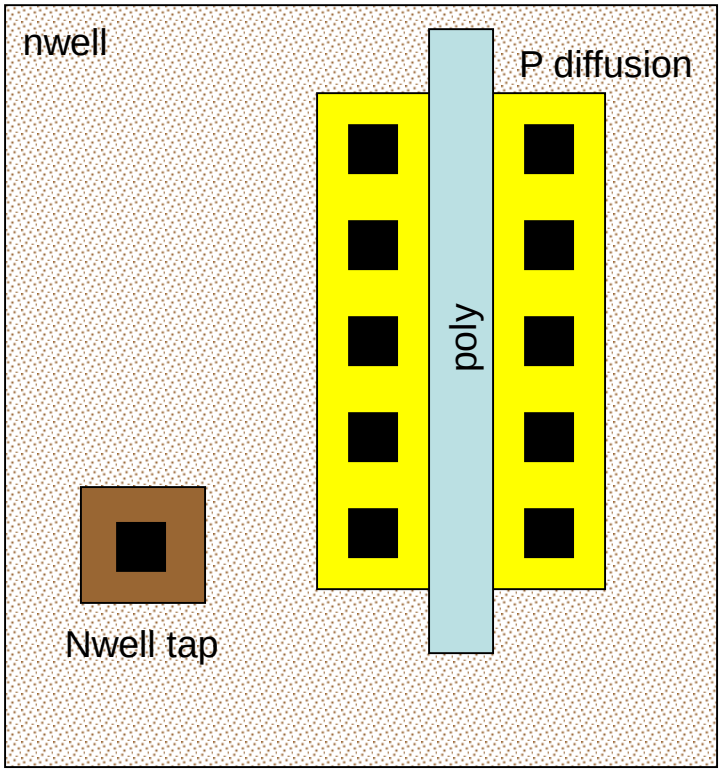
Layout

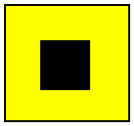
- Transistor defined as poly over diffusion

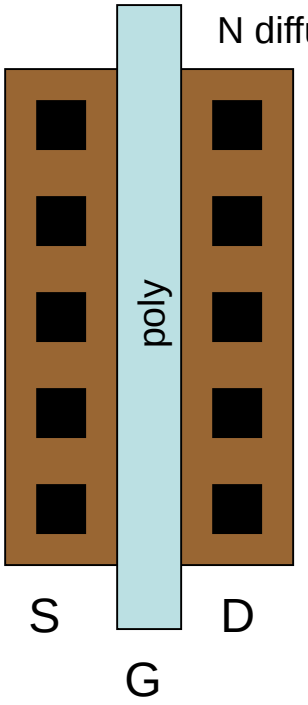


PMOS

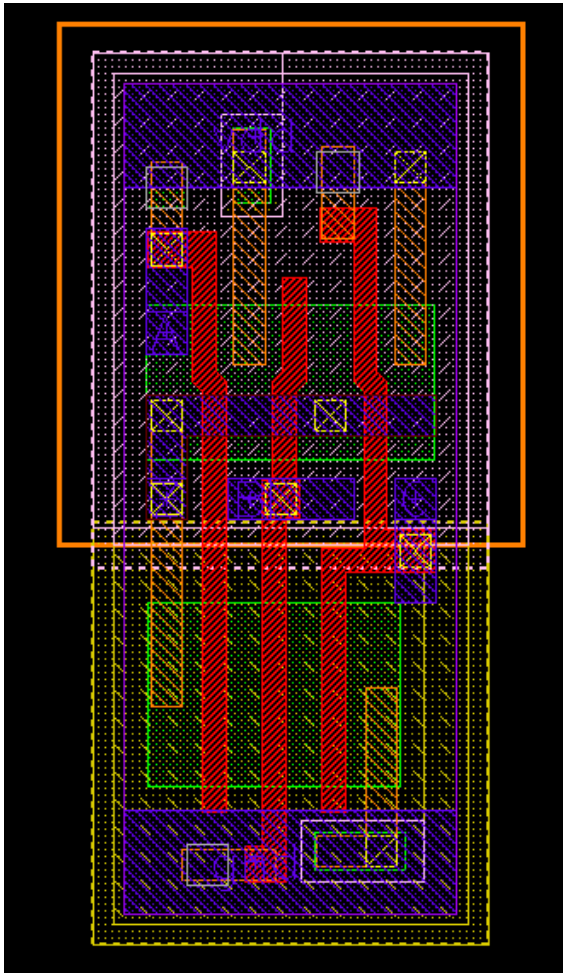
NMOS

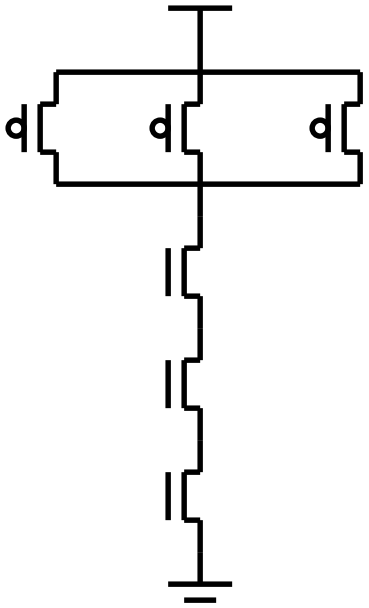




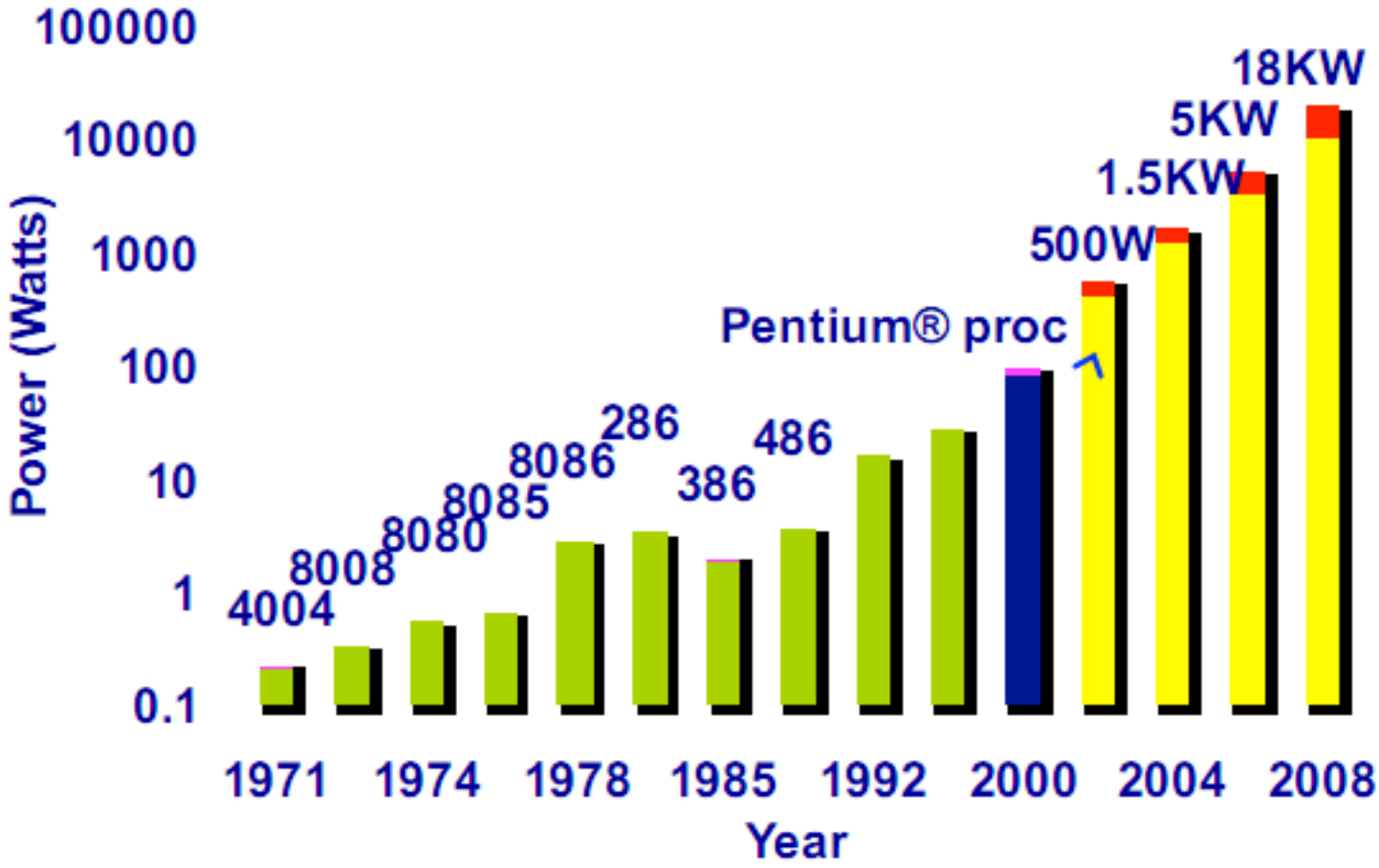


Layout vs. Schematic





Power Dissipation Prediction (2000)



- Did this really happen?

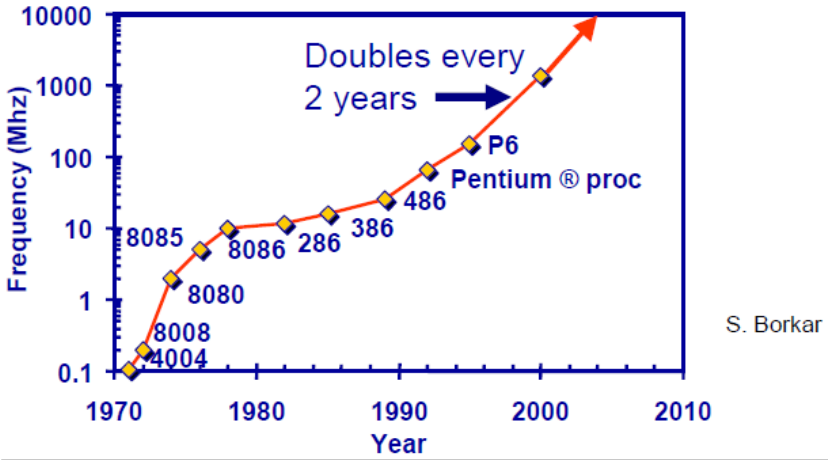
Challenges

- **Ultra-high speed design**
- **Interconnect**
- **Noise, Crosstalk**
- **Reliability, Manufacturability**
- **Power Dissipation**
- **Clock distribution.**

- **Time-to-Market**
- **Millions of Gates**
- **High-Level Abstraction**
- **Reuse & IP: Portability**
- **Predictability**
- **etc.**

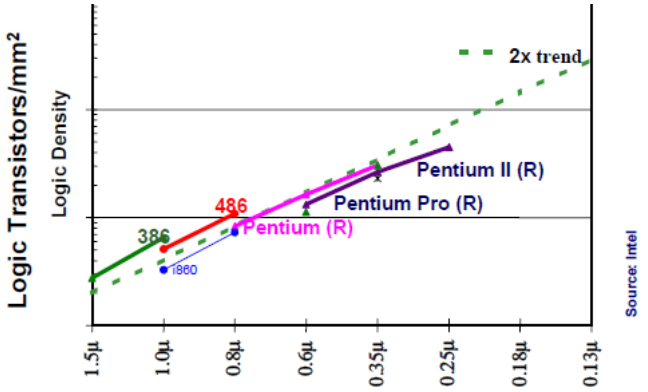
Challenges

Frequency/speed



Lead Microprocessors frequency doubles every 2 years

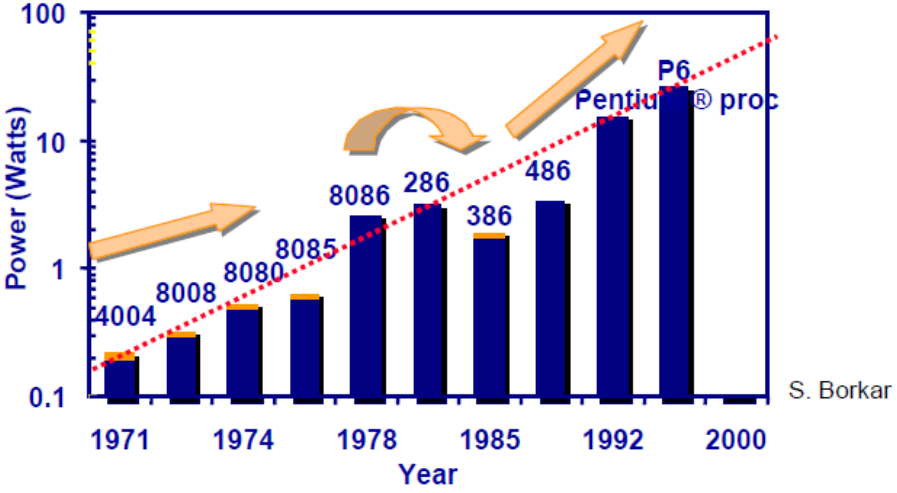
Moore's Law - Logic Density/Area



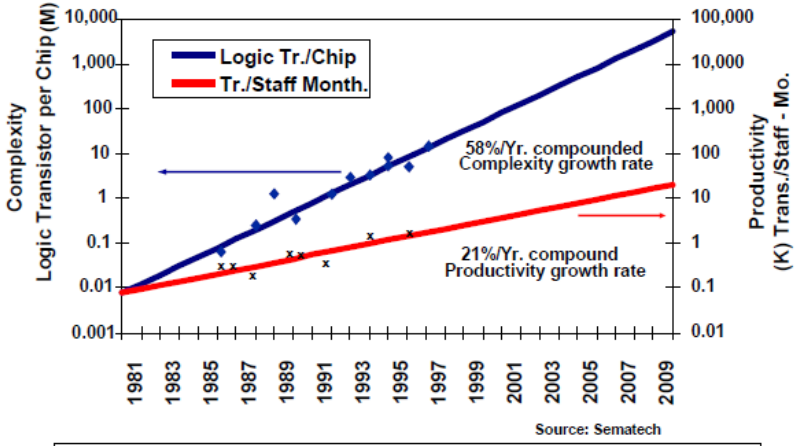
Shrinks and compactions meet density goals

New micro-architectures drop density

Power



Complexity outpaces design productivity



Suggested Reading

- What is a Circuit
- Polarity
- Semiconductor
- Resistors
- Diodes
- Capacitors
- Transistors