DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

Digital Integrated Circuits - ENCS333

Dr. Khader Mohammad

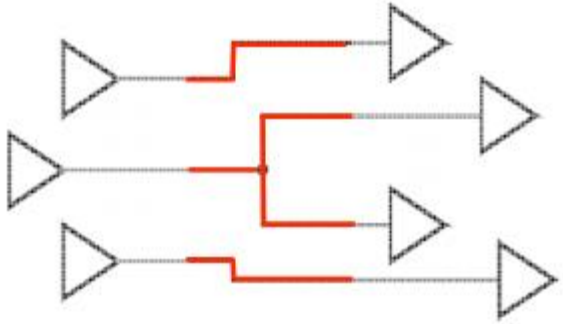
Lecture #10

Interconnect, R , C Wire modeling

Digital Integrated Circuits

	Course topics and Schedule
	Subject
1	Introduction to Digital Integrated Circuits Design
2	Semiconductor material: pn-junction, NMOS, PMOS
3	IC Manufacturing and Design Metrics CMOS
4	Transistor Devices and Logic Design The CMOS inverter
5	Combinational logic structures
6	Layout of an Inverter and basic gates
7 8	Static CMOS Logic Dynamic Logic
9	Sequential logic gates; Latches and Flip-Flops
10	Summary : Device modeling parameterization from I-V curves.
11	Interconnect: R, L and C - Wire modeling
12	Parasitic Capacitance Estimation
13	Timing
14	Power dissipation;
15	Clock Distribution
16	SPICE Simulation Techniques (Project)
17	Arithmetic building blocks
18	Memories and array structures
19	VOLTAGE, Package and protection
20	Reliability and IC qualification process
21	Advanced Voltage Scaling Techniques
22	Power Reduction Through Switching Activity Reduction
23	CAD tools and algorithms
24	SPICE Simulation Techniques (Project)

The Wire



Schematic

Physical

Agenda

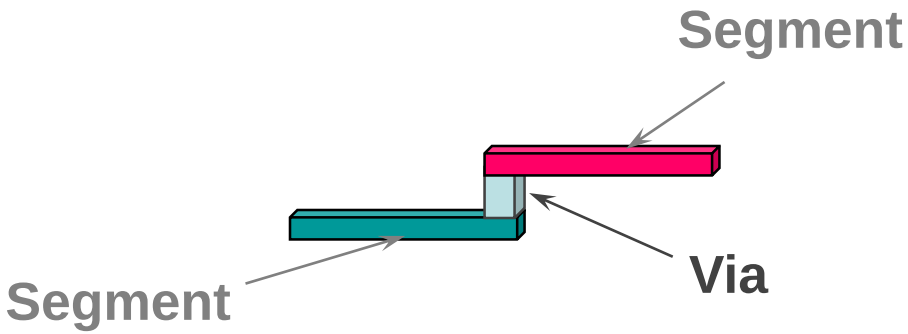
- Interconnect Definition
- RC Equation of a Line
- Interconnect Resistivity
- Interconnect Capacitance
- Cross Capacitance & Miller Effect
- Interconnect Modeling
- Repeaters
- Interconnect DO’s and DON’Ts

Interconnect Definition

- Interconnect is any net used to connect two different pins on the layout, commonly referred to as metal layer.
- Each process has a different number of metal layers.
- Each metal layer has specific electrical parameters defined by process file.
- The minimum width and minimum spacing provided by process process file.
- .

Interconnect Definition – Cont'd

- An interconnect net includes segments and Vias.
- Segment: Is a polygon of metal layer.
- Vias: Is the connection between segments from different metal layer.



Process example Layer's Properties

Layer	RC	Where to use it.
M1	Very High	Local interconnect.
M2	Very High	Local interconnect.
M3	High	Some internal buses
M4	Medium	Critical signals & buses in fub
M5	Medium_low	Clk, critical signals & buses
M6	Low	Clk, Full chip signals & buses
M7	Low	Clk, Full chip signals &buses

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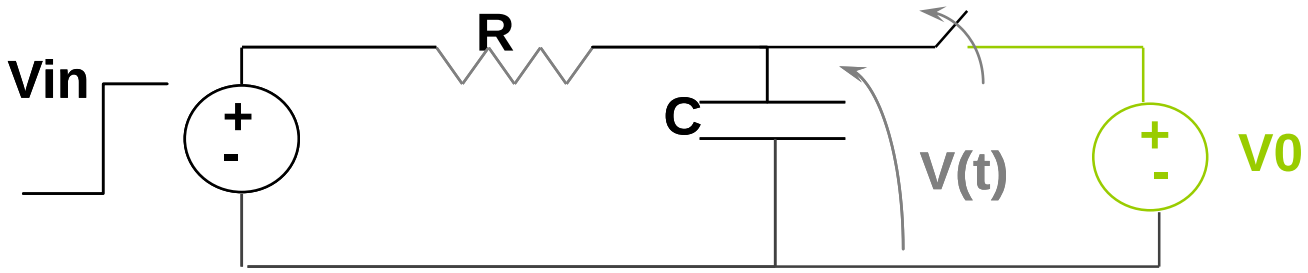
First Order Line model (RC Model)



Current law $I_R + I_C = 0$

$V/R + C\, dv/dt = 0$

$dv/V = -1/RC\, dt$

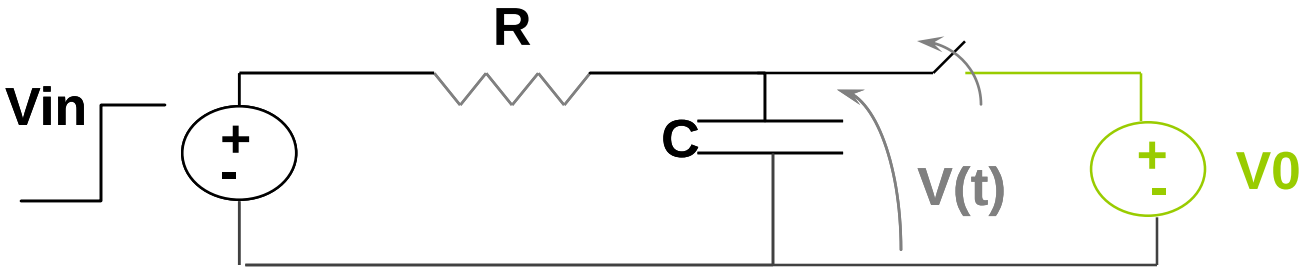
$\int dv/V = \int -1/RC\, dt$

$\text{Ln } V = -1/RC\, t + CON$

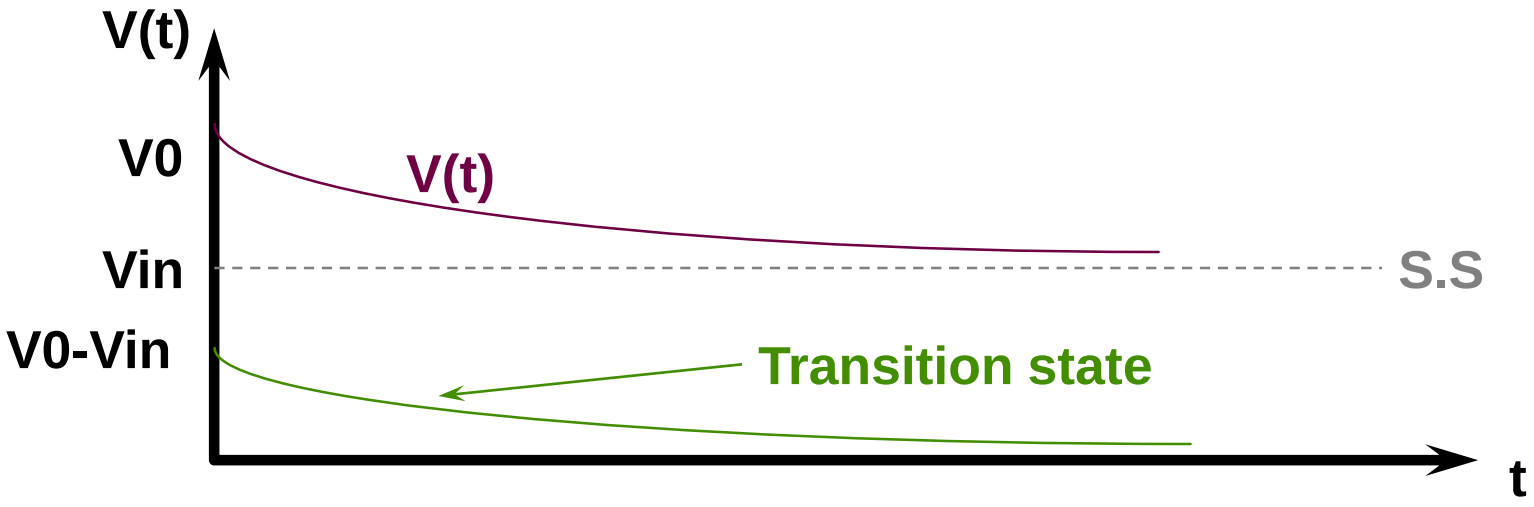
$V(t) = Ae^{-1/RC\, t}$

$V(t) = V_0 e^{-t/RC}$

First Order Line model (RC Model)



- $V(t) = V0\ e^{-t / rc} + Vin\ (1 - e^{-t / rc})$



Resistance, Capacitance & Inductance

RESISTOR

$$V(t) = R * i(t) \quad , \quad R = V / I = V / A = \Omega$$

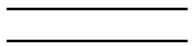
R

$$P(t) = I^2 R = V^2 / R \quad , \quad W(t0,t1) = R\int_{t0}^{t} I^2 \partial t = \frac{1}{R}\int_{t0}^{t} V^2 \partial t$$

CAPACITOR

$$Q(t) = CV \quad , \quad C = Q / V = A * Sec / V = FARAD$$

$$I(t) = \partial Q / \partial t = \partial (CV(t)) / \partial t = C \partial V / \partial t$$



C

$$V(t) = V(t0) + 1/c * \int_{t0}^{t} I(t) \partial t \quad P(t) = CV(t) \partial V / \partial t$$

INDUCTOR

$$\Phi(t) = L * I(t), \; L = \Phi / I = webber / A = V * Sec / A = Henry$$

$$V(t) = \partial \Phi / \partial t = \partial (LI) / \partial t = L * \partial I / \partial t$$

L

$$I(t) = I(t0) + \frac{1}{L}\int_{t0}^{t} V(t) \partial t \quad , \quad P(t) = L * I * \partial I / \partial t$$

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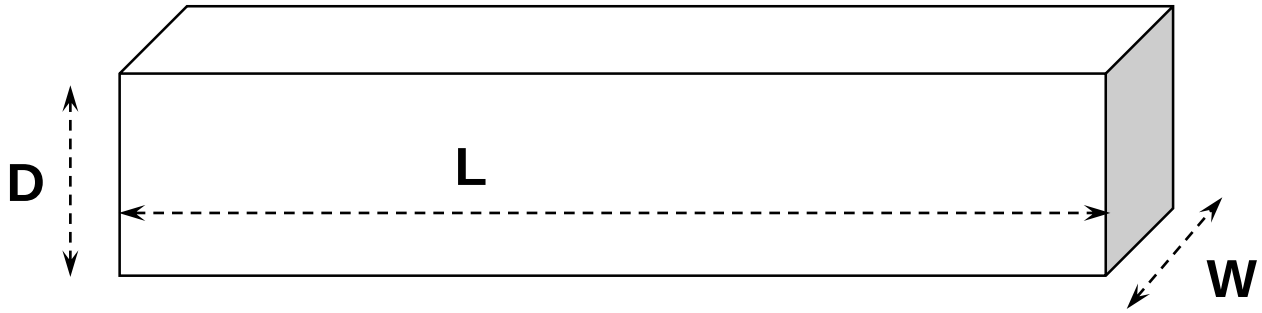
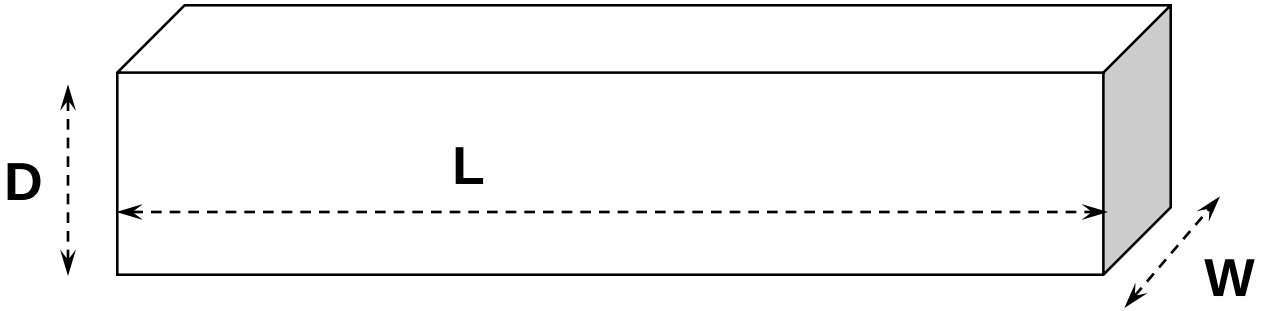
Line Resistance Simple Model



R = Rho * L / (W*D)

- "D" is a process fixed number per layer
- We can set the Length "L", and Width "W" of each segment
- This model does not include any temperature effect !!!

Segment Resistance Model in P1262



R = Rho * SQR * Tscal

Resistor per square given in process File (include D)

Len/(Wid+dlr) Number of Squares in segment.

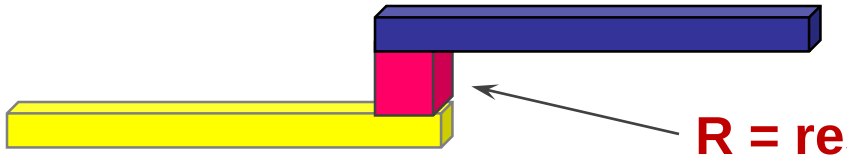
1+(te * (Temp-25)) Temperature Coefficient Process file parameters are given for “25C”

Segment Resistance Model Example

- The process files has two models for each metal layer
  - Undegraded: A model for normal operation mode
  - Degraded: A model of the line after 100,000 Hours of work under the Worst RV conditions

Metal layer	Rho	t_e	dlr
Metal 6 over Metal 5	4.22000e-05	5.53000e-01	-1.46800e-01
Metal 4 over Metal 3	8.35000e-05	3.64000e-01	-1.03000e-01
Metal 2 over Metal 1	1.08200e-04	2.92000e-01	-6.48000e-02

Via Resistance Model in P1262



R = res * (1 + (te * (Temp - 25)))

te,res : Are process file parameters given for a specified Via model

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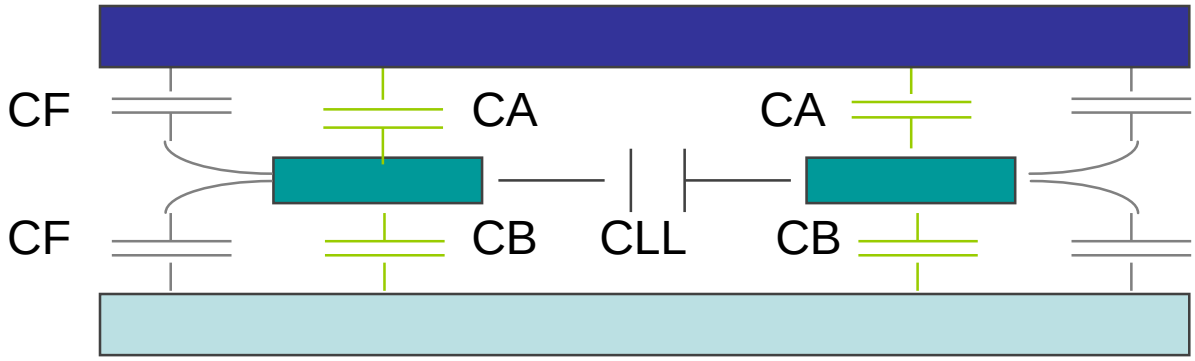
Interconnect Capacitance

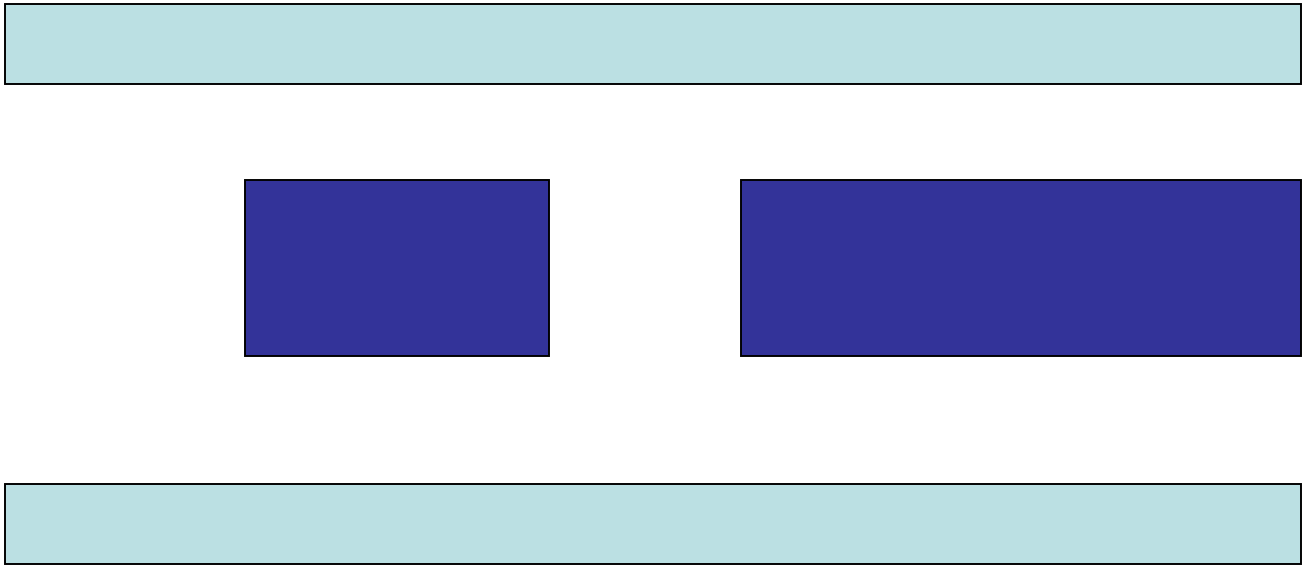


CLL Line to Line Capacitance.

CA, CB Capacitance to Other Plane.

CF Fringing Capacitance.

Solving a speed path.

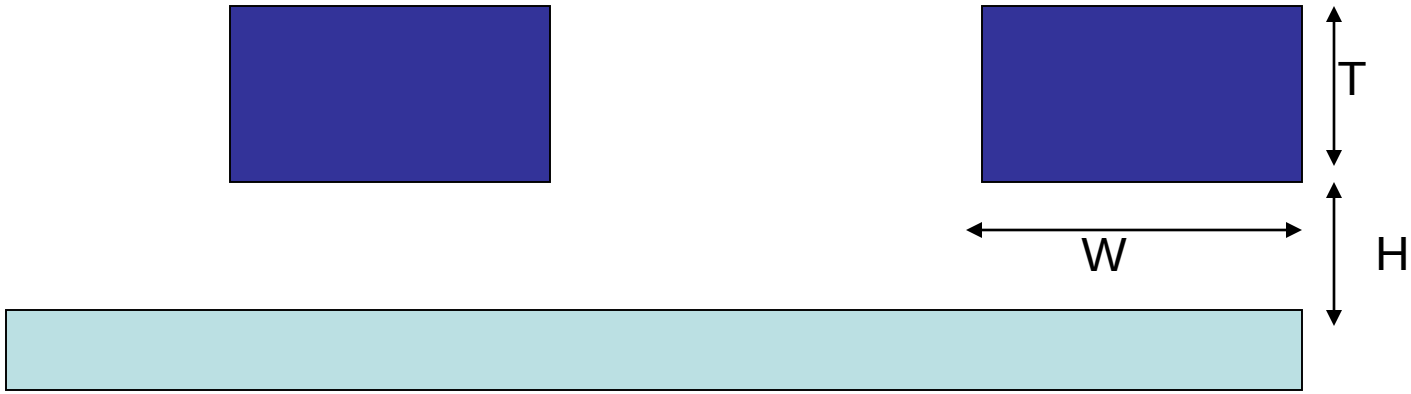


What happened to R?

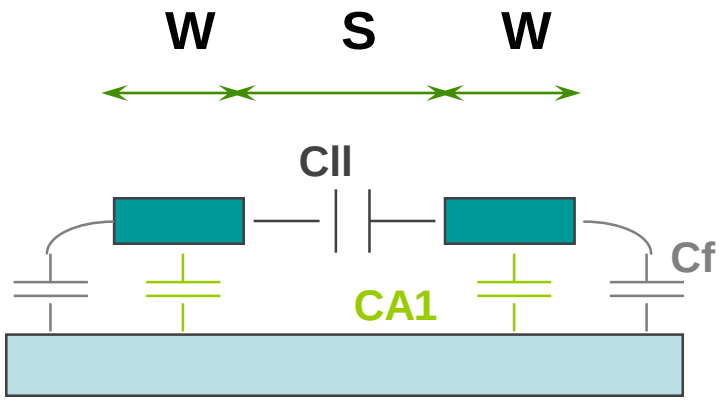
What happened to C?

Fringe Capacitance

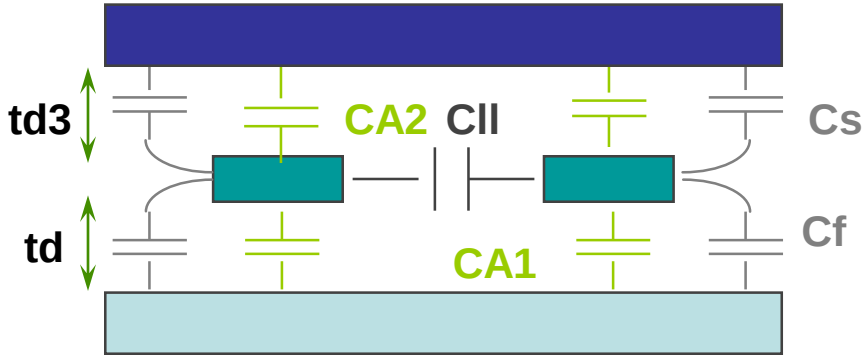
- As the process dimensions get smaller, the interconnect ratio (T/W) and (T/H) increases, since T has to increase to get a better resistance. Therefore Fringe capacitance becomes more and more significant.



Line Capacitance Calculation



Pizza model



Sandwich model

Ctotal = Ca1 + Ca2 + 2*Cll + 2*Cf + 2*Cs

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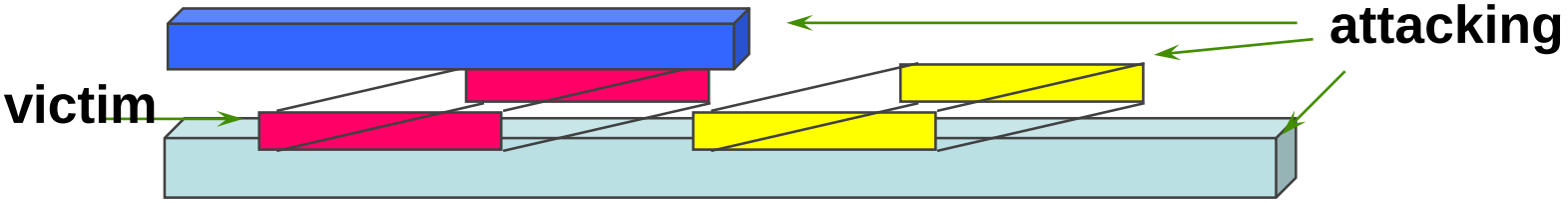
Cross Capacitance



- Cross Capacitance is any capacitance between nets, which are non DC nets.
- In the worst case all the capacitance between nets can be cross capacitance.
- We call the signal that we are analyzing the victim, and all the signals that have cross capacitance to it we will call them attacking signals.

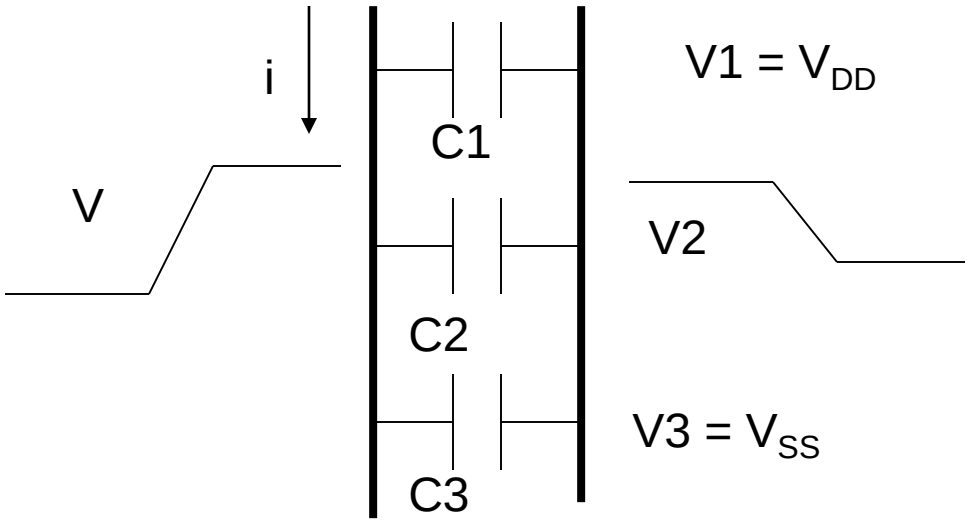
Cross Capacitance & Miller Effect

- **Remembering the current-voltage equation for a capacitor**
  i(t) = C * dv(t)/dt
- **In case that the attacking signal is also switching, then the dv(t)/dt is actually bigger or smaller than the DC case, depending on the switching directions of the victim and attacking signals.**

- **In verification tools we always calculate the voltage referenced to the Ground "Vss" which is a DC signal.**
- **We can see this effect as if the effective capacitance between the line and the Ground changes, this is called the Miller Effect.**

- **Miller Coefficient is the factor that we use to multiply the Xcap in order to model the Miller Effect.**

Miller Coupling Mathematics



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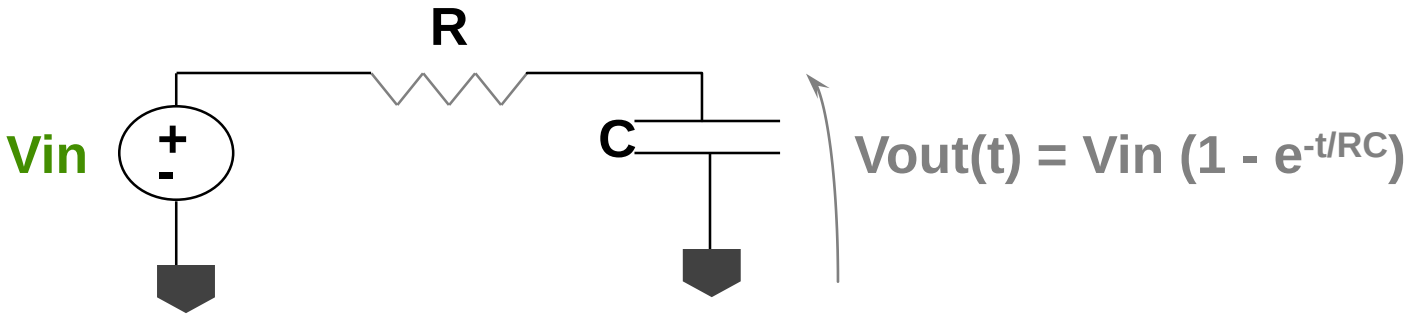
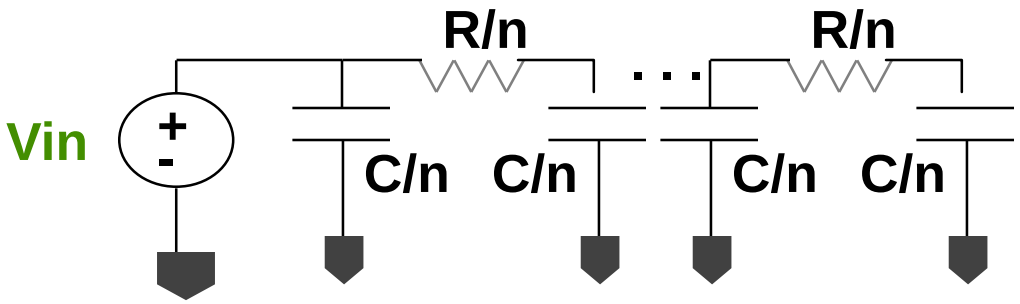
Lumped Line Model

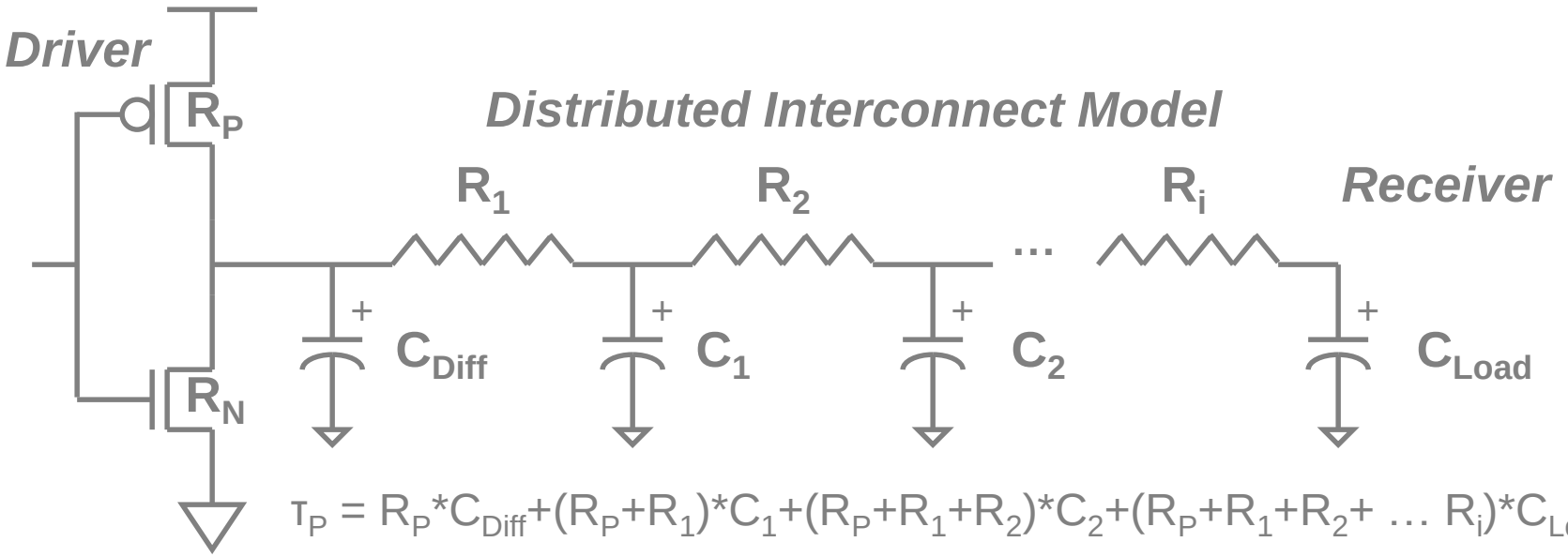


- A lumped model is a pessimistic one, which assumes that all the capacitance, line and load, is located at the end of the line, in other words that the driver “sees” the total load through the total line resistance.
- As the RC delay increases the lumped RC model is less and less accurate.

Distributed Line Model



- The distributed line model is a more accurate model which assumes that the line is built out of many segments, when each segment is modeled as a lumped RC model.
- For calculating the RC delay using the distributed model a simulation is needed

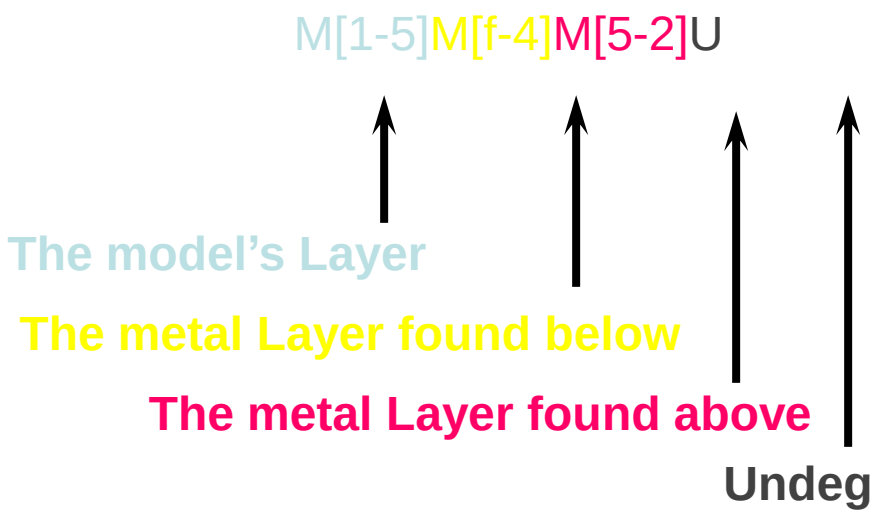


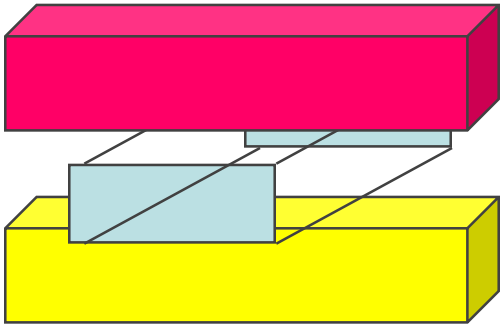
$$\tau_P = R_P*C_{Diff}+(R_P+R_1)*C_1+(R_P+R_1+R_2)*C_2+(R_P+R_1+R_2+ \ldots R_i)*C_{Load}$$

$$\tau_N = R_N*C_{Diff}+(R_N+R_1)*C_1+(R_N+R_1+R_2)*C_2+(R_N+R_1+R_2+ \ldots R_i)*C_{Load}$$

Line Capacitance Models

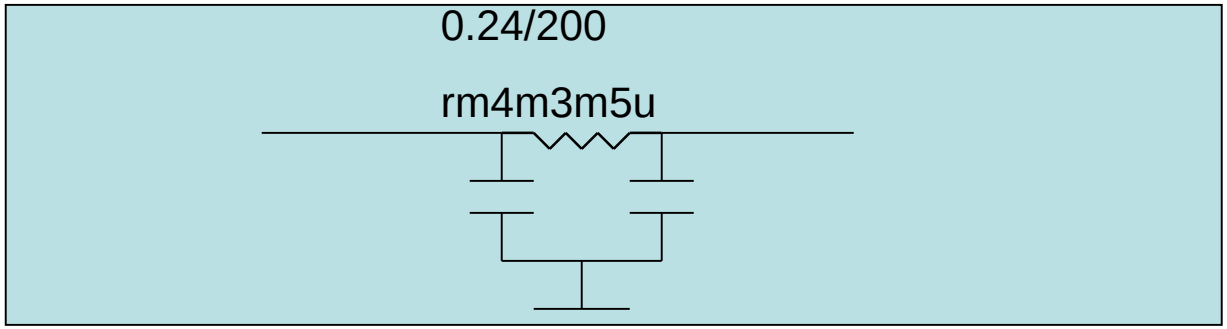
- Unlike the Line resistance, its capacitance is dependent not only on the line topography, but also on its neighbors from all directions.
- In order to model the Line capacitance we define the parameters for all the possible configurations, and then map each line segment to one of these configurations.
- The naming convention of the models is:





FTRC Elements

- The FTRC element is a library cell which enables the user to build a line simulation model using the lumped approximation for the distributed line.
- The FTRC element has the following parameters
  - MODEL: define the segment's capacitance and resistance model the model should be one of the process file defined models (m2m1m3u, m1fm4, ...)
  - wid: The segment width
  - Spc: The segment spacing
  - Length: The length of the segment



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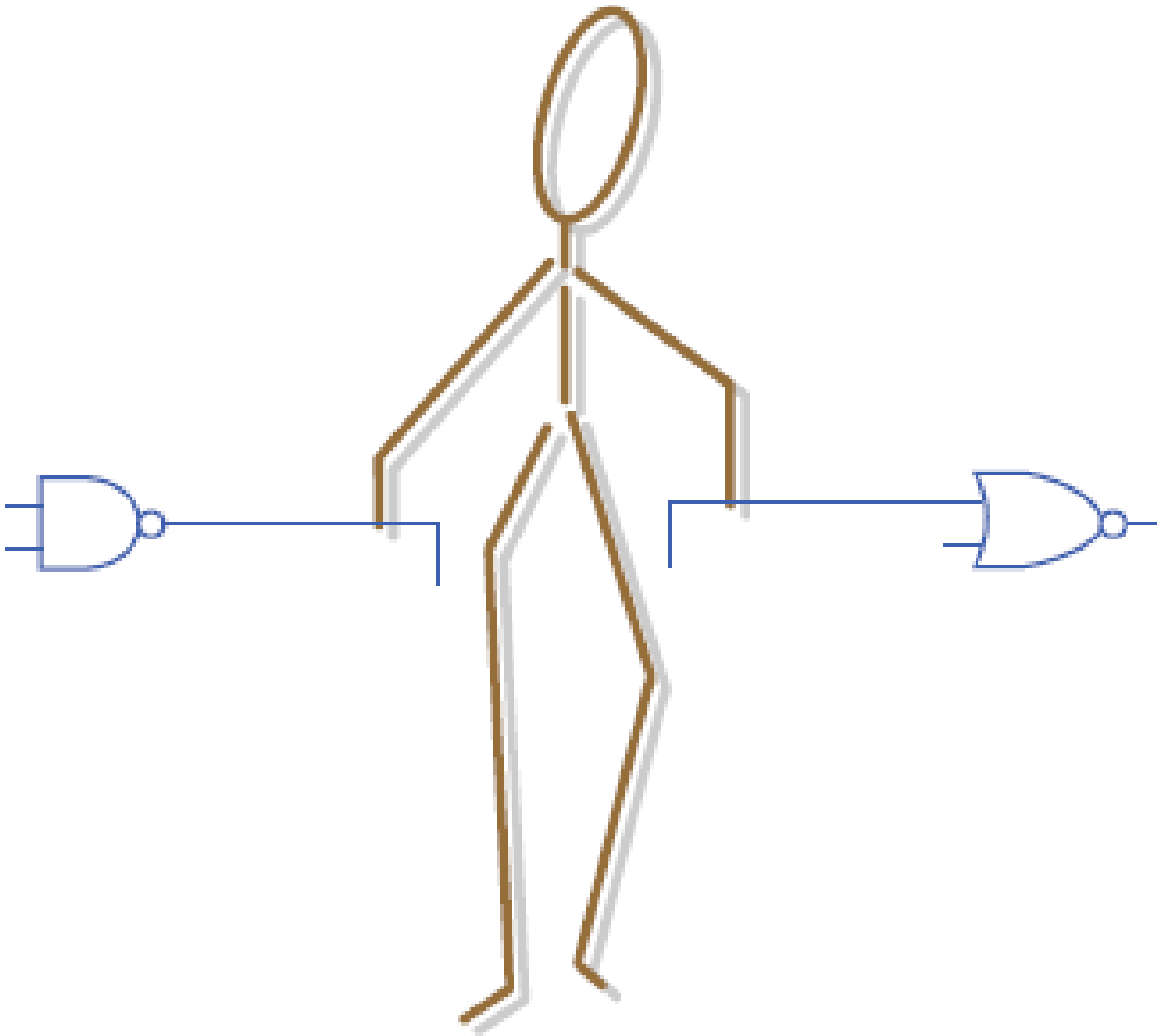
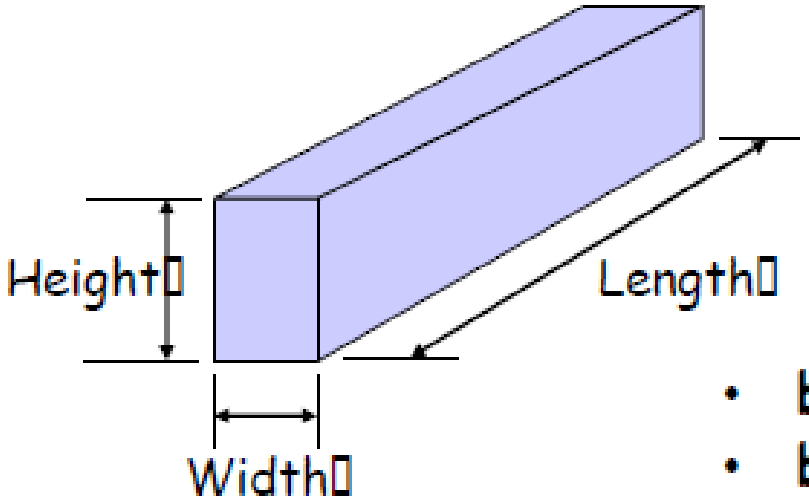
Wires



Interconnect Problems

- A lot of circuit designers are very worried about what's happening with wires in CMOS technology
- Device technology has been scaling well, with gate performance increasing linearly with decreasing feature size
- Wires scale differently, and long wires have been getting relatively slower over time
- delay is a function of wire resistance and capacitance

Wire Resistance



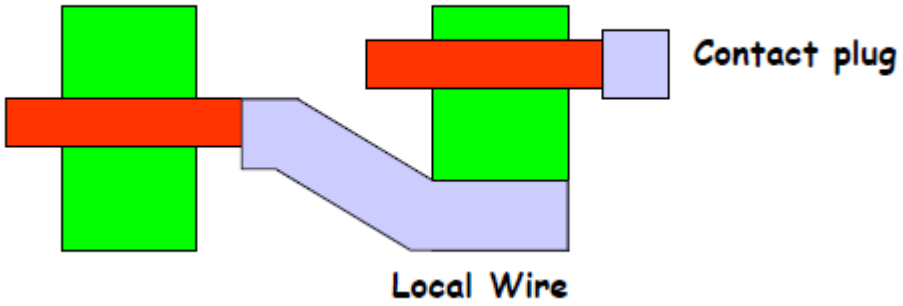
$$\text{resistance} = \frac{(\text{length} \times \text{resistivity})}{(\text{height} \times \text{width})}$$

- bulk aluminum 2.8×10^{-8} Ω-m
- bulk copper 1.7×10^{-8} Ω-m
- bulk silver 1.6×10^{-8} Ω-m

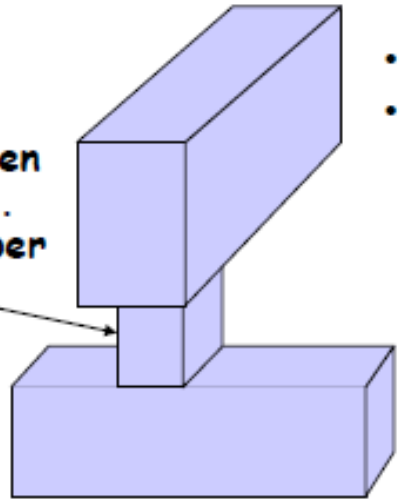
- Height (Thickness) fixed in given manufacturing process
- Resistances quoted as Ω/square
- TSMC 0.18μm 6 Aluminum metal layers
  - M1-5 0.08 Ω/square (0.5 μm x 1mm wire = 160 Ω)
  - M6 0.03 Ω/square (0.5 μm x 1mm wire = 60 Ω)

Local Interconnect

- Use contact material (tungsten) to provide extra layer of connectivity below metal 1
- Can also play same trick with silicided poly to connect gates to diffusion directly in RAMs
- Typically used to shrink memory cells or standard cells
- Contacts directly to poly gate or diffusion



Via Resistance



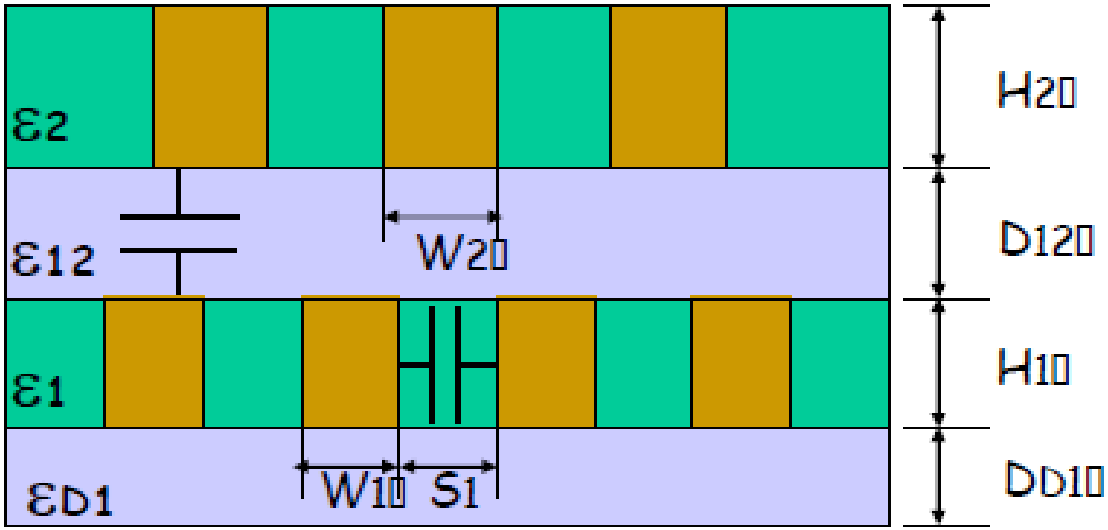
Vias made from Tungsten in Aluminum processes. Vias are Copper in Copper processes

- Via resistance significant
- TSMC 0.18μm 6-Al

Diff-M1	11.0 Ω
Poly-M1	10.4 Ω
M2-M1	4.5 Ω
M3-M1	9.5 Ω
M4-M1	15.0 Ω
M5-M1	19.6 Ω
M6-M1	21.8 Ω

- Resistance of two via stacks at each end of M1 wire equivalent to about 0.1 mm wire (~20 Ω)
- Resistance of two via stacks at each end of M6 wire about the same as 1 mm narrow M6 wire (~60 Ω)!!!
- Use multiple vias in parallel to reduce effective contact resistance
- Copper processes have lower via resistance

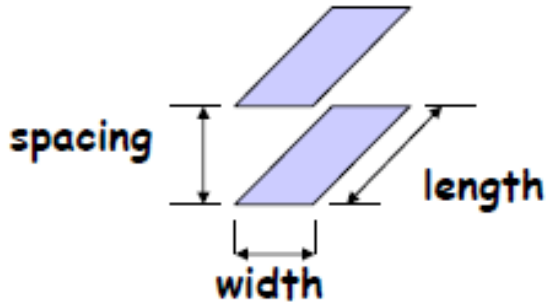
Wire Capacitance



- Capacitance depends on geometry of surrounding wires and relative permittivity, ε_r, of insulating dielectric
  - silicon dioxide, SiO_2 $\varepsilon_r = 3.9$
  - silicon flouride, SiOF $\varepsilon_r = 3.1$
  - SiLK™ polymer, $\varepsilon_r = 2.6$
- Can have different materials between wires and between layers, and also different materials on higher layers

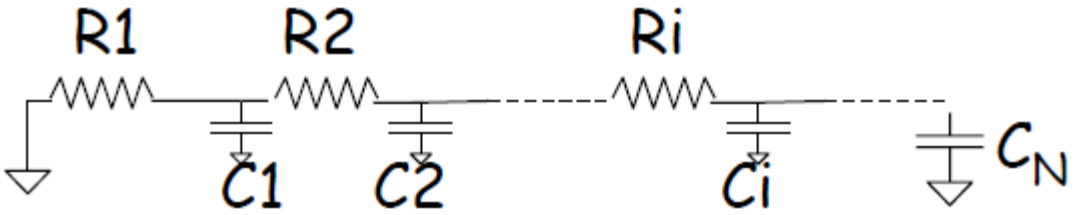
Capacitance Scaling

$$\text{parallel plate capacitance} \propto \frac{\text{width}}{\text{spacing}} \times \text{length}$$



- Capacitance/unit length ~constant with feature size scaling (width and spacing scale together)
  - Isolated wire sees approx. 100 fF/mm
  - With close neighbors about 160 fF/mm
- Need to use capacitance extractor to get accurate values

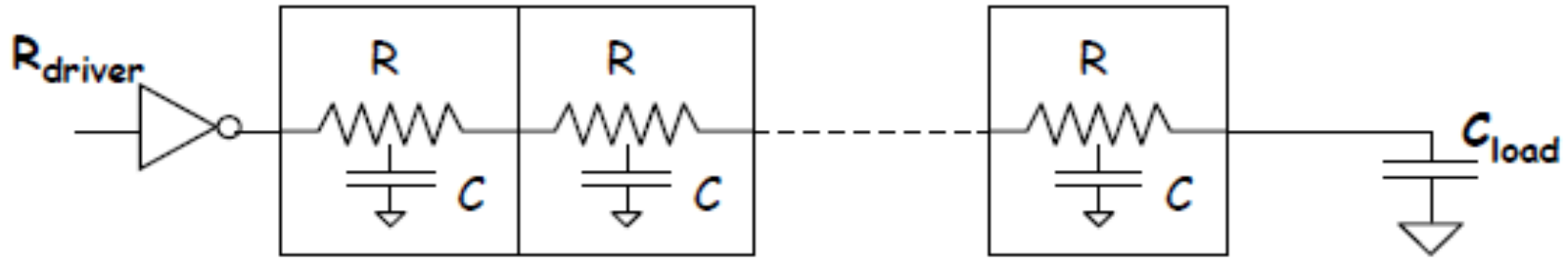
RC Delay Estimates



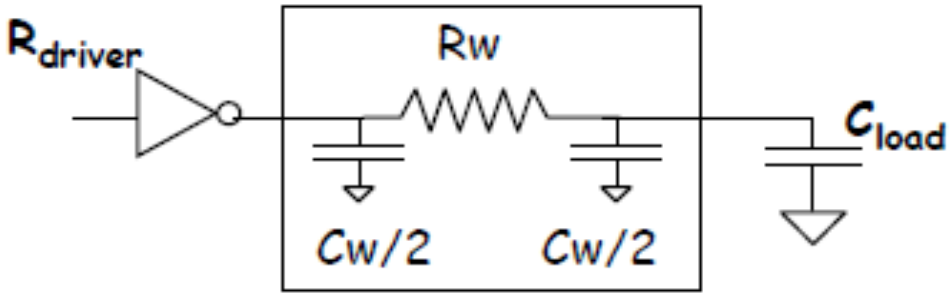
Penfield-Rubenstein model estimates:

$$\text{Delay} = \sum_{i}\left(\sum_{j=1}^{j=i} R_j\right) C_i$$

RC Delay Estimates



- Wire has distributed R and C per unit length
  - wire delay increases quadratically with length
  - edge rate also degrades quadratically with length
- Simple lumped Π model gives reasonable approximation
  - Rw is lumped resistance of wire
  - Cw is lumped capacitance (put half at each end)



$$\text{Delay} = \text{Rdriver} \times \frac{\text{Cw}}{2} + (\text{Rdriver} + \text{Rw}) \times \left(\frac{\text{Cw}}{2} + \text{Cload} \right)$$

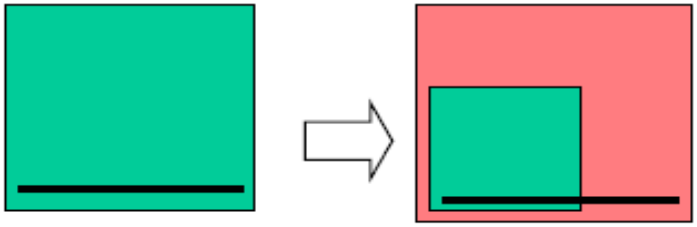
Wire Delay Example

- In 0.18μm TSMC, 5x minimum inverter with effective resistance of 3 kΩ, driving FO4 load (25fF)
- Delay = Rdriver x Cload = 75 ps

- Now add 1mm M1 wire, 0.25μm wide
  - Rw = 320Ω wire + 22Ω vias = 344Ω
  - Cw = 160fF

$$\begin{aligned} \text{Delay} &= \text{Rdriver} \times \frac{Cw}{2} + (\text{Rdriver} + \text{Rw}) \times \left(\frac{Cw}{2} + \text{Cload} \right) \\ &= 3\text{k}\Omega \times 80\text{fF} + (3\text{k}\Omega + 344\Omega) \times (80\text{fF} + 25\text{fF}) \\ &= 591\text{ps} \end{aligned}$$

Wire Delay Scaling, Global Wires

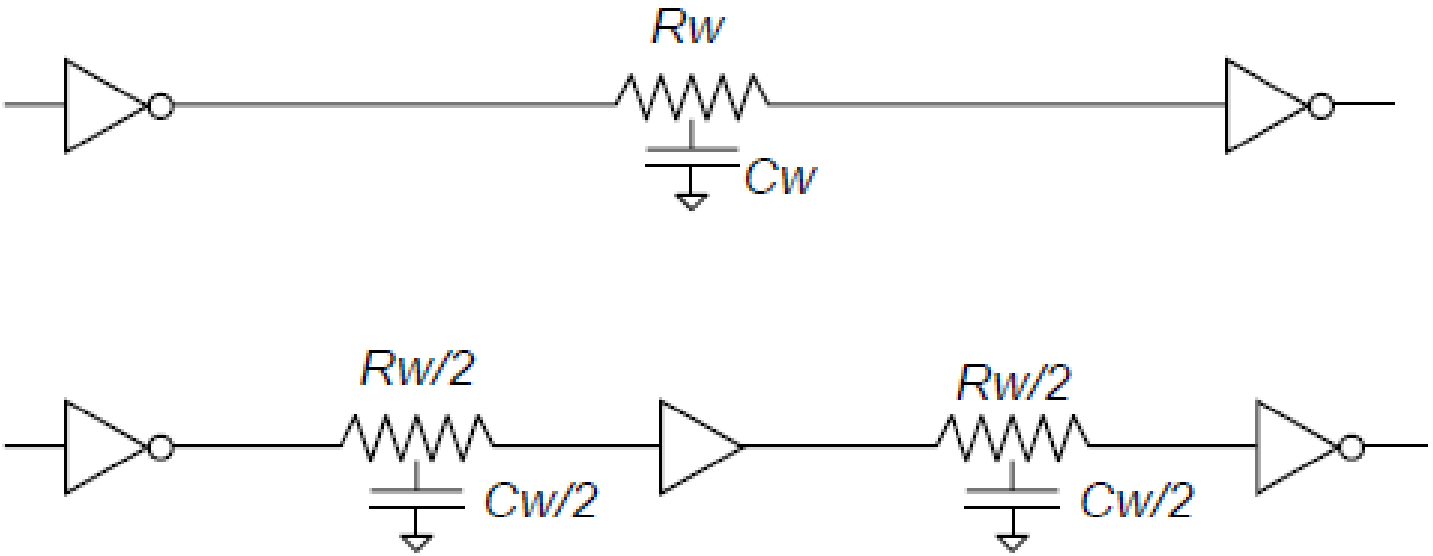


- For wire crossing whole chip
  - Resistance grows linearly
  - Capacitance stays fixed
- Wire delay increases relative to gate delay

Process Technology Fixes

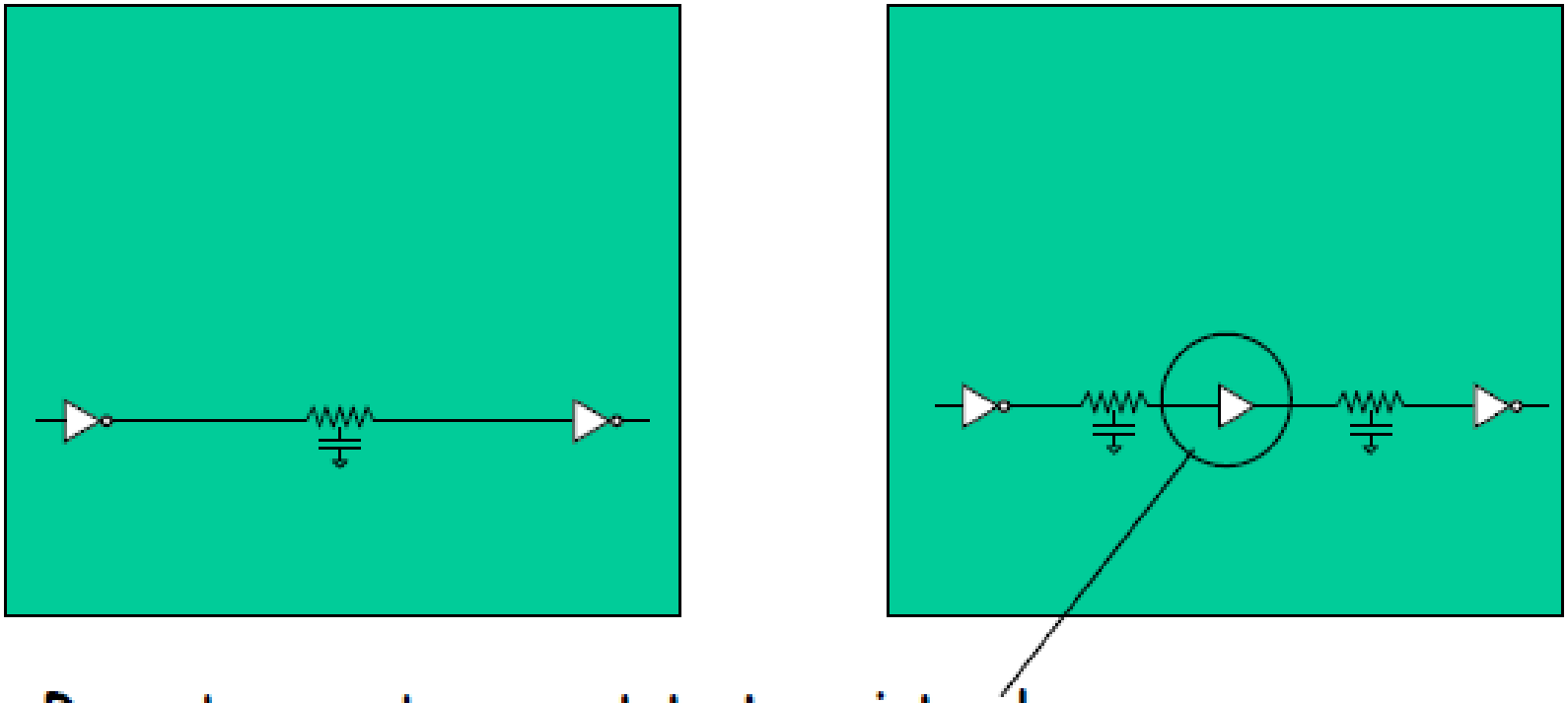
- Reduce R
  - use copper instead of aluminum, 40% reduction
  - provide upper layers with thicker metal for long range wires
  - provide more layers to improve density, makes wires shorter
- Reduce *C*
  - use low-k dielectric, >2x reduction possible
  - increase inter-layer spacing (limited effect, problems with via formation)
  - provide more layers to improve density, makes wires shorter

Circuit Fixes - Repeaters



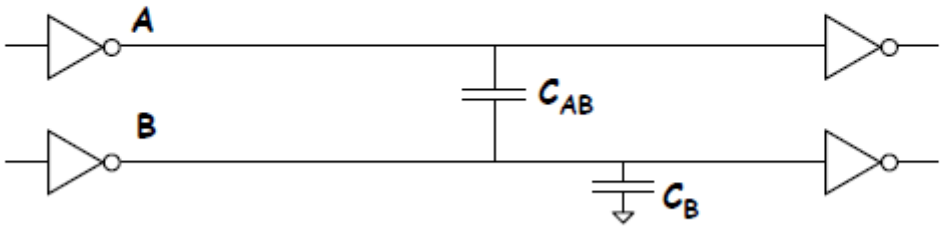
- Use repeaters
- Converts quadratic dependence into linear dependence on length (but watch the constants)
- Can determine optimal repeater sizing for minimum delay

Repeater Issues



- Repeater must connect to transistor layers
- Blocks other routes with vias that connect down
- Requires space on active layers for buffer transistors and power connections
- Repeaters often grouped in preallocated repeater boxes spread around chip
  - repeater location might not give ideal spacing

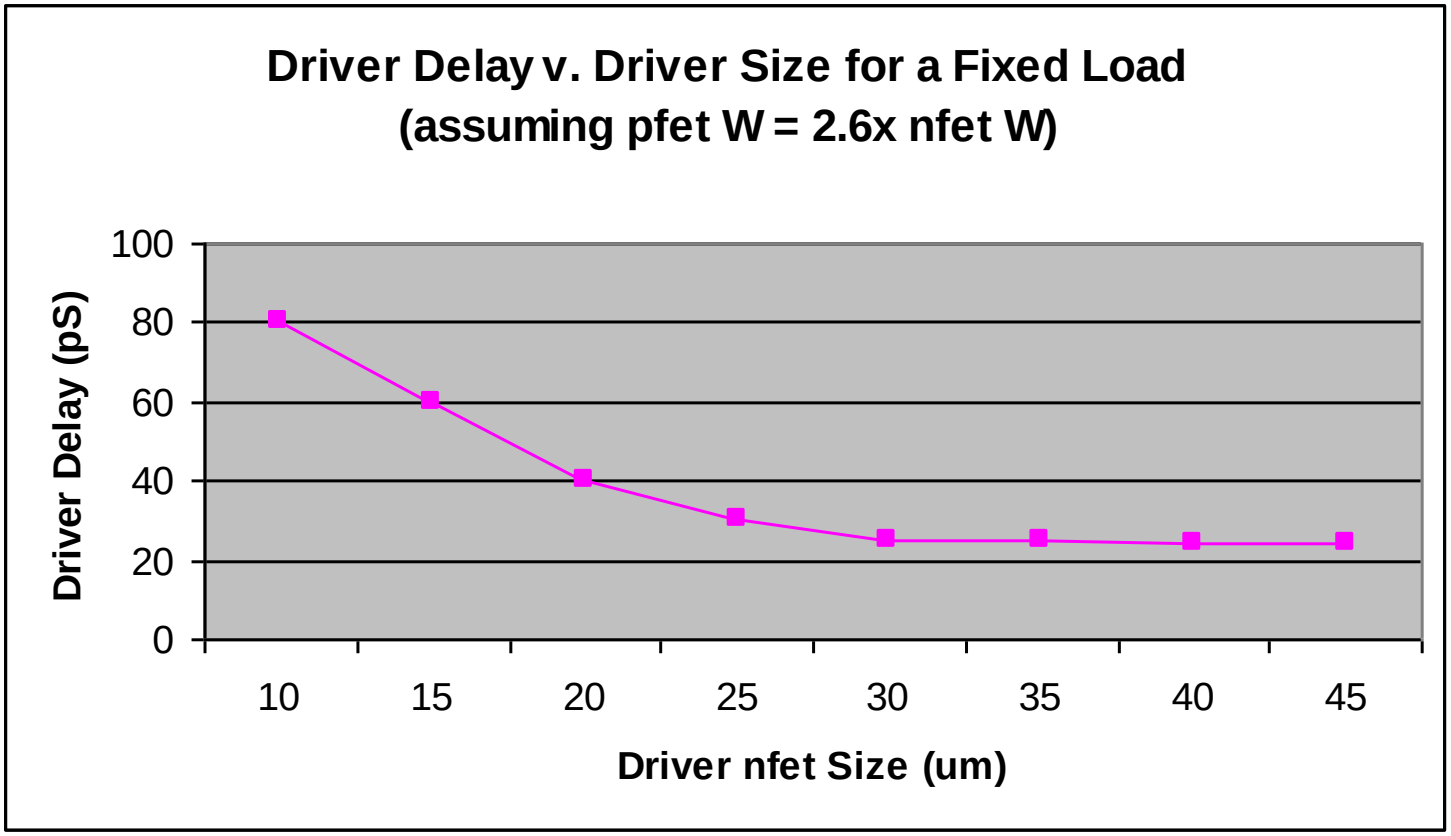
Fixing Coupling Problems



- Avoid placing simultaneously switching signals next to each other for long parallel runs
- Reroute signals which will be quiet during switching inbetween simultaneous switching signals
- Route signals close to power rails to provide capacitance ballast
- Tough problem to solve – moving one wire can introduce new problems
  - "timing closure" causes many real-world schedule slips

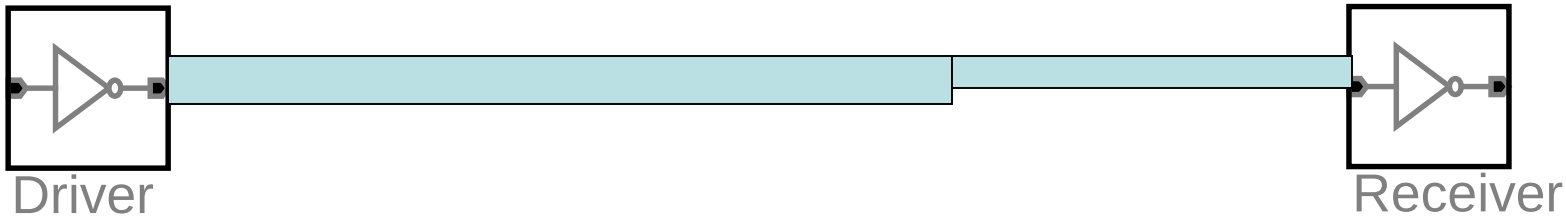
Repeaters

- Use repeaters to break lengthy high-metal routes into segments
- It also assists in preventing your routes from running into slope and noise issues
- Bigger repeaters don’t always translate into faster paths; use the right sized device for the job
- Don’t try to squeeze too much out of the interconnect/repeater design solution by over-sizing repeaters just to gain a few pS… often the path can be solved in the driver or receiver fub at a lower total W cost



- ***Note:*** for this example, improvement in driver delay starts tapering off at nfet W = 25 um; this is the knee of the curve after which ROI for further W increases declines rapidly

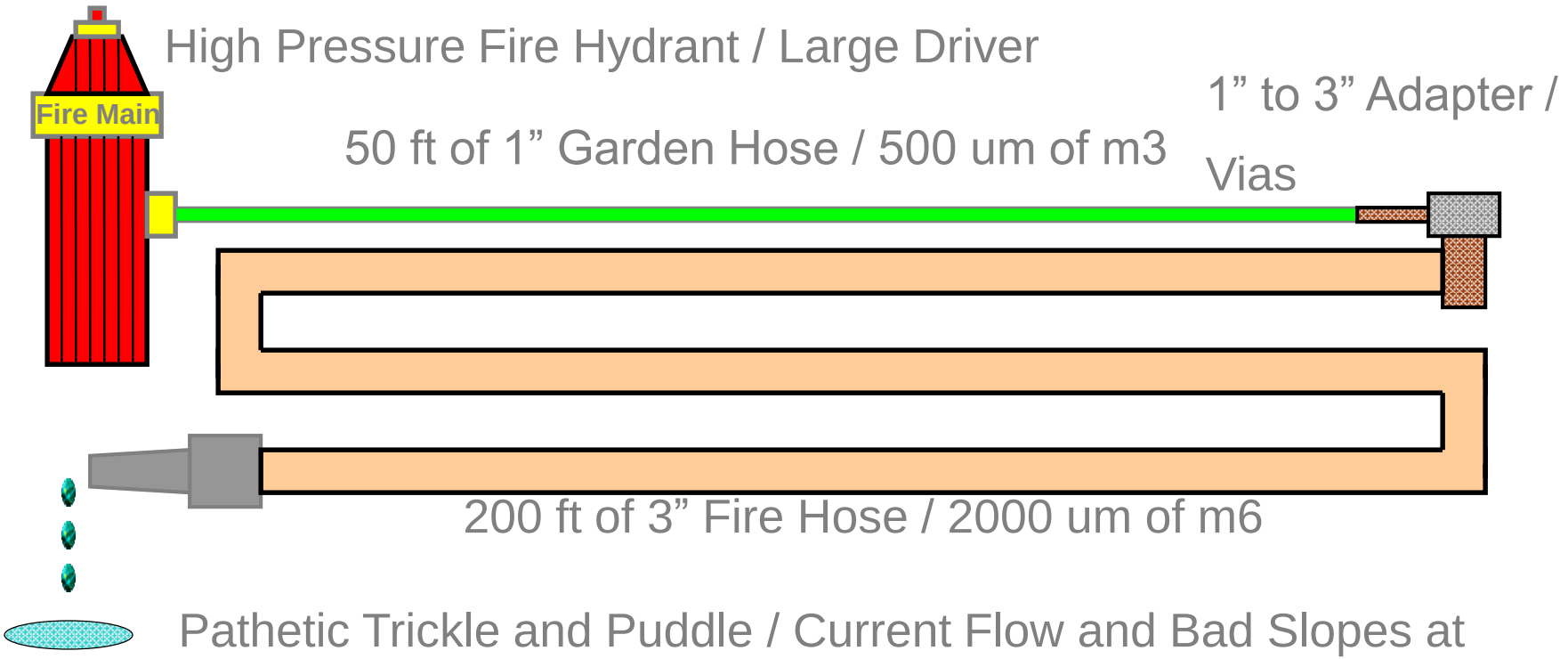
Tapering



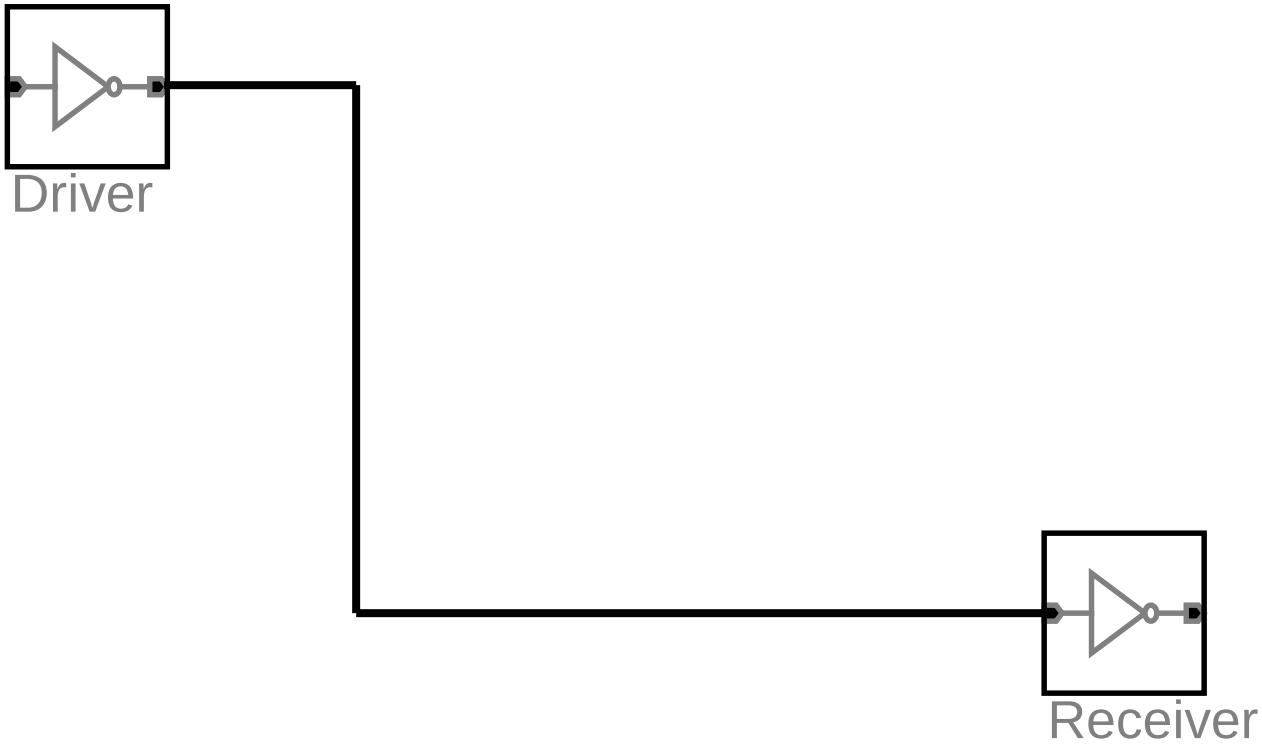
Agenda

- Interconnect Definition
- RC Equation of a Line
- Interconnect Resistivity
- Interconnect Capacitance
- Cross Capacitance & Miller Effect
- Interconnect Modeling
- Repeaters
- Interconnect DO’s and DON’Ts

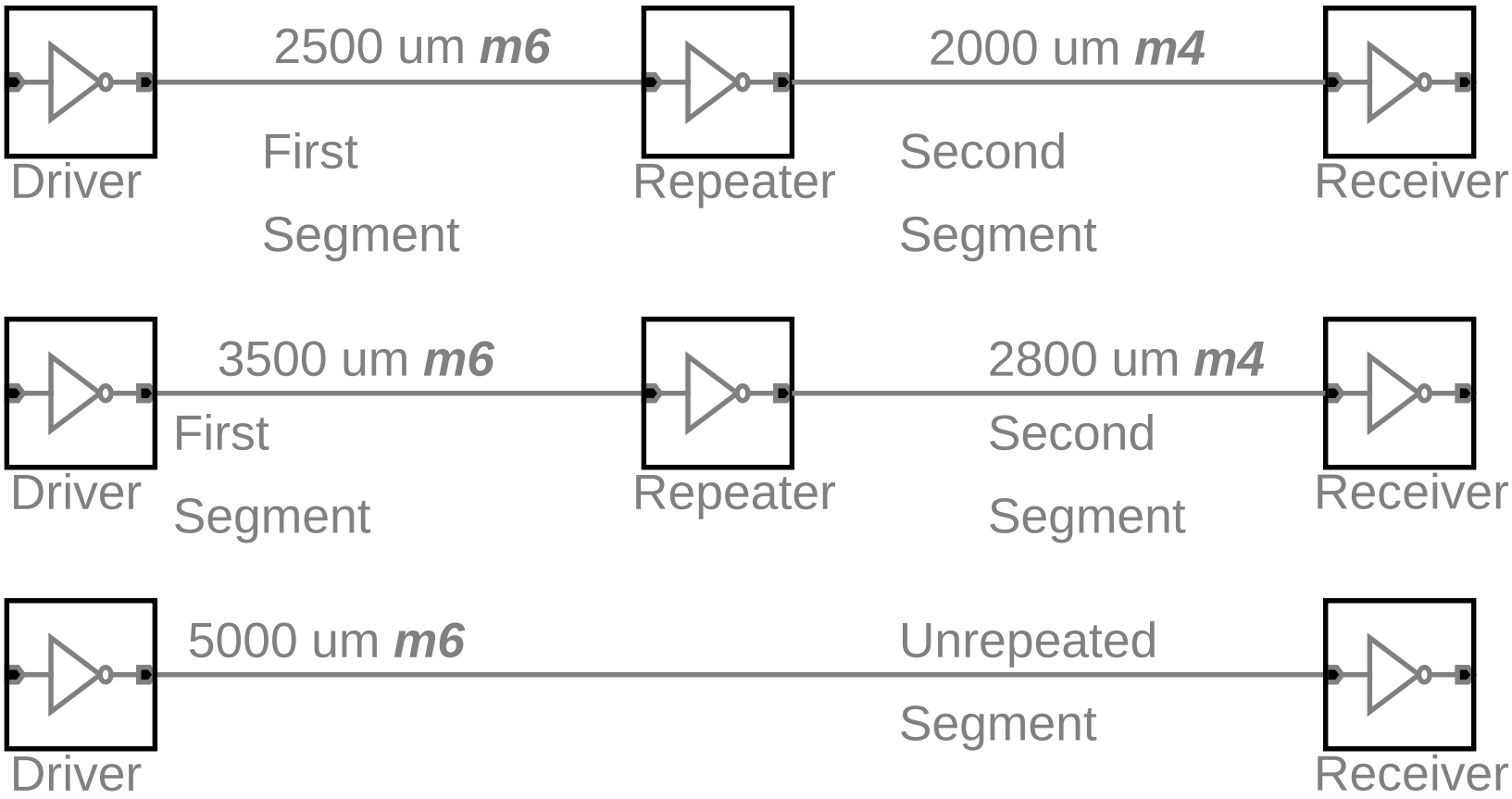
Do Not Do : Example



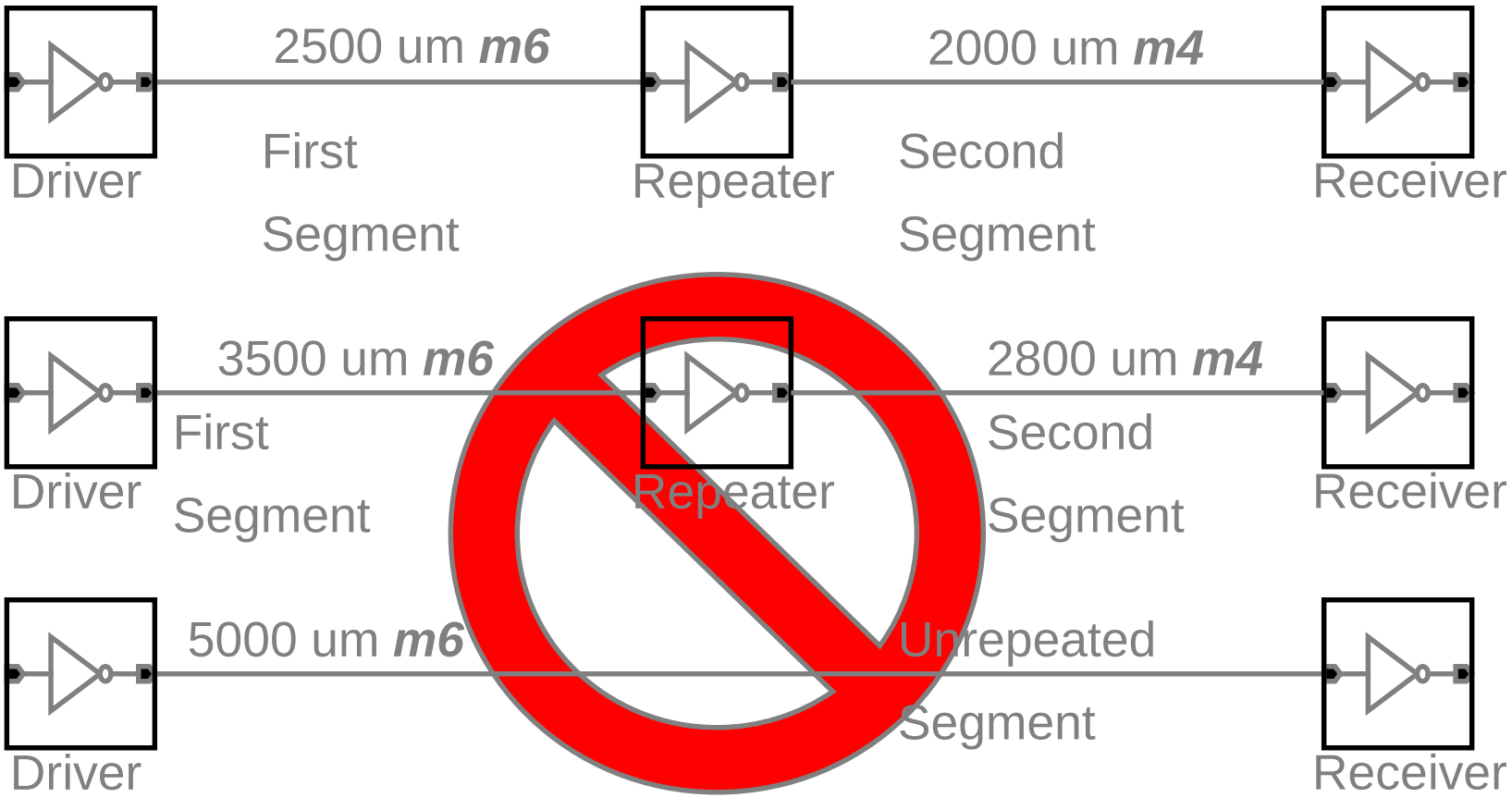
- Lengthy high metal routes initiating in lengthy m3 routes (> a few hundred microns) fall victim to a large amount of R-shielding of the downstream C. This typically leads to undersized drivers, and even if the drivers are intentionally oversized, the driver is choked off by the lengthy and highly resistive m3.


Driver
Receiver

Device Rule 1: Example



Device Rule 1: Example



- **Reduce Robustness**
- **Affect Performance**

Classes of Parasitics

- **Capacitive**
- **Resistive**
- **Inductive**

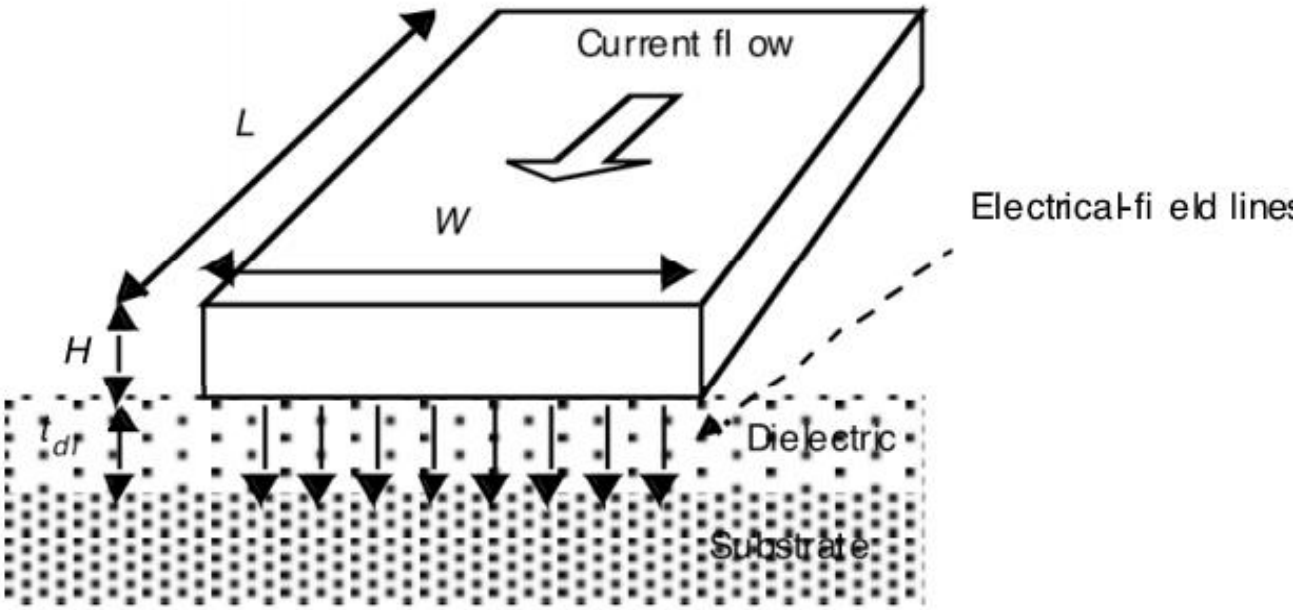
Methods For Improving RC Delay

- Optimizing the Routing Path Length
- Tapering & Optimizing the Width Across the Net
- Reducing The Line Cap (Spacing, ...)
- Optimizing the Driver Size
- Reducing The Receivers Load
- Adding Repeaters

Impact of Interconnect Parasitics

- Interconnect and its parasitics can affect all of the metrics we care about
  - Cost, reliability, performance, power consumption
- Parasitics associated with interconnect:
  - Capacitance
  - Resistance
  - Inductance

Capacitance: The Parallel Plate Model



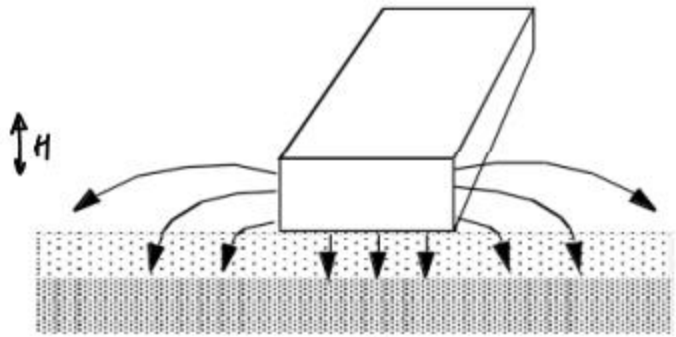
$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

Permittivity

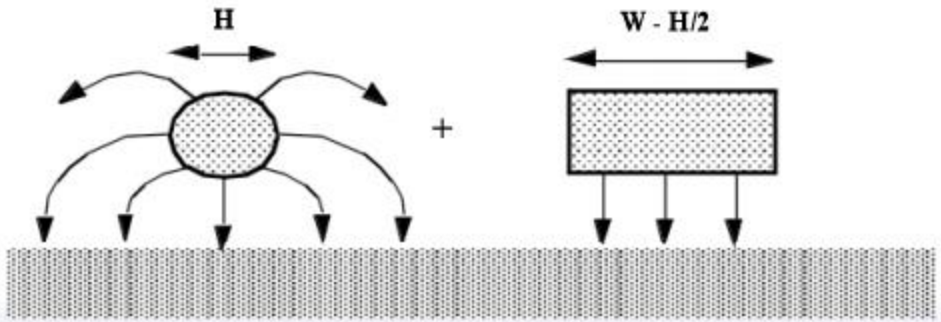
Material	ε_r
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

Fringing Capacitance

$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$



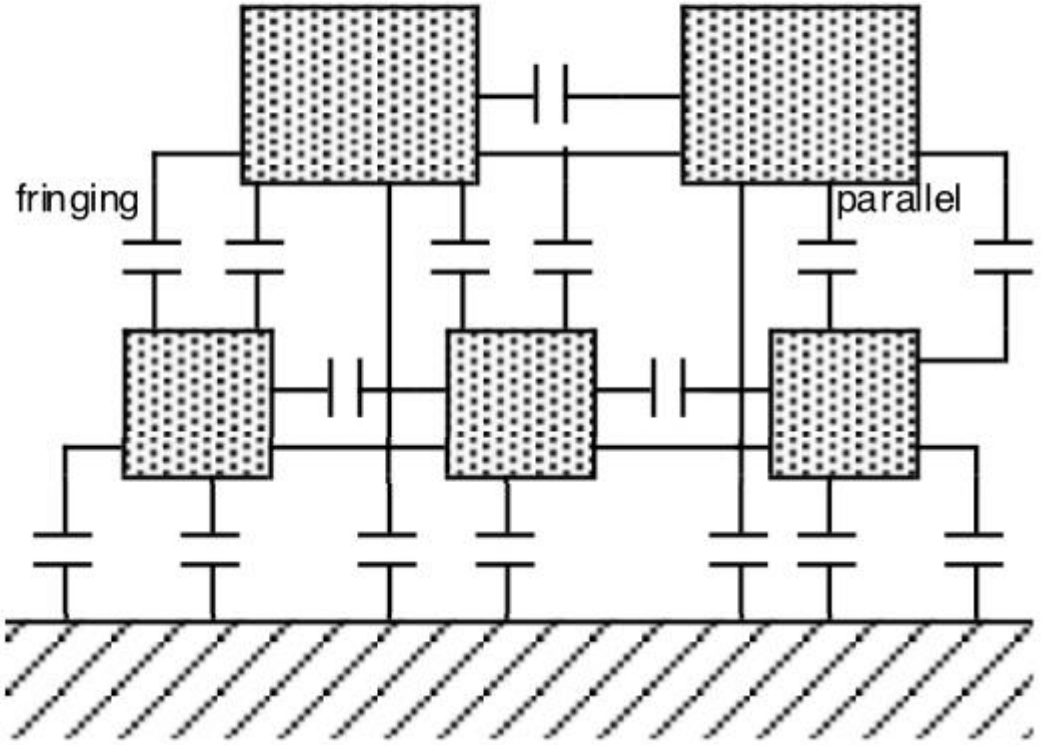
(a)



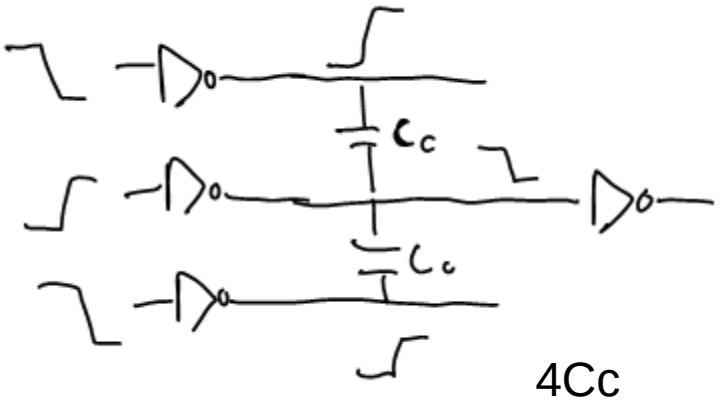
(b)

$$C = C_{pp} \cdot W \cdot L + 2 C_{fringe} L$$

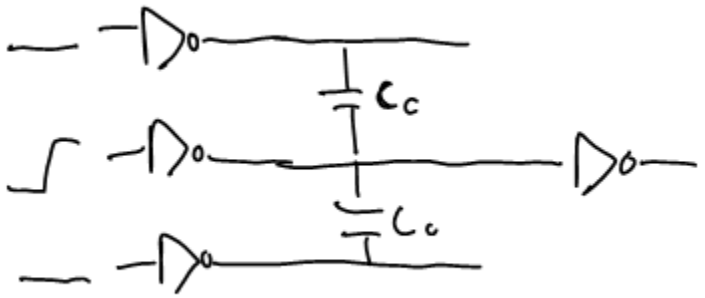
Interwire Capacitance



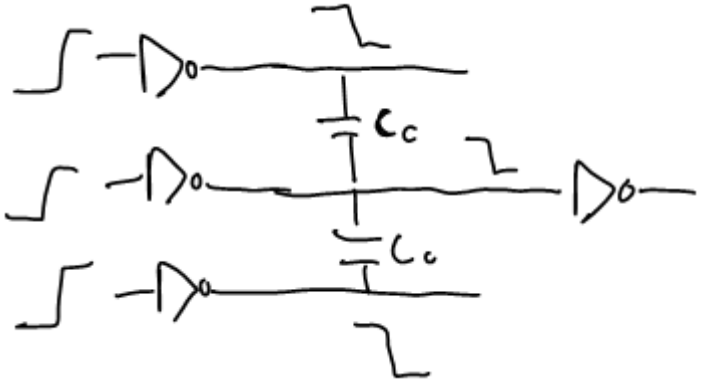
Coupling Capacitance and Delay



4Cc



$C_{c,\,eff} =$ 2Cc

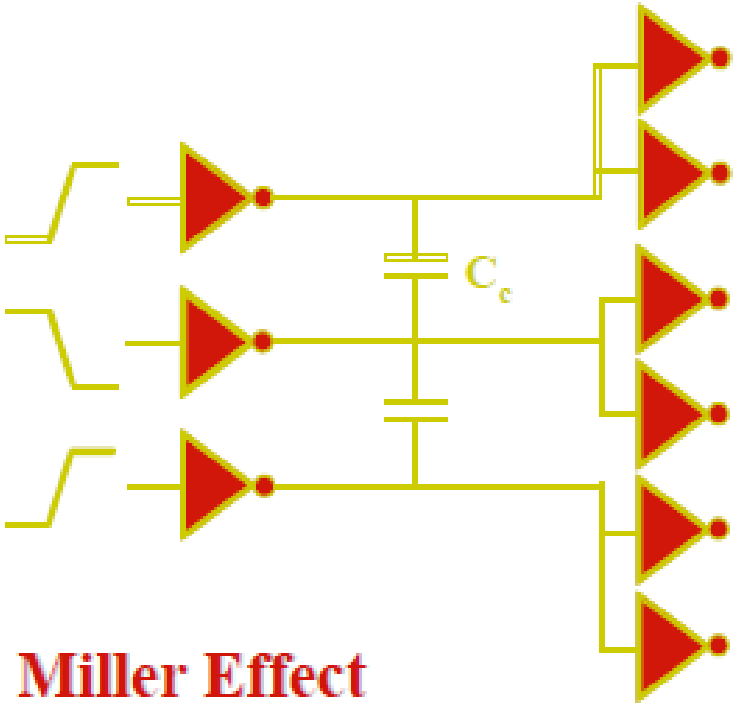


zero

Dealing with Capacitive Cross Talk

- Avoid floating nodes
- Protect sensitive nodes
- Make rise and fall times as large as possible
- Differential signaling
- Do not run wires together for a long distance
- Use shielding wires
- Use shielding layers

Delay Degradation



Miller Effect

- Impact of neighboring signal activity on switching delay

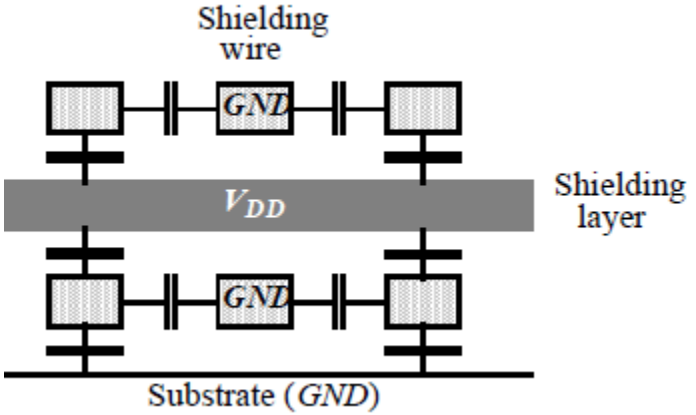
- When neighboring lines switch in opposite direction of victim line, delay increases

- Both terminals of capacitor are switched in opposite directions ($0 \rightarrow V_{dd}$, $V_{dd} \rightarrow 0$)

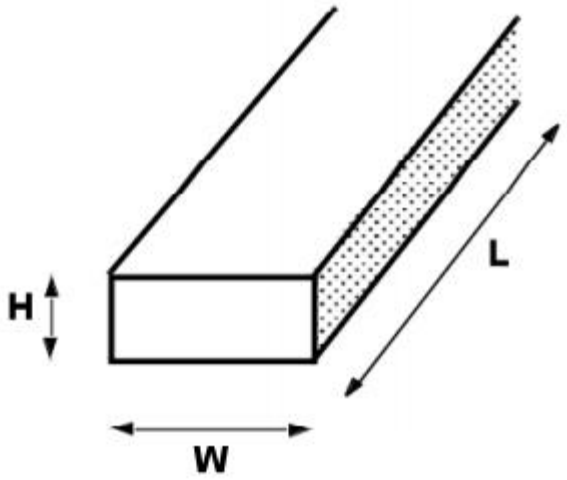
- Effective voltage is doubled and additional charge is needed (from Q=CV)

How to Battle Capacitive Crosstalk

- Avoid large crosstalk cap's
- Avoid floating nodes
- Isolate sensitive nodes
- Control rise/fall times
- Shield!
- Differential signaling



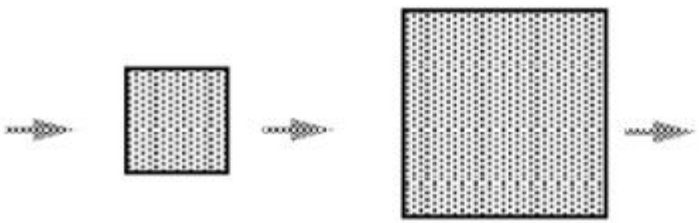
Wire Resistance



$$R = \rho \frac{L}{H W}$$

Sheet Resistance
R_o

$R_1 \equiv R_2$



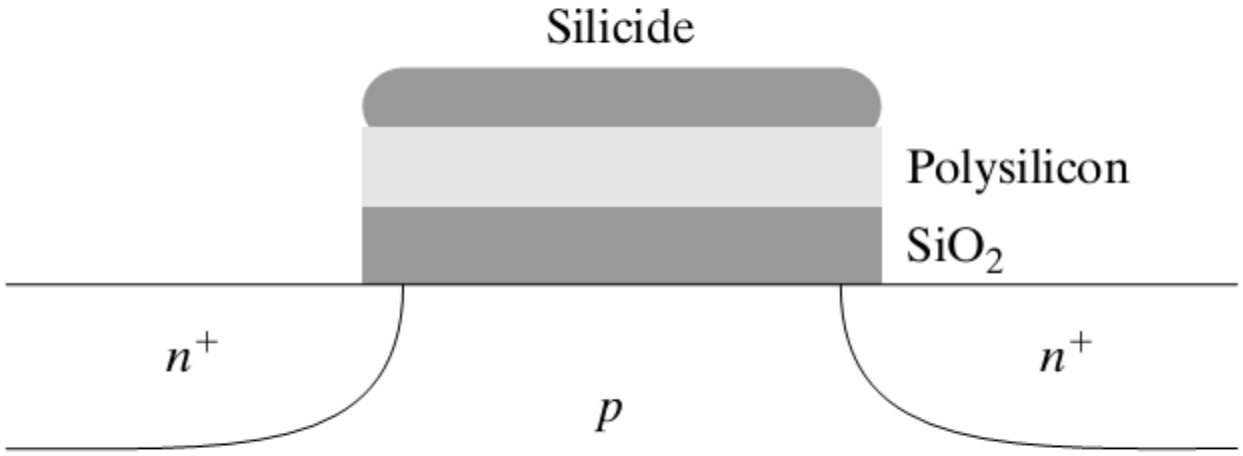
Interconnect Resistance

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Dealing with Resistance

- **Use Better Interconnect Materials**
  - e.g. copper, silicides
- **More Interconnect Layers**
  - reduce average wire-length
- **Selective Technology Scaling**

Polycide Gate MOSFET



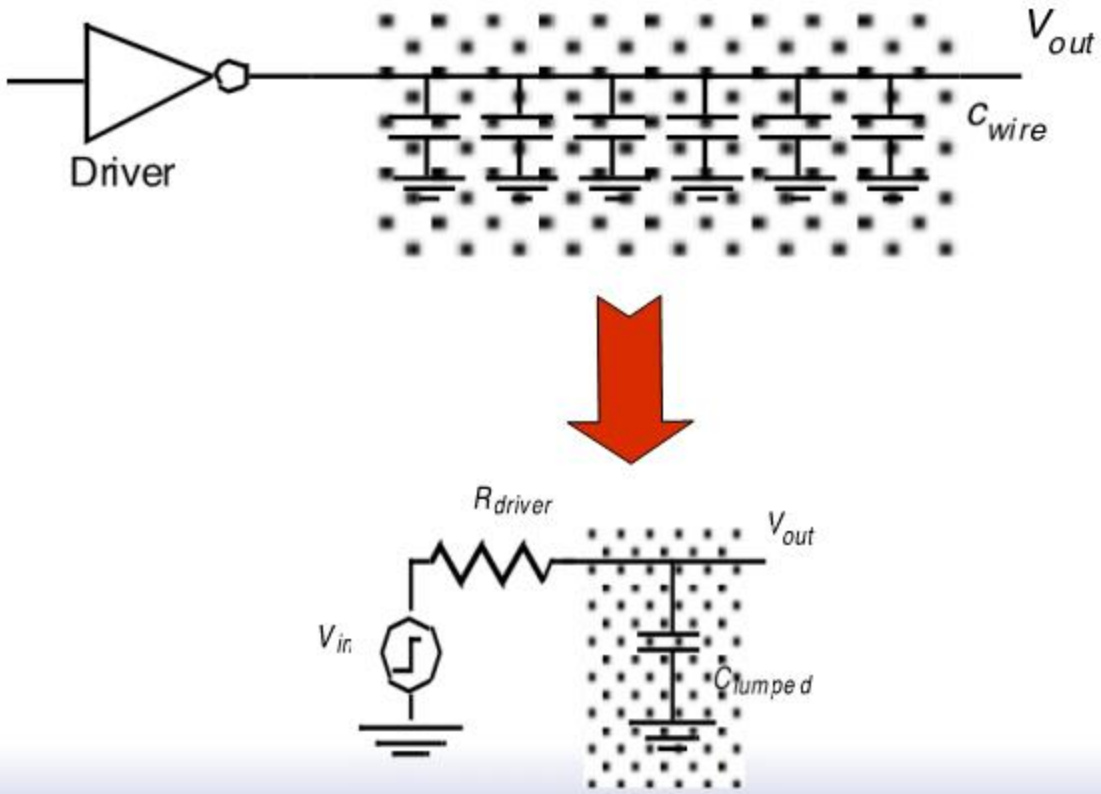
Silicides: WSi_2, $TiSi_2$, $PtSi_2$ and TaSi

Conductivity: 8-10 times better than Poly

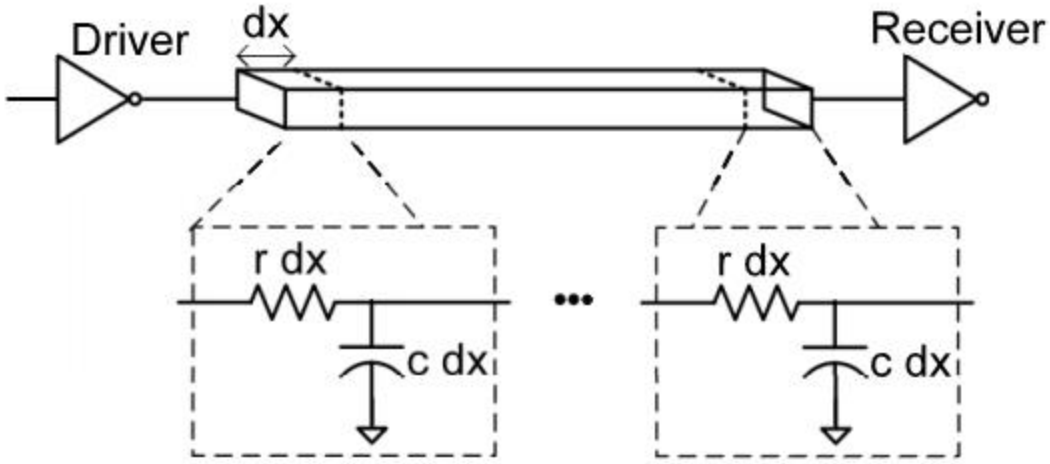
Sheet Resistance

Material	Sheet Resistance (Ω/❑)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

The Lumped Model

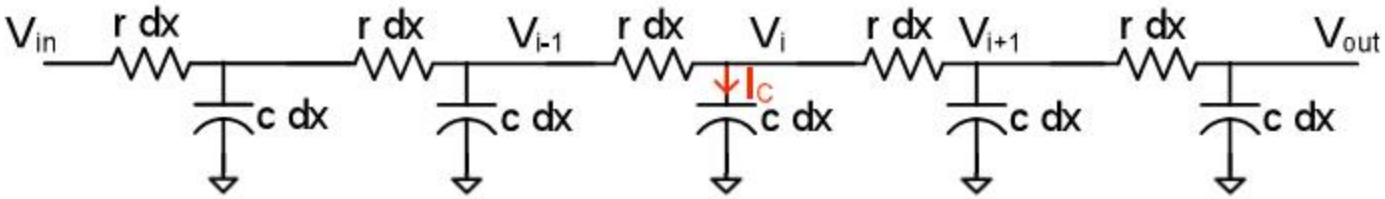


The Distributed RC-line



- Analysis method:
  - Break the wire up into segments of length dx
  - Each segment has resistance (r dx) and capacitance (c dx)

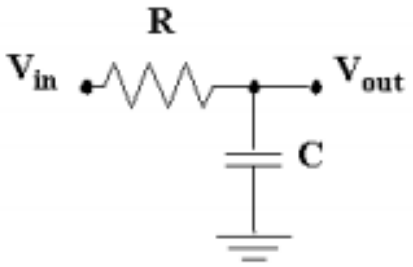
The Distributed RC-line



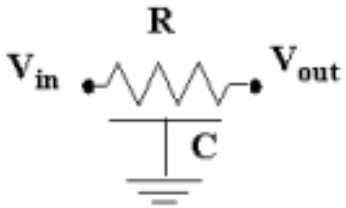
$$I_C = c\Delta L\frac{\partial V}{\partial t} = \frac{(V_{i-1} - V_i) - (V_i - V_{i+1})}{r\Delta L} \longrightarrow \boxed{rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}}$$

$$\boxed{\tau = \frac{L^2}{2}rc}$$

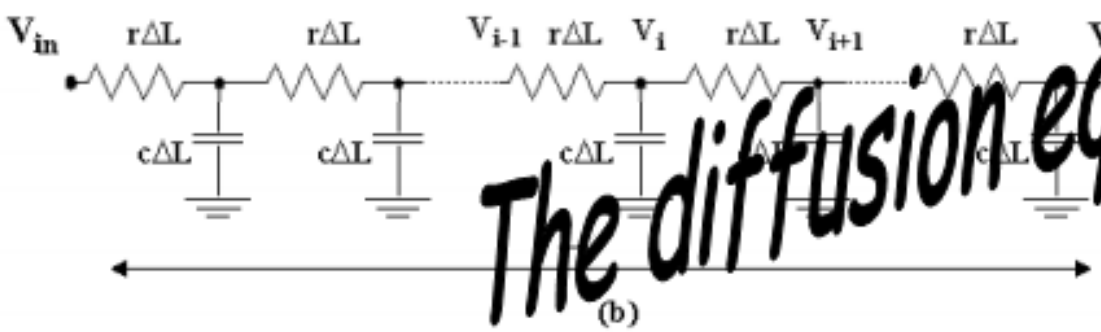
The Distributed RC Line



(a)



(c)



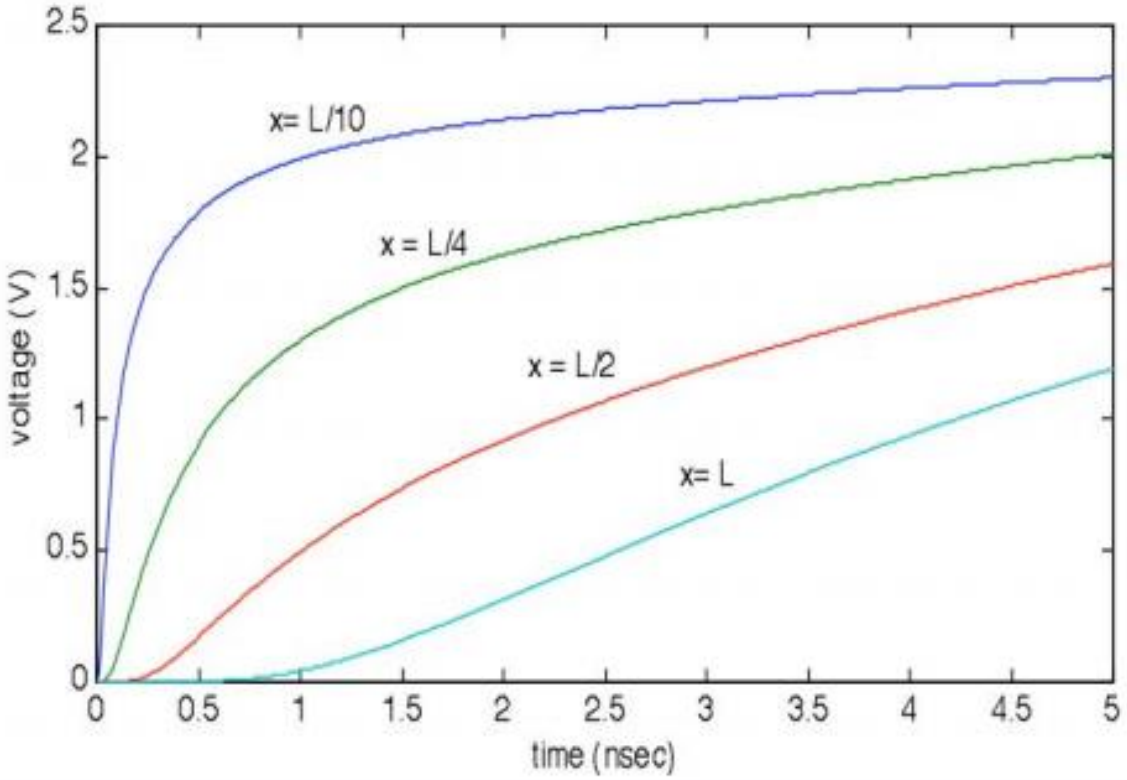
(b)

The diffusion equation

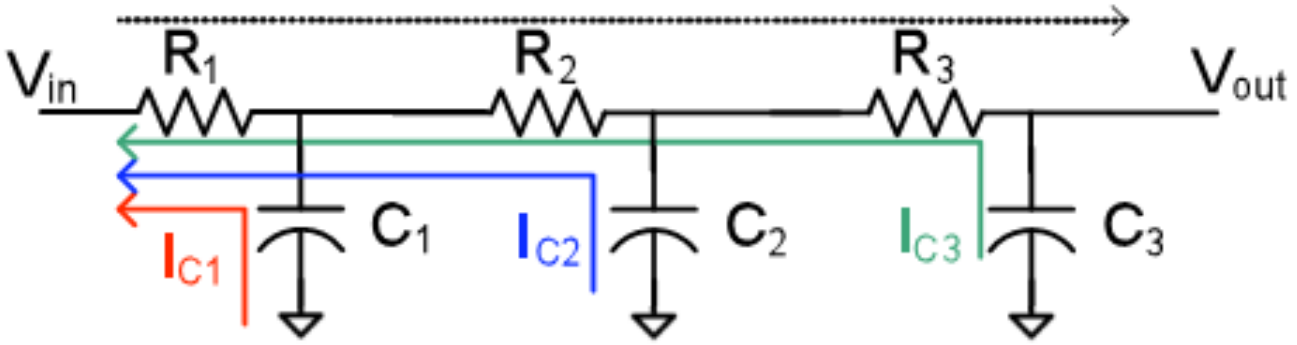
$$rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}$$

$$\tau(V_{out}) = \frac{rc\ L^2}{2}$$

Step-response of RC wire as a function of time and space

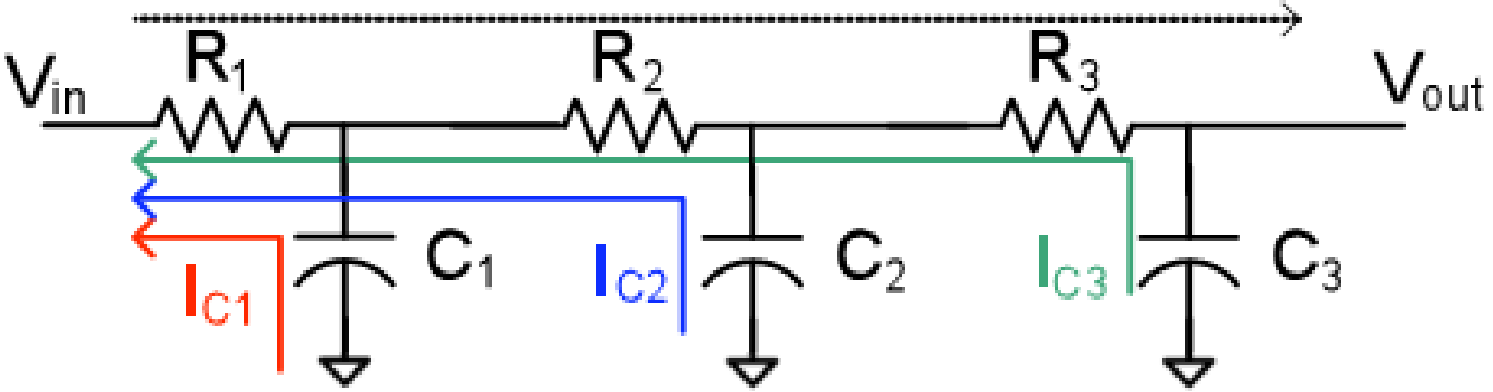


Simplified Model: Elmore Delay



- "Elmore delay": approximation for delay of arbitrary (complex) RC circuits
- To find "Elmore time constant":
  - For each capacitor, draw path of current from cap to input
  - Multiply C by sum of R's on current path that are common with path from V_{in} to V_{out}
  - Add up RC products from all capacitors

Simplified Model: Elmore Delay



$$\tau_{Elmore} = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3$$

Wire Model

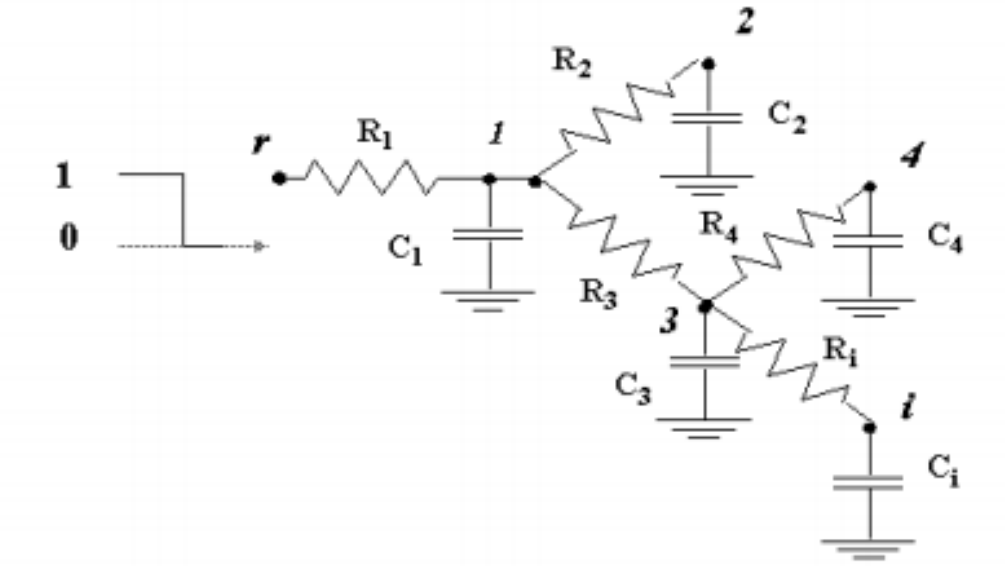
Model the wire with N equal-length segments:

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \ldots + Nrc) = (rcL^2)\frac{N(N+1)}{2N^2} = RC\frac{N+1}{2N}$$

For large values of N:

$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

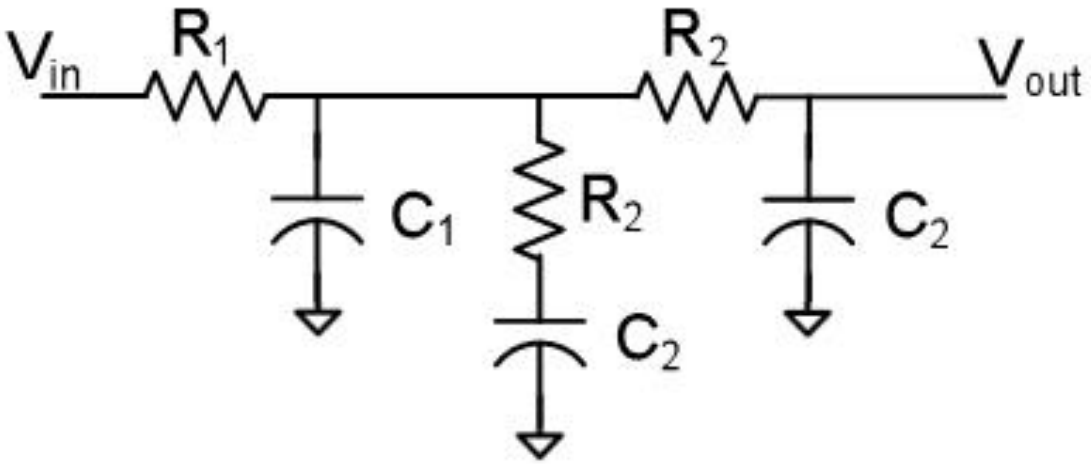
Elmore Delay - Extended



$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \to i) \cap path(s \to k)])$$

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

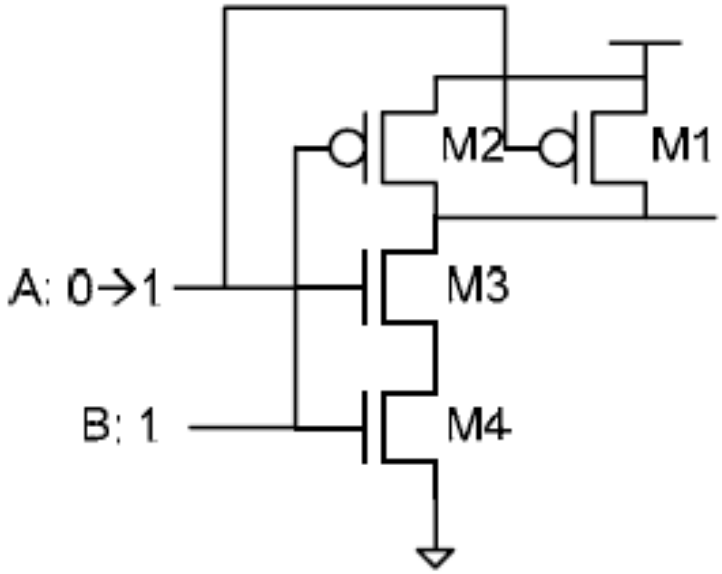
Another Elmore Delay Example

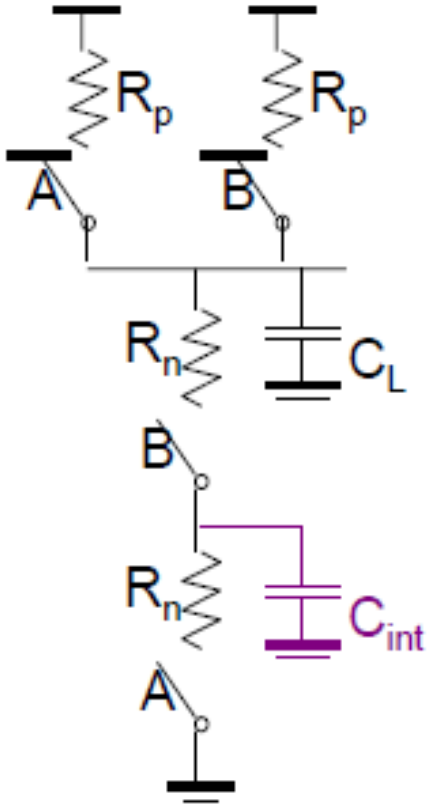


$$\tau_{Elmore} =$$

Complex Gate Delay

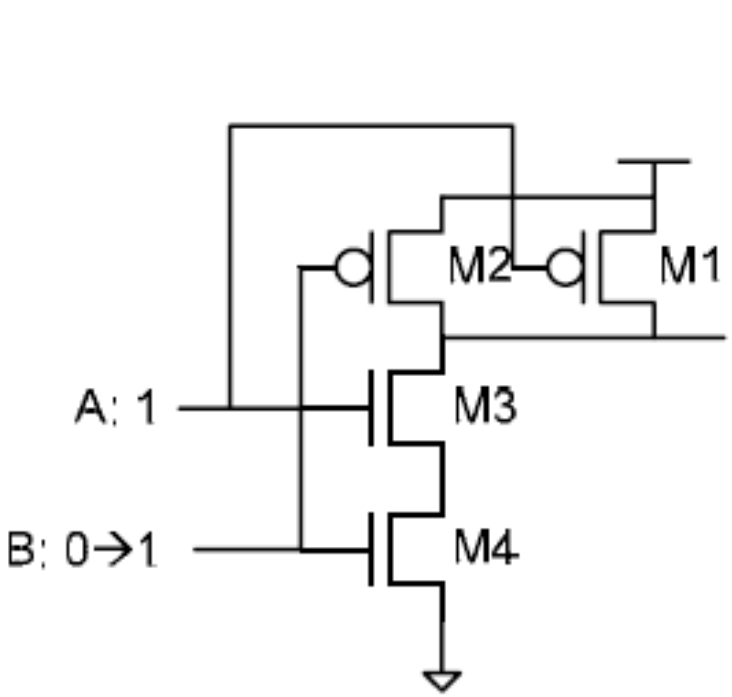
- Use RC model to estimate delay:

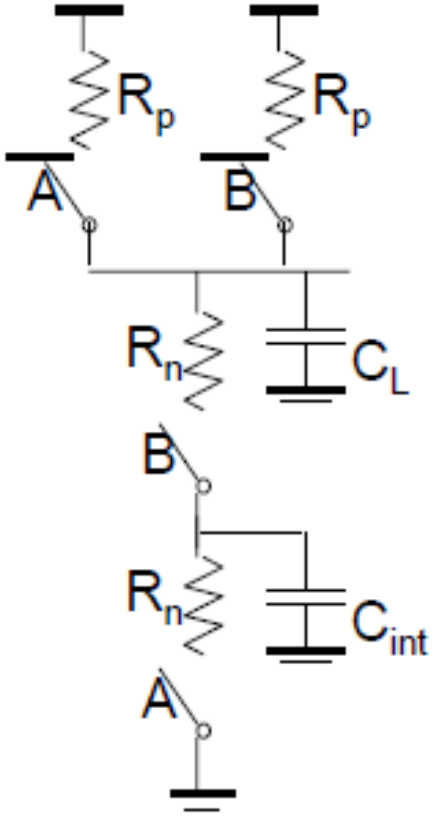




Complex Gate Delay (2)

- What is the delay in this case?





PROBLEM……

PROBLEM 2: Complex Gate Delay

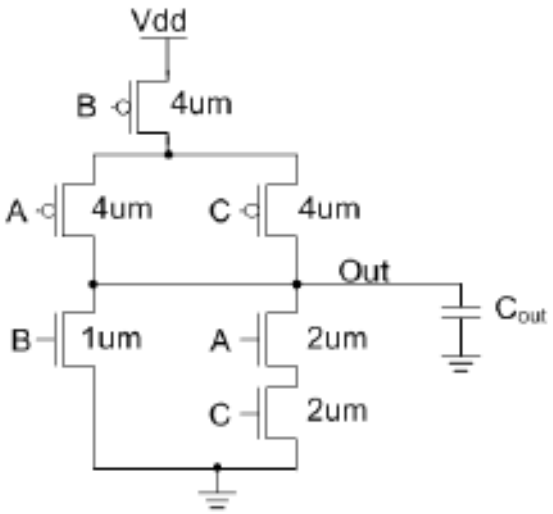
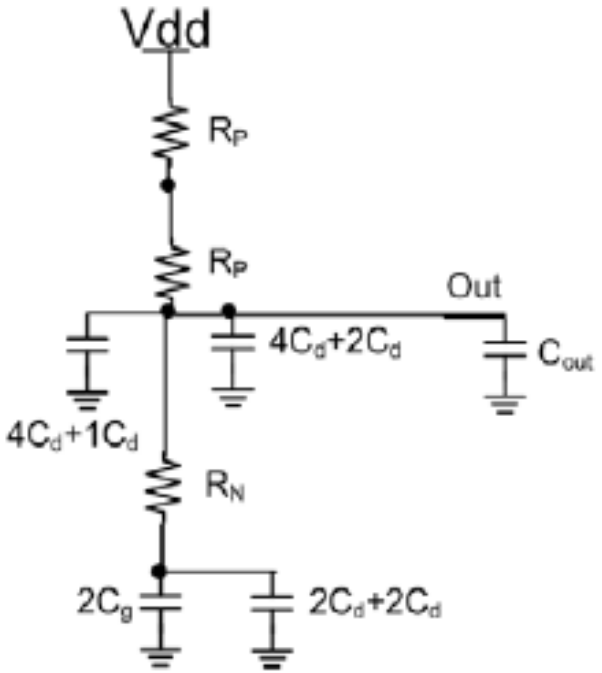


Figure 3.

For this problem you should assume that L_{min} = 100nm, C_g=2 fF/μm, C_d=1.6 fF/μm, R_p=20 kΩ/□, and R_n=10 kΩ/□, C_{out} = 12fF.

a) If A = 1 and B = 0, draw the switch model you would use to calculate the delay of the gate when C transitions from 1 to zero (i.e., the output going high).

Using the switch model, the equivalent RC circuit we would use to calculate the delay when A = 1, B = 0, and C transitions from 1 to zero is shown below.



b) What is the delay of the gate in this case?

Solution:

Using Elmore delay, the time constant for this circuit is:

$$\tau_{LH} = 2R_P\left(5C_d + 6C_d + 2C_g + 4C_d + C_{out}\right)$$

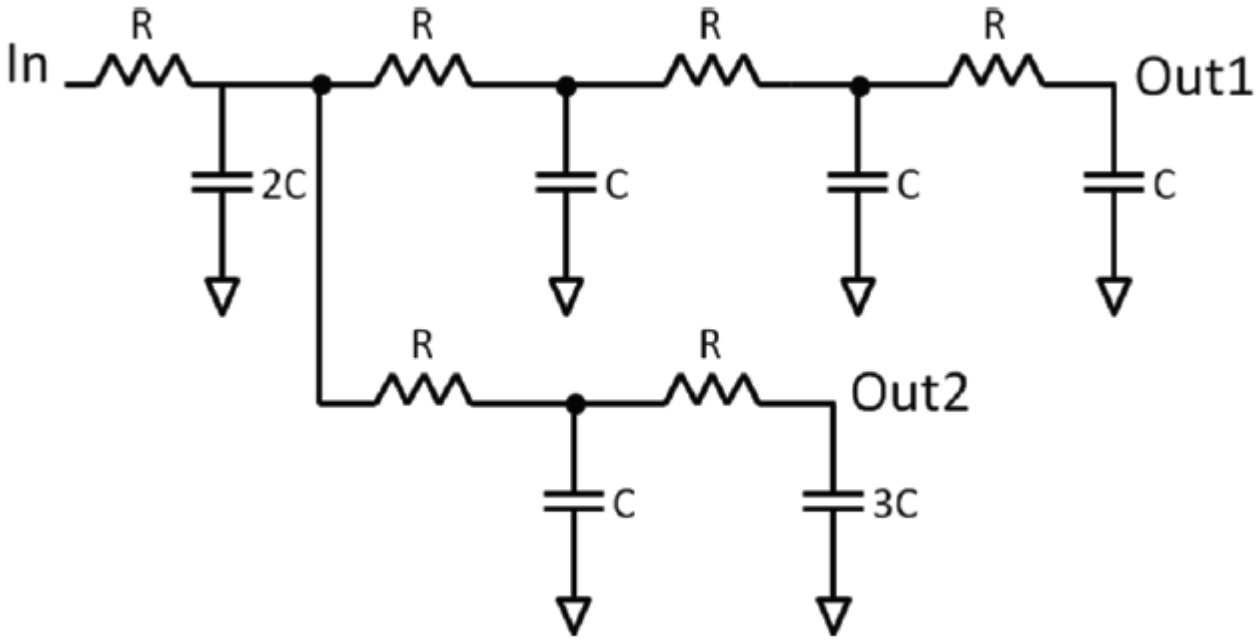
Where the resistance of each PMOS transistor is:

$$R_P = R_p\frac{L}{W} = 20k\Omega\frac{0.1\mu m}{4\mu m} = 500\Omega$$

Therefore, t_{pLH} for the gate will be:

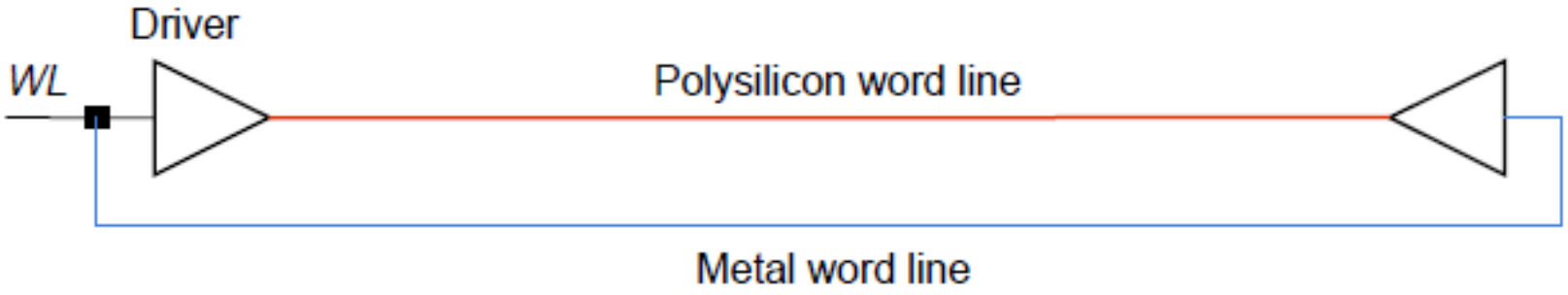
$$t_{pLH} = ln2 \times \tau_{LH} = ln2 \times 2 \times 500\Omega \times (5 \times 1.6fF + 6 \times 1.6fF + 2 \times 2fF + 4 \times 1.6fF + 12fF\ ) \approx 27.73ps$$

Calculate Elmore delay from In to out1 and from In to out2?

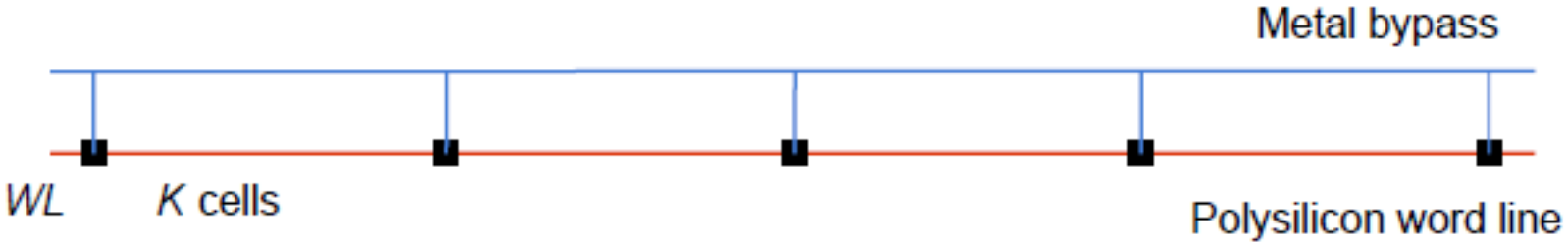


Solution:
Elmore to out1 is 15RC
Elmore to out2 is 16RC

Using Bypasses

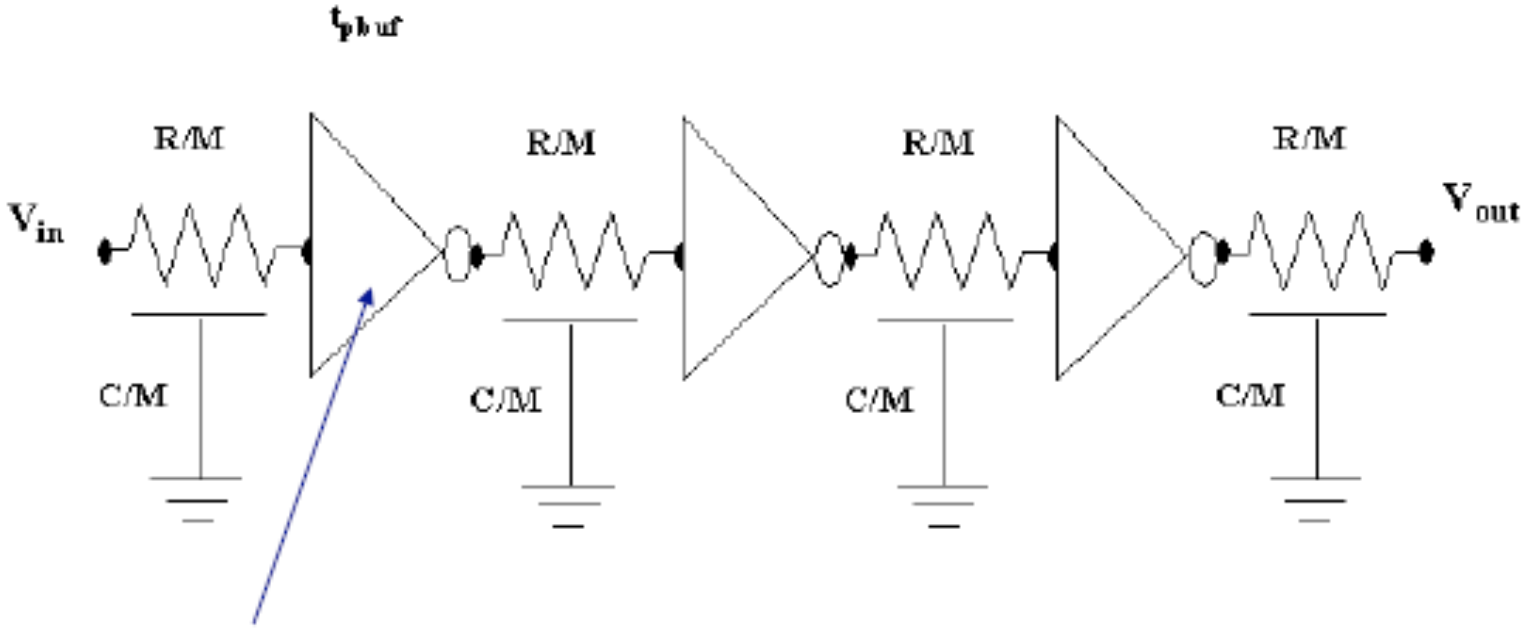


Driving a word line from both sides

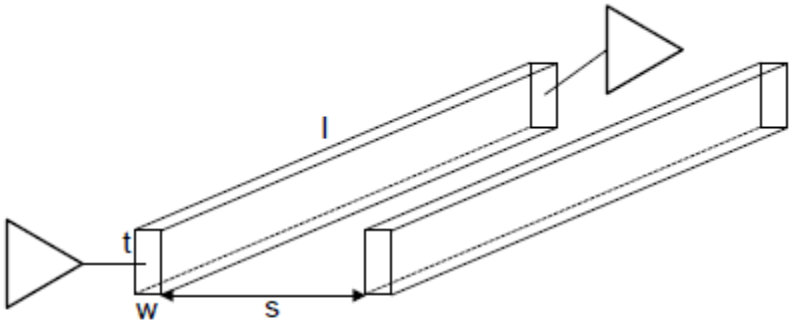


Using a metal bypass

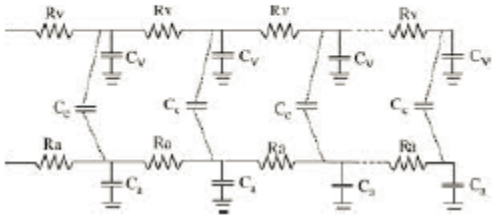
Reducing RC-delay Using Repeaters



Interconnect delay



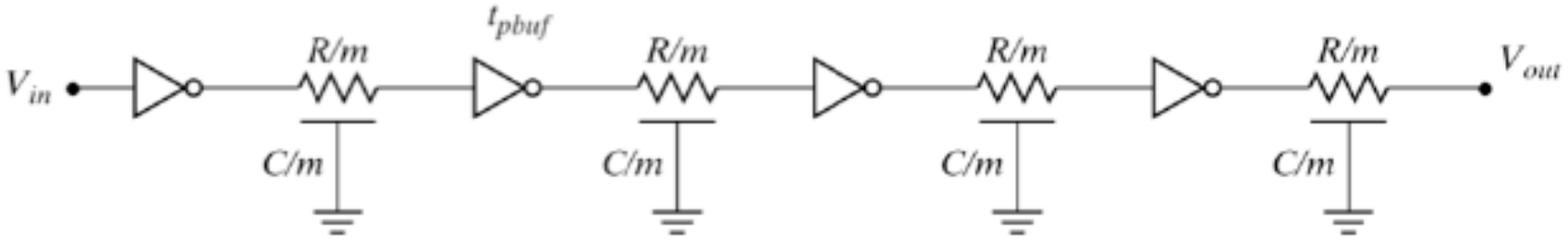
modeling



$$R = \rho \frac{l}{t \cdot w} \qquad C = \epsilon \frac{t \cdot l}{s} \qquad Delay \propto RC \propto l^2$$

- Extra

Repeaters



$$t_p = m\left(0.69\frac{R_d}{s}\left(s\gamma C_d + \frac{cL}{m} + sC_d\right) + 0.69\left(\frac{rL}{m}\right)(sC_d) + 0.38rc\left(\frac{L}{m}\right)^2\right)$$

$$m_{opt} = L\sqrt{\frac{0.38rc}{0.69R_dC_d(\gamma+1)}} = \sqrt{\frac{t_{pwire(unbuffered)}}{t_{p1}}}$$

$$s_{opt} = \sqrt{\frac{R_dc}{rC_d}}$$

Repeater Insertion (Revisited)

Taking the repeater loading into account

$$m_{opt} = L\sqrt{\frac{0.38rc}{0.69R_dC_d(\gamma+1)}} = \sqrt{\frac{t_{pwire(unbuffered)}}{t_{p1}}}$$

$$s_{opt} = \sqrt{\frac{R_d c}{rC_d}}$$

For a given technology and a given interconnect layer, there exists an optimal length of the wire segments between repeaters. The delay of these wire segments is independent of the routing layer!

$$L_{crit} = \frac{L}{m_{opt}} = \sqrt{\frac{t_{p1}}{0.38rc}} \qquad t_{p,crit} = \frac{t_{p,min}}{m_{opt}} = 2\left(1+\sqrt{\frac{0.69}{0.38(1+\gamma)}}\right)t_{p1}$$

Electric Model for Transmission Lines

$$\phi = \int B \partial S; L = \phi / I$$

$$\Delta\phi = IL\Delta x$$

$$Vad = \Delta\phi / \Delta t = ILv$$

$$C = Q / V; I = \Delta Q / \Delta t$$

$$I = Vad * C * v$$

$$==> v = 1/\sqrt{LC}$$

$$Z0 = V / I = \sqrt{L / C}$$

$$FromMaxwell's laws$$

$$v = 1/\sqrt{\varepsilon\mu} = C0/\sqrt{\varepsilon r \mu r}$$